# AN10710

## Features and applications of the P82B715 I²C-bus extender

Rev. 2 — 26 August 2010 Application note

### Document information

| Info | Content |
|---|---|
| **Keywords** | I2C-bus, twisted pair cables, Cat5e, Fast-mode, Fast-mode Plus, Fm+, inter-IC, SDA, SCL, P82B715, P82B96, PCA9600, AdvancedTCA, IPMB, SMBus, PMBus |
| **Abstract** | The P82B715 allows extending I²C-bus systems over long cables and to a total capacitance of about 3000 pF without compromising the important features of the I²C-bus. It causes minimal changes to bus logic signal levels and does not introduce any additional requirements on the levels of the signals that it handles. That makes it compatible will all I²C-bus devices and related buses and devices that use TTL switching levels instead of I²C levels. It permits inclusion of all other classes of I²C-bus buffers—even those that impose additional logic LOW level requirements on the bus signals or that use static level or dynamic level offsets. The slew control minimizes ringing and overshoot when driving I²C signals over twisted pair communication cables that have a low characteristic impedance (e.g., Category 5e and similar 4-pair cables, as typically used for Ethernet communications, are around 100 Ω). A quick design method is presented for cable design applications to 100 kHz and 30 m. Application examples include driving 20 m cables to 400 kHz in Fast-mode, a very large system for driving architectural LED displays that could include more than 240 m of cabling, and an AdvancedTCA radial IPMB distribution bus example driving 2800 pF. |

### Revision history

| Rev | Date | Description |
|---|---|---|
| v.2 | 20100826 | Application note; second release.<br>Modifications:<br>• Type number “IES5501” is replaced with “PCA9521”.<br>• Type number “IES5502” is replaced with “PCA9522”.<br>• Section 10 “Solution for Fast-mode systems that prohibit P82B715’s internal clamp diodes from its bus lines to $V_{CC}$”, third paragraph, third sentence is changed from “... typical 60 mV sinking 3 mA, ...” to “... typical 80 mV sinking 3 mA, ...” |
| v.1 | 20080528 | Application note; initial version. |

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# 1. Introduction

## 1.1 P82B715 characteristics and operating principles

The P82B715 is based on the earliest known attempts to extend the range of an I²C-bus using emitter-followers to increase the bus sink capability, creating a low-impedance bus that can support a large capacitance. The simple emitter-follower approach shown in Figure 1 sacrifices 0.7 V of valuable noise margin* (see Section 4) when the bus is LOW because the drop across the transistor's emitter-base means the low-impedance bus line can only be pulled down to a logic LOW level that is 0.7 V above the voltage at the I²C-bus driver's output, but it proved adequate in many applications.

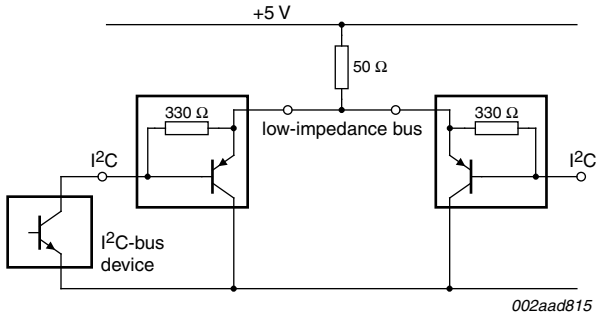



**Fig 1. Simple impedance converter using an emitter-follower**

The P82B715 refined this concept, leading to the equivalent function shown in Figure 2.

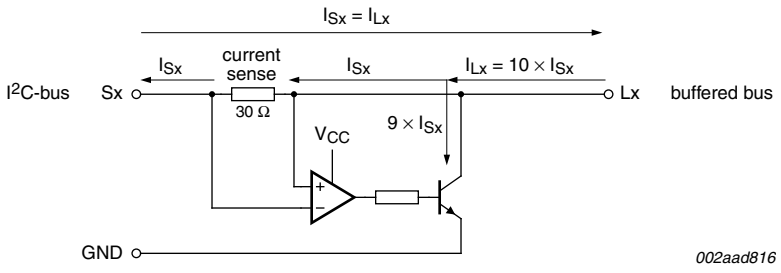



**Fig 2. Simplified equivalent circuit of P82B715**

The action of this circuit is very similar in function to the simple emitter follower but has important differences:

- The current amplification factor has been controlled. It is set to a factor ×10 so when the current sunk by the device at the Lx terminal is 30 mA that requires the I²C-bus device connected at the Sx terminal to sink 3 mA.
- The voltage drop across the 30 Ω sense resistor is always less than 100 mV so it hardly affects noise margin and enables applications in lower voltage systems (e.g., 3.3 V) where the extra 0.7 V offset would become significant.

At first the lower gain may appear to be a disadvantage because this arrangement now cannot drive the 50 Ω bus in the first example. The bus load current at Lx would be (5 V − 0.5 V) / 50 Ω = 90 mA and that would require the I²C-bus device to sink 9 mA.

The key lies in the reverse situation, where the I²C-bus has a capacitance that must be charged as the bus rises. When the buffer has a gain of ×10 a capacitance of 100 pF on the I²C-bus at Sx becomes equivalent to a capacitance of 1000 pF to be charged up by the low-impedance bus and that slows its rise. In the simple emitter-follower version, where the transistor could have a gain of 200, the equivalent capacitance to be charged by the low-impedance bus becomes 100 pF × 200 = 20 nF and that would cause very slow rising edges. Of course, if another pull-up resistor is always used on the I²C-bus (or at the Sx terminal) and it is selected to cause the I²C-bus to attempt to rise faster than the low-impedance bus, then neither the emitter-follower nor the amplifier in P82B715 would be activated. While not essential for operation of either circuit, it will be shown that it simplifies system design and is 'good design practice' to fit such pull-ups on the Sx side.

The P82B715 is not a symmetrical device, and it does not truly 'buffer' or isolate the loading on one I/O from the other. When the Lx side of the device is pulled LOW, the Sx side is simply pulled LOW via the internal 30 Ω current sense resistor. None of the amplification circuitry is activated; the device is simply equivalent to a passive 30 Ω resistor. It therefore creates no significant signal delays and the maximum static voltage drop across the 30 Ω resistor will only occur when the Sx pin sinks the I²C-bus maximum static 3 mA.

The chip is specified to have a maximum static offset (Lx/Sx difference) of 100 mV and when driving lighter loads at Sx it is even smaller. Note that the device on the Lx side must sink, via the sense resistor, the I²C-bus current that is sunk at the Sx pin. The Sx and Lx currents are equal in magnitude as illustrated at the top of the figure. If the Sx side is pulled LOW then current flows from the Lx side in the current sense resistor and this activates the amplifier and causes a current 9 times larger than the sense current to flow to ground in the transistor as shown. That means the total current flowing into the Lx terminal will be 10 times the current flowing out the Sx terminal. A device at Sx sinking the allowed I²C-bus load of 3 mA can thus cause an Lx sink current of 30 mA. During falling edges, an I²C-bus with significant capacitive loading requires the I²C driver to sink a 'dynamic' current that is approximately double the usually quoted 3 mA 'static' sink current. The P82B715 then sinks higher peak currents at Lx.

In this active mode there is some delay before the ×9 sink current flows in the transistor, and therefore some delay before 30 mA can flow. During this delay time the only current flowing into Lx can be the current flowing out Sx to the I²C device. That can mean the driver at the Sx pin cannot drive this pin LOW until the buffer 'assists' with the large sink current. The delay is only around 250 ns, but the important point to note is that the input voltage at Sx cannot go LOW before the output voltage at Lx goes LOW.

> **RULE:** The input and output voltages of this type of buffer are always essentially equal. The buffer has no separate 'input' and 'output' **voltages**; the two must always be nearly equal. The voltage difference, in either direction, never exceeds the voltage calculated by simply multiplying the Sx current by the internal 30 Ω sense resistance—and for practical purposes its static value will always be found to be under 100 mV. The 'input' and 'output' **current** magnitudes can be different, but only if current is flowing out of Sx.

When designing this type of buffer into an I²C-bus system the designer must make allowance for its input-output offset voltage. Compliance with I²C-bus Fast-mode specification for hysteresis and noise margin requires the I²C-bus lines of the system be correctly controlled (driven by the buffers) whenever the bus voltage is required to be low. With a bus voltage $V_{CC}$ that means whenever at or below $0.25V_{CC}$, the maximum allowed bus LOW level. P82B715 has a maximum offset of 100 mV so the system designer should

ensure the buses at either side can be driven down to ($0.25V_{CC}$ − 0.1 V). For the usual system, that will use two P82B715s in series with their Lx sides linked and will therefore add two offsets, it means the I²C-buses connected at either Sx terminal need to be driven below ($0.25V_{CC}$ − 0.2 V). For example, a 3.3 V bus system requires the designer to ensure the buses connected at either Sx can be pulled below ($0.25 \times 3.3$ V − 0.2 V) = 0.63 V to guarantee the Fast-mode I²C-bus low voltage level specification at the other Sx is met. Because all devices for driving an I²C-bus are required to drive their output LOW to 0.4 V max this requirement can be met, and there is even some margin left (0.23 V) for adding series transient suppression resistors or other buffers where those are required.

When calculating the rise or fall times for bus edges, the same rule applies: the input and output (voltage) rise and fall times must be the same. Rise time will be determined by whichever side has the slower rise. For P82B715 the propagation delay measured in the conventional way, that is when referenced to logic voltage levels, is essentially zero in both directions. That does not mean that this buffer does not ever introduce any propagation delay but simply that, when it does, both the applied drive and the output waveforms remain essentially identical. They will both exhibit the delay caused by the buffer. The data sheet gives the ‘effective’ propagation delay that will be caused when the buffer is active. It can still be difficult to determine exactly what is causing an observed resultant delay. Designing for approximately equal natural bus rise times (product of pull-up resistor and bus capacitance) on each side of the buffer will keep the buffer inactive during rising edges and simply avoids the problem on rising edges. Falling edge delays, which will include the 250 ns delay in activating the buffer, will normally not be as significant as the bus rise time in system design.

This style of ‘buffer’ should not strictly be called a buffer because it does not provide any isolation between the buses connected on its two sides. This bus ‘extender’ is simply a unidirectional current amplifier, with bidirectional unity voltage gain, used as an impedance converter. The two buses that it connects are always linked by the 30 Ω resistor inside the chip. That is why there can be no isolation, and logic voltage level shifting is not possible.

## 2. Important characteristics of this type of buffer

This device operates with a very low difference in voltage between its Sx and Lx I/Os, making the logic signal levels on its Sx side compatible with virtually every I²C device and I²C buffer—including those buffers that use special logic switching levels on some I/Os.

Just like all true I²C-bus devices, there is no restriction on interconnecting multiple buffers together using either of their I/Os. (The usual practical restriction on total I²C bus capacitance applies and, uniquely for this part, calculation of the effective I²C-bus loading must take account of ‘transformed’ loading—$^1/_{10}$ of the loading at Lx becomes part of the total loading on the I²C-bus at Sx.)

It has slew-control on its amplifiers to minimize ringing and overshoot when driving cables.

## 3. Where is this part most useful?

The P82B715 is most useful when:

1. Driving long wiring. With a buffer at each end of twisted pair cables, for example the pairs found in Cat5 Ethernet wiring, and when operating with a 5 V bus supply, driving at least 30 m of cable is possible.

   To avoid ringing/overshoot a cable needs to be terminated by its characteristic impedance, meaning 100 Ω at each end, but that is much lower than the allowed pull-ups can provide. The practical alternative is to use relatively slow bus rise/fall times as produced by this buffer.

2. When building relatively short bus systems that have much more capacitance than the 400 pF specification and where the bus logic levels would not be compatible with the special logic levels used by other types of buffer such as P82B96. When correctly designed it is possible to have a total system capacitance of around 3000 pF running with bus logic voltage levels on the Sx I/Os that are compatible with all I²C or related devices and with all types of buffer. One example of that application is its use as the signal distribution buffer for an analog radial IPMB as used in AdvancedTCA systems. In those systems it is normal to find plug-in modules with buffer types having non-compliant logic switching levels that require IPMB logic low levels of 0.4 V.

   P82B715 makes it easier to meet that requirement by:

   a. its low typical input-output differential (or 'offset') below 70 mV, and

   b. minimizing the offsets across those other buffers by keeping their loading within the limits specified for a bused IPMB.

## 4. Cable drive applications

P82B715 allows extending an I²C-bus at relatively high speeds via a cable up to at least 30 m long.

Figure 3 shows the P82B715 converting the signals from an I²C-bus with a master microcontroller (left) to a lower impedance bus and back to an I²C on the right with an I²C slave. In this example it is assumed that the master and slave have 5 V compatible I/Os so their I²C-bus runs at 5 V.

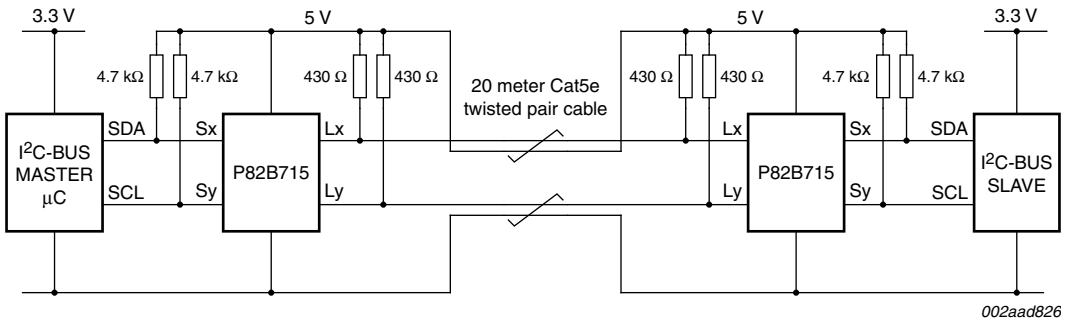



**Fig 3. A pair of P82B715s permit including a 20 m cable extension**

If the parts have I/Os rated only for 3.3 V, then the whole system may simply be run at 3.3 V as shown in Figure 4. In Figure 4 the de-rated performance guarantees for P82B715 on 3.3 V bus (24 mA guaranteed sink) mean the pull-ups have the same value as for the 5 V case and they cannot be scaled down as would normally be possible on a lower voltage bus. The same arrangement in Figure 4 is used when 5 V master and slave parts are used on a 5 V bus.

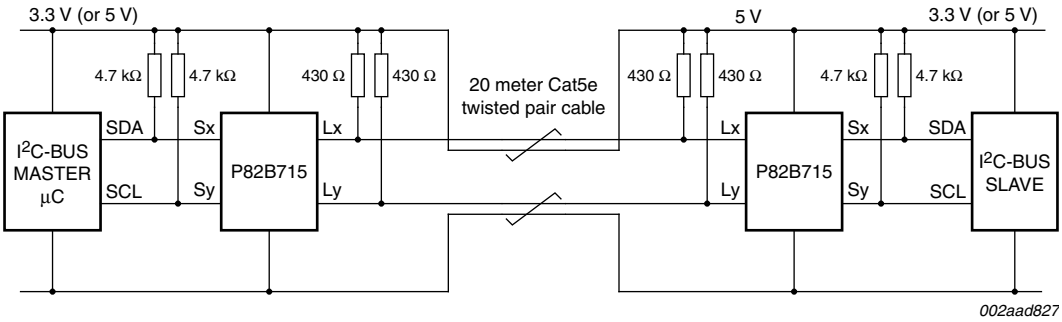



**Fig 4. Same arrangement as Figure 3 except for equal chip/bus operating logic signal levels**

When the I²C chips and their pull-ups run with 3.3 V supply the logic signals on the cable bus are 3.3 V logic levels, independent of whether P82B715 has the 5 V supply as in Figure 3 or the 3.3 V supply option in Figure 4. The noise margins of the whole system when the bus is LOW are limited by the noise margin (LOW) of a 3.3 V system. Running the P82B715 at the 5 V levels in Figure 3, or Figure 4 using the 5 V supply option, still has two advantages. Firstly, the noise margin when the bus is at the logic HIGH level (the quiescent state) is greater, and secondly, the P82B715 has its full rated performance because its supply is 5 V. The bus has higher impedance when it is HIGH, as determined by the pull-ups, than when it is driven LOW by one of the I²C chips. The higher impedance bus is more susceptible to capacitively coupled noise, so the larger noise margin of a 5 V system is advantageous. The lower impedance of the Lx/Ly bus also helps.

*[The noise margin of a logic system is the difference between the voltage actually present on the bus and the voltage level that would represent the opposite logic level. It is the 'safety margin' of the system. When the bus is LOW, the noise margin (LOW) is the difference between the bus LOW level (typically under 200 mV) and the level that is a logic HIGH—usually around $V_{CC}$ / 2 but in any case, for a compliant I²C-bus, greater than $0.3V_{CC}$. When the bus is HIGH it settles close to $V_{CC}$, and the level required to cause a false logic LOW is again around $V_{CC}$ / 2, but in any case guaranteed to be below $0.7V_{CC}$.

**Example:** System in Figure 3. The guaranteed bus LOW level at the slave is < 0.6 V when the master is at its maximum allowed 0.4 V, but typically it will be below 0.2 V. The switching level for 3.3 V logic is around 1.65 V so the typical noise margin (LOW) is at least 1 V while the guaranteed margin is ($0.3V_{CC}$ − 0.6 V) = 0.3 V. When the bus is HIGH it is approximately 5 V. The level required for a LOW on the 3.3 V logic is typically 1.65 V but guaranteed less than 2.3 V so the noise margin (HIGH) is typically 3.35 V and the guaranteed margin is 2.7 V. Bus levels quoted are for Standard-mode.]

Pull-up for the system in Figure 3 (or Figure 4 with 5 V supply) are calculated as follows:

1. The maximum static sink capability of the master or slave is 3 mA. The master (or slave) must sink the current in its local pull-up (4.7 kΩ) plus $\frac{1}{10}$ of the current sunk at the Lx terminal of its P82B715. It is 'good practice', and it generally simplifies design, to have pull-ups on all the bus segments. It is also simplest to make the design symmetrical unless either the master or slave bus has an unusually high capacitance.
2. Because the P82B715 gives ×10 gain, allocating about 30 % of the 3 mA sink current to each local I²C will yield low-impedance bus pull-ups each around 10 times lower than the local I²C buses. In turn that allows up to 30 % of the normal 400 pF on each I²C-bus and around 70 % of 4000 pF on a low-impedance (100 kHz) bus. See Section 5 for details.
3. If the system is required to operate above 100 kHz it must then comply with Fast-mode bus rise times. For a 5 V Fast-mode bus, the capacitance on an I²C-bus must be less than 240 pF, so on the ×10 lower impedance bus less than 2400 pF. The 30 % allocation then represents 72 pF on the local I²C-bus, while the 70 % allows up to 1680 pF on the cable bus.

In its usual application mode the P82B715 amplifies the normal I²C-bus signals to allow driving long cables having a lower impedance. This enables the usual I²C-bus communications to be used between two or more widely separated modules that already use I²C for their internal communications.

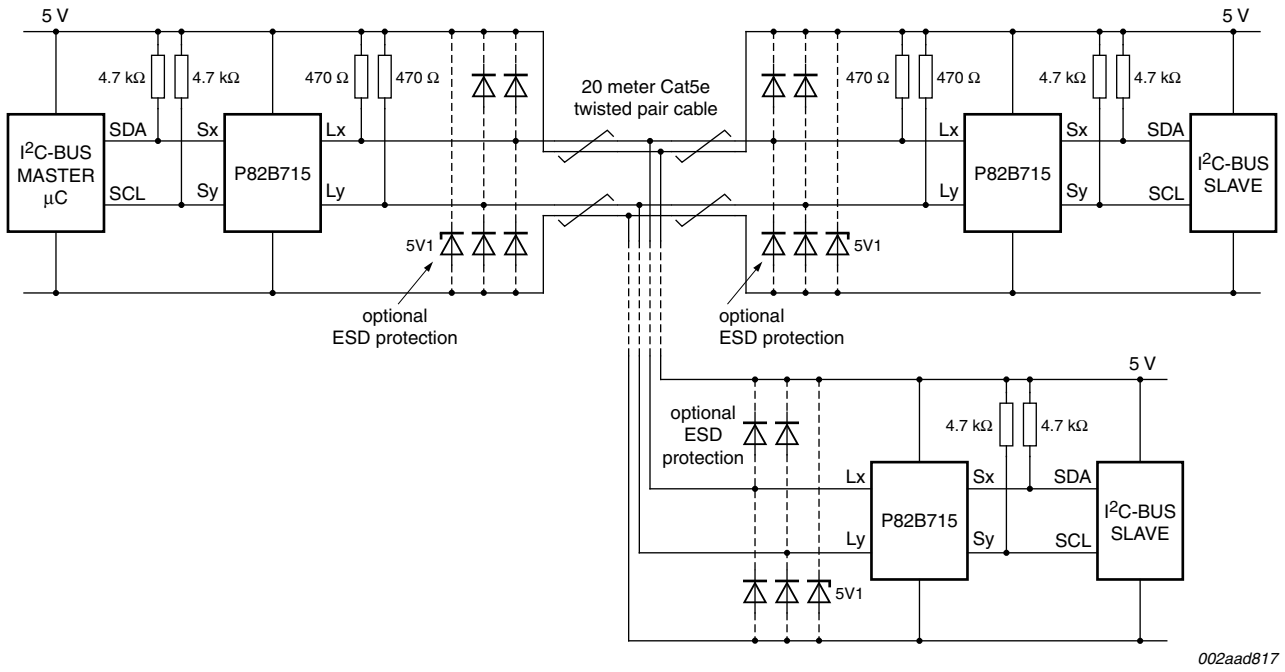
With many variables—cable length/capacitance, local capacitive loading on each I²C-bus, bus voltages, bus speed—optimizing a design can be complex.

# 5. Simplified design approach

P82B715 offers adequate performance for cable lengths up to 30 m and bus speeds up to 100 kHz. Longer distances and higher speeds are possible but require more careful design. With many variables—cable length/capacitance, local capacitive loading on each I²C-bus, bus voltages, and bus speed—optimizing a design can be complex and requires significant study of the data sheet and application information.

## 5.1 Proven circuit with the P82B715

To allow easy implementation, the circuit and simplified approach shown in Figure 5 has been checked to provide adequate performance in the typical 100 kHz application and can be directly implemented by using the values and circuit shown for a point-to-point application (up to 30 m), and, if additional nodes need to be added along the way, in multi-point applications.




**Remark:** Cable bus pull-ups only fitted at the cable ends, not fitted to modules connected along cable.

**Fig 5. P82B715s interfacing standard I²C-bus signals to twisted pair cables up to 30 m long**

Here are the rules that were followed in the simplified approach to Figure 5:

1. Allocate about ⅓ of the allowed bus sink current (3 mA) to each of the normal I²C-buses and ⅔ to driving the cable bus. That means each I²C-bus sinks about 1 mA and 2 mA is available to drive Sx/Sx. The ×10 gain of P82B715 then allows 20 mA loading at Lx/Ly on the cable bus.
2. The pull-up on each I²C-bus is ($V_{CC}$ − 0.4 V) / 1 mA = 4.6 kΩ. Use 4.7 kΩ as the nearest usual value.
3. The net pull-up on the cable bus can be ($V_{CC}$ − 0.5 V) / (21 − n) mA where n = total number of P82B715 modules on the cable. When there are only two modules, one each end of the cable, the pull-up = (4.5 / 19) = 237 Ω. (The remote I²C-bus uses 1 mA of the allowed 20 mA. The buffer offset increases the maximum bus LOW from 0.4 V to 0.5 V.)
4. Make the pull-ups at each end of the cable equal. Signalling is bidirectional so there is no advantage optimizing for any one direction. The pull-up at each end will be 474 Ω. Again, select 470 Ω as the nearest usual value.
5. The 100 kHz rise time requirement is 1 μs. Meeting this requires the product of the bus capacitance and pull-up resistor on each bus section to be less than 1.18 μs. This sets one capacitance limit. With 4.7 kΩ pull-ups the I²C limit is 250 pF each, while the 235 Ω sets a cable bus limit at 5000 pF.
6. The 300 ns bus fall time, and the standard I²C-bus limit specification limit of 400 pF, must also be observed. The 400 pF limit is a measure that ensures the fall time specification will be met. Again allocate about ⅓ of this 400 pF limit, or 133 pF, to each I²C-bus leaving ⅔, or 266 pF, for the cable bus loading as it will appear at the Sx/Sy pins. The ×10 gain of P82B715 allows the loading at Lx/Ly to be 10 times the load at Sx/Sy, so 2660 pF maximum. The loading at Lx/Ly due to the other standard buses is 133 pF each so their total should be subtracted from the maximum. For just one remote module the cable capacitance may then be up to (2660 − 133) = 2530 pF. For typical twisted pair or flat cables, as used for telephony or Ethernet (Cat5e) wiring, that capacitance is around 50 pF to 70 pF per meter, so the cable could, in theory, be up to 50 m.
7. If there are severe EMI/ESD tests to be passed, then large clamp diodes can be fitted on the cable bus at each module to $V_{CC}$ and to ground. They may be diodes rated for this ESD application, or simply large rectifiers (1N4000). The low-impedance bus easily accommodates their relatively large capacitance. The P82B715 does not provide any isolation between Lx and Sx so this clamping method provides the best protection for the lower voltage I²C-bus parts. The $V_{CC}$ supply should be bypassed using low-impedance capacitors. Zeners may be fitted to prevent the supply rising due to rectification during very large interference.

## 5.2 P82B715 waveforms in Figure 5

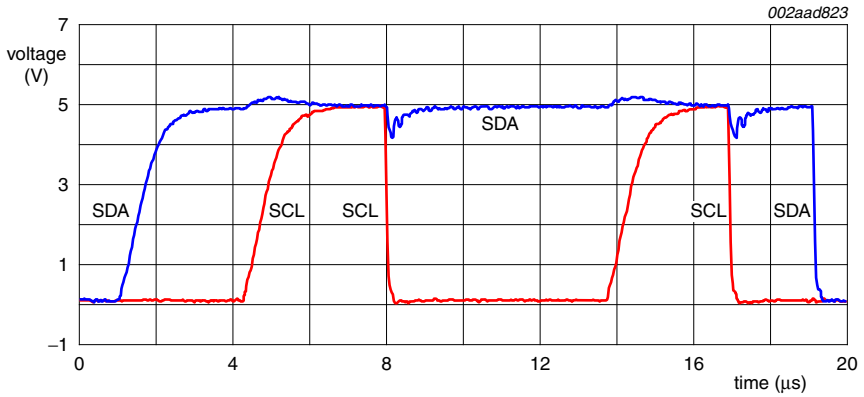



**Fig 6. Waveforms at input to Sx at sending end of 20 m cable using the arrangement in Figure 5**

Slight cross-coupling of SCL edges to SDA is present while the SDA line is HIGH and therefore higher impedance. Notice that (capacitive) coupling is not evident on SCL for changing edges of SDA because SCL has a very low impedance while held LOW by the P82B715.

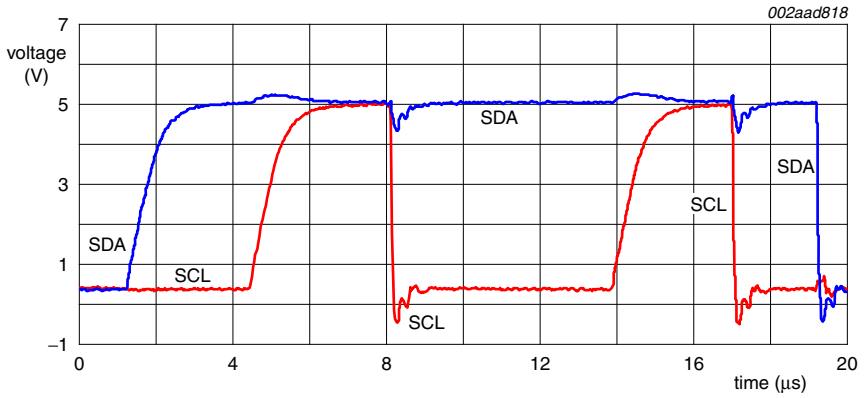



**Fig 7. Waveforms output by Sx at the receiving end of the arrangement in Figure 5**

Slight ringing is evident on falling edges, mostly due to the fast/strong drive from a 74HC05 gate on the I²C-bus driver board. Otherwise the waveforms closely resemble the driving waveforms. The offsets through the two P82B715s are very small and the $V_{OL}$ of the received signal is still under 400 mV. This low offset makes the P82B715 attractive in applications where the signals must interface to chips that do not use I²C-bus compliant logic switching levels, for example TTL or other classes of buffer that require special logic LOW levels for their operation (e.g., the Sx I/O of P82B96 and both I/Os of PCA9511A).

## 5.3 P82B96 waveform when substituted for P82B715 in Figure 5

For comparison, the waveforms output by a P82B96 connected in place of the receiving P82B715 and with the same arrangement and pull-ups as in Figure 5 are shown in Figure 8.

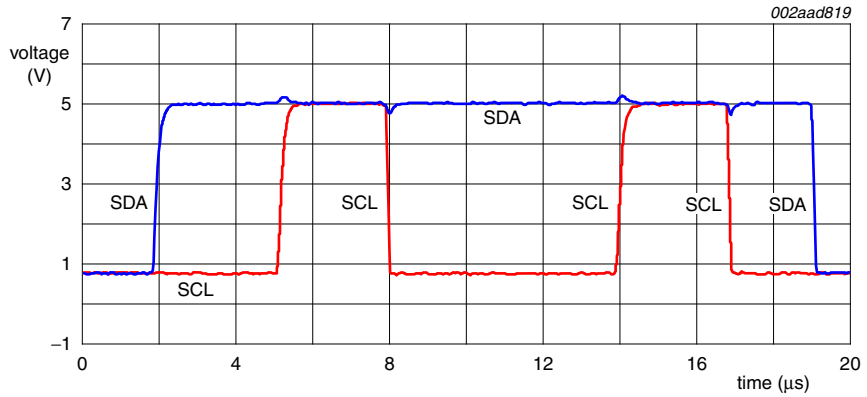
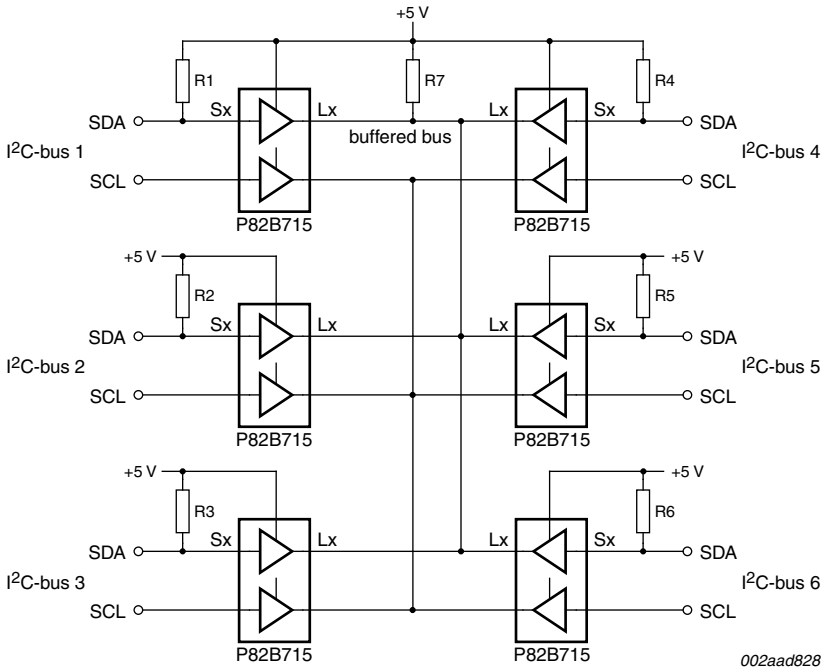



**Fig 8. Waveforms at Sx/Sy outputs of P82B96 replacing the receiving P82B715 in the arrangement of Figure 5**

The different mode of operation of buffers like P82B96 is evident in the traces of Figure 8. Note how the cross-coupled noise/ringing/disturbances on the cable bus cannot pass through this 'isolating' design of buffer. The outputs are clean and have fast rise/fall times that are determined only by the bus loading at Sx/Sy. The rise/fall times present on the cable bus input at Rx/Ry do not affect the Sy/Sy output rise/fall times. There is some small cross-coupling of SCL edges into the SDA signal when SDA is HIGH and therefore has high impedance; in this case 4.7 kΩ. This cross-coupling is due only to capacitive coupling between the P82B96 Sx and Sy lines and the faster rise/fall times of SCL. Still SDA edges cannot couple into SCL when SCL is LOW because Sy/Sy of P82B96 are low-impedance while LOW.

An important point of difference is the $V_{OL}$ of the Sx/Sy on P82B96 is much higher than for P82B715 in Figure 7. The typical $V_{OL}$ of P82B96 at the 1 mA sink current of the 4.7 kΩ pull-up is just under 0.8 V at 25 °C. That level is not compatible with some other buffers that use special levels to achieve a load isolating type of buffering. The limit specification for Sx/Sy of P82B96 is also above 0.8 V at low temperatures and/or usual bus currents, creating problems with worst-case design tolerances when interfacing to parts that use TTL levels instead of I²C-bus levels. While, in practice, those TTL devices are compatible with P82B96, their worst-case compatibility is not guaranteed. PCA9600, with guaranteed TTL level compatibility offers an alternative in that case, but it still cannot provide the compatibility of P82B715 with all other buffers.

## 6. Using P82B715 to increase the total allowable I²C system bus capacitance




For clarity, bus capacitance loadings and SCL pull-ups have been omitted.

**Fig 9. Building a large I²C-bus system with up to 3000 pF total loading**

Figure 9 shows an I²C-bus system in which six I²C-buses are linked via P82B715s to a central buffered bus connected on their Lx terminals. In this application of P82B715 a large total system capacitance is divided into a number of bus segments (like the six shown) where the loading capacitance on each section is made roughly equal (to simplify the design), but anyway kept less than about half the bus capacitance allowed by the speed/voltage requirements of the I²C class. For a Standard-mode bus that means 200 pF (half the specified 400 pF), or to meet the 300 ns rise time for a 5 V Fast-mode bus that limit is 240 pF and each section would be kept below 120 pF. A practical system capacitance limit is about 3000 pF. While the theoretical total may approach 4000 pF, that would require an impractical number of bus segments. Even 20 segments will only permit a 2760 pF total, with 138 pF each, and in practice each must include an allowance of at least 20 pF for its buffer.

There are three I²C-bus specification requirements to consider when designing this system:

- The static loading on each I²C-bus. It must not exceed 3 mA
- The bus rise time for the bus speed selected.
- The bus fall time.

Because these requirements are inter-dependent, system optimization would be difficult. A practical approach is to minimize the variables and to design only to meet the system minimum requirements.

Meeting the bus fall time will require that the effective loading on each bus should not exceed the 400 pF specification limit. It is not necessary to consider any other limits as perhaps set by Fast-mode and higher voltages. For a total of N segments, each having a local loading C pF, the effective capacitance loading on each is segment will be:

$$effective\ loading\ on\ each\ I^2C\text{-}bus\ segment = C + \frac{1}{10}(N-1)C \quad (1)$$

To determine the minimum number (N) of (equally loaded) segments required to support a given total system capacitance (CT, in pF), or the total capacitance possible for a given number of segments, use one of these expressions:

$$number\ of\ segments\ required\ N \geq \frac{9 \times CT}{(4000 - CT)} \quad (2)$$

$$total\ system\ capacitance\ (pF)\ CT \leq 4000 \times \frac{N}{(N+9)} \quad (3)$$

**Example:** For a total system capacitance of 1000 pF the minimum number of segments would be 3, each 333 pF. The loading on each I²C-bus will become 333 + $^1/_{10}$(2 × 333) = 399 pF.

Next, select the maximum value for the pull-up resistors that just allows meeting the required I²C rise time. Select each pull-up so the product of its resistance and the bus capacitance is 1.18 times the rise time requirement. For a standard 100 kHz bus the I²C rise time required is 1 μs so the necessary RC product is 1.18 μs. In the example with 333 pF loading on each of three segments, the maximum resistance (R1, R2, R3) = 1.18 μs / 333 pF = 3.53 kΩ. For simplicity, and some safety margin on rise time, select these pull-ups as 3.3 kΩ.

The common node where the Lx pins join will have a capacitance approximately 10 pF for each IC and 3 pF for each inch of connecting PCB track. In a system with just 3 segments that will be less than 50 pF, requiring a pull-up (R7) of approximately 23.6 kΩ. Fitting 22 kΩ gives a small safety factor. (For such a simple system, that node could in fact be ignored and no pull-up fitted. For larger systems this node will require either that the calculated pull-up be fitted **or** that the Lx loading contribution (per IC) be accounted for by added it into the Sx side's load capacitance used for timing calculations.)

Check the DC static bus loading. The DC load on each I²C-bus is calculated by adding $^1/_{10}$ of the loading on the common Lx point to each I²C-bus local loading.

When one I²C-bus drives the system LOW, its local P82B715 will be active, providing a gain of ×10, but all other P82B715s will remain passive and their I²C-buses will be driven low via their internal 30 Ω resistance. That means the effective loading at the common Lx point is simply the parallel combination of all the pull-ups on the other I²C-buses and the pull-up (if any) on the common node. In the example with 1000 pF and 3 branches, with an Lx pull-up, the total loading at Lx is the parallel combination 3.3 kΩ, 3.3 kΩ, 22 kΩ = 1.53 kΩ. The P82B715 reduces that to a loading of 15.3 kΩ at its Sx side where it appears in parallel with the local 3.3 kΩ to produce a net static loading of 2.7 kΩ. That is above the minimum of 1.53 kΩ allowed on a 5 V bus.

**Example:** Calculations for a system as in Figure 9, with a total of 6 segments, and required to meet Fast-mode timing.

Maximum total capacitance allowed so that fall times will be met is calculated from Equation 3. Maximum total capacitance = 400 × (60 / 15) = 1600 pF. Each segment will be maximum 1600 / 6 = 267 pF and we will allow 13 pF for the loading at Lx and no pull-up will be fitted at Lx. The allowed maximum loading at each Sx becomes 267 − 13 = 254 pF. That must include provision for 10 pF loading by the Sx pin so the external wiring plus I²C-bus device loading must be kept below 244 pF on each I²C-bus. The fall time requirement sets one limitation. This requirement means the external connected buses could have up to 6 × 244 = 1464 pF in total.

The 5 V Fast-mode requirement imposes an additional requirement that the effective bus loading capacitance on an isolated I²C-bus be kept just below 240 pF so the 300 ns rise time is met when the pull-up has its minimum allowed value for 5 V of (5 V − 0.4 V) / 3 mA = 1.533 kΩ. (The RC product for 1.533 kΩ and 240 pF is 368 ns and the corresponding I²C-bus rise time is 368 / 1.18 = 311 ns).

To have the fastest possible rise time, design with the limit static loading (i.e., set each effective I²C-bus loading to 1.533 kΩ). That loading on each bus is made up by its local load in parallel with a resistor 10 times the resultant of the 5 other I²C-bus pull-ups in parallel. (The Lx loading capacitance will be included in each Sx loading, so no resistor R7 is used.)

Effective loading = R1 in parallel with 10 times the loading due to the parallel combination of R2 through R6. When all resistors R1 through R6 are made equal, that loading becomes R1 in parallel with 10(R1 / 5) = 0.667 R1. The minimum is 1.533 kΩ, so R1 must be 2.3 kΩ (or greater). Selecting 2.4 kΩ provides a small margin on the static loading. To meet the Fast-mode 300 ns rise time requirement, the RC product must be 354 ns. The allowed capacitance with 2.4 kΩ is 150 pF. Fast-mode operation sets an additional capacitance limit at just 150 pF per segment, so the total allowed 5 V Fast-mode system loading is 900 pF.

If the bus voltage is reduced to 3.3 V, each pull-up can be 1.45 kΩ and each load increases to 238 pF, for a total 1430 pF. If the requirement was 5 V Standard-mode, the rise time requirement of 1 μs would set a capacitance limit per segment of 1.18 μs / 2.4 kΩ = 490 pF. In this case the rise time is not a limiting factor. The fall time requirement then sets the system capacitance limitation as above.

In practice, I²C-bus devices have a dynamic sink capability much greater than the minimum required to achieve the bus fall time driving the 400 pF limit and fall times will be no problem. As I²C-bus devices do not publish that dynamic sink capability, it is not possible to make those relevant calculations but, in practice, meeting the rise time will be found to set the practical system limitation. Some I²C derivative buses (for example IPMB in AdvancedTCA) allow a bus loading above 400 pF. Then fall time requirements should be calculated by adapting Equation 1 through Equation 3 to their allowed maximum capacitance. The ‘4000’ in those expressions represents 10 times the appropriate allowed bus capacitance. 400 pF is used for I²C-bus. The pull-up calculations for IPMB must also be adapted to the limit defined for those systems.

This arrangement is useful in extending systems that include TTL logic levels because P82B715 does not affect any of the logic thresholds in the system. Just be aware that failure of any $V_{CC}$ supply to any of the devices in these systems will result in holding the bus LOW because P82B715 has internal diodes from all I/Os to $V_{CC}$. In systems where that may cause problems it is necessary to use FET isolating switches, for example the overvoltage tolerant 74LVCV2G66.

## 7. Including logic level shifting by using a low cost transistor

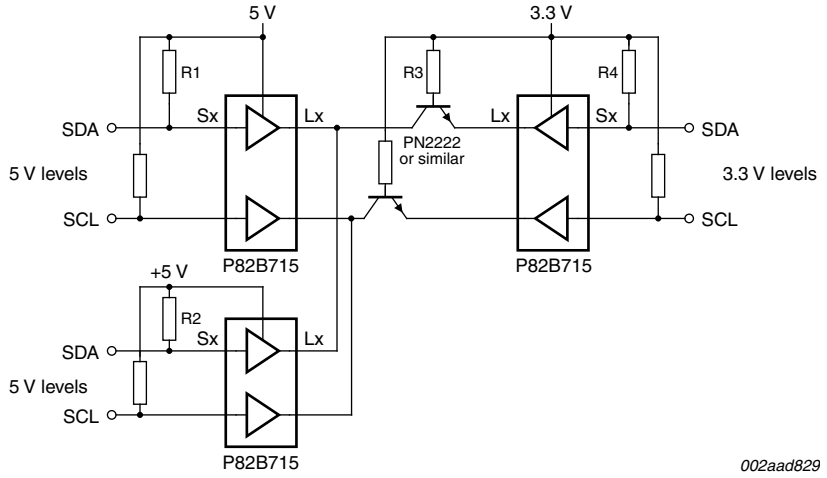



**Fig 10. Including level shifting via external transistor**

Figure 10 shows how Figure 9 can be adapted to include logic level shifting while retaining the feature of minimal logic level offsets as required when handling non-standard I²C-bus levels such as TTL levels or interfacing with buffers that have special logic levels. As in Figure 9, it is possible to extend the total system capacitance well beyond the 400 pF limit, but there is now the restriction that there must be a pull-up (R3) on the Lx (low-impedance) bus and that pull-up must be connected to the lower logic supply voltage. It must have a value that ensures sufficient base drive to the NPN transistor to keep it saturated. That requirement is easy to meet when the emitter is driven LOW by Lx of the buffer on the right hand side 3.3 V bus because the transistor will have its full specified gain, at least 75 for a general purpose transistor from the 2N2222 family. For good saturation use a design value of 20 for this gain. But when the collector side is driven LOW by an Lx of a bus on the left the transistor has only its 'inverse' gain and a suitable design value for that gain is around 10. That means the pull-up current in R3 must be $\frac{1}{10}$ the current in R4 when the bus is driven LOW. The emitter-base (or collector-base when driven in reverse) voltage will be around 0.7 V and the collector-emitter saturation voltage will be around 0.1 V in both cases.

The loading on the 5 V bus to be driven by the transistor with normal gain is R1 in parallel with R2. Neglecting the small offset of the bus LOW, the base current is (3.3 V − $V_{BE}$) / R3 and the load is (5 V / (R1 in parallel with R2)). For a gain of 20
(3.3 V − $V_{BE}$) / R3 = 5 V / 20 (R1 || R2).

$$R3 \leq \frac{20(R1 \parallel R2)}{5\ V} \times (3.3\ V - V_{BE}) \quad (4)$$

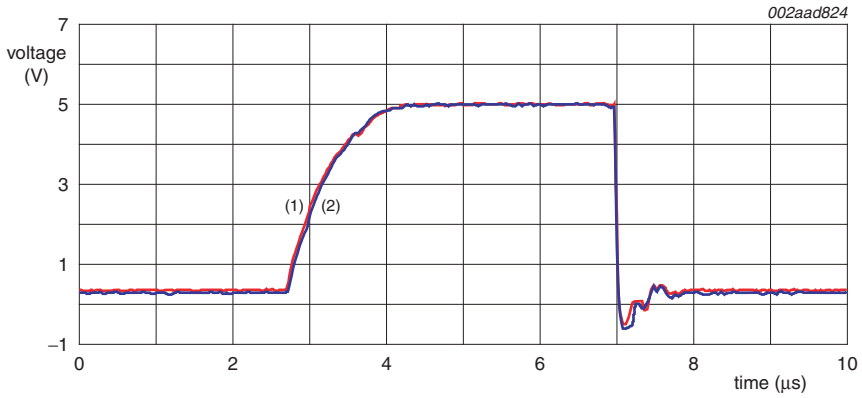
When the 5 V bus is driving the transistor collector, so the gain is 10, the requirement becomes:

$$R3 \leq \frac{10\ R4}{3.3\ V} \times (3.3\ V - V_{CE}) \quad (5)$$

R3 must be chosen equal to or less than the lower of those two requirements.

## 8. When is it allowed to work without any pull-up on the Sx side?

Figure 11 shows how a pull-up at Sx affects the rising edges in an application similar to Figure 5. When there is no Sx pull-up, the pull-up on the Lx or low-impedance bus must pull up the Sx side via the internal 30 Ω sense resistor. When it does that, there is a possibility the P82B715 could become active and for Lx to sink current to oppose the rise of the bus. Because the op-amp that senses the 30 Ω resistor must be designed with an input offset to guarantee the buffer is not active in the quiescent state with no current in the sense resistor, it always requires some minimum current to flow in the sense resistor before there is any buffer action. When the load capacitance on the Sx pin is very small, for example 20 pF, the charging current for that capacitor during the rising edges will remain small provided the bus rise time is also relatively slow. When the bus has a rise time of 1 μs the dV/dt on a 5 V bus has a maximum value, just as the bus starts to rise, of 5 V/μs. The charging current of a 20 pF capacitance at that rate causes a current of 100 μA and a voltage across the 30 Ω sense resistor of just 3 mV. In practice that will not exceed the offset of the chip, so the chip will remain inactive and the 20 pF loading at Sx simply appears as 20 pF loading on the bus at Lx. The sensing op-amp offset in the P82B715 is neither published nor guaranteed but it is relatively safe to assume it is not less than 10 mV. Whenever the bus rise time requirement is not a critical design factor and charging the capacitance at Sx will cause less than 300 μA, then a pull-up at Sx offers limited benefit. In Figure 11 the P82B715 is passively receiving the signal and the traces illustrate that a small capacitance at Sx will not activate it.

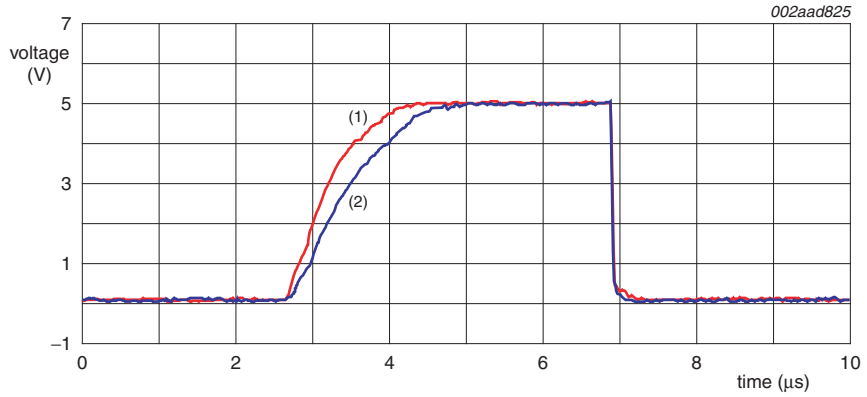



(1) 4.7 k pull-up at Sx.

(2) No pull-up at Sx.

**Fig 11. Passive P82B715 with/without Sx pull-up at the receive end of 20 m cable**

In Figure 11 the 4.7 kΩ pull-up has decreased the propagation delay on rising edge by less than 50 ns and increased the static offset by about 50 mV. (The theoretical increase in offset is about 30 mV. The rise time improvement is simply the effect of the additional 4.7 kΩ pull-up acting on the cable bus. The minimal offsets, fast fall time, and exaggerated overshoot result from driving the P82B715 Sx/Sy at the sending end from a pair of open-drain 74LVC gates to ensure identical drive signal conditions.)




Waveforms at Sx at sending end of 20 m cable.

(1) 4.7 k pull-up at Sx.

(2) No pull-up at Sx.

**Fig 12. Effect of 4.7 kΩ pull-up at Sx for an active P82B715 driver**

If the P82B715 has been active then a pull-up will improve turn-off because, just after P82B715 has been active to drive Lx, it will reverse the current and voltage across the sense resistor, increasing the turn-off input voltage to the op amp. Figure 12 shows the effect of the same 4.7 kΩ pull-up on the rise time of the P82B715 that is actively driving the cable.

In Figure 12 the 4.7 kΩ pull-up speeds up the P82B715 turn off. It has reduced the propagation delay (measured to $V_{CC}$ / 2) by about 200 ns and decreased the I²C-bus rise time by about 250 ns. The same 74LVC driver is used and gives the fast fall time and minimal offset.

## 9. Operating P82B715 on lower supply voltages

The P82B715 was originally specified for operation at 4.5 V or above. While its performance at higher supply voltages is typically maintained for $V_{CC}$ down to 3.3 V, the guaranteed performance is de-rated for supplies below 4.5 V. With supplies below 3.3 V the typical performance will also degrade, especially at very low temperatures. The specified 3.0 V should be regarded as the practical lower operating limit supply for this part.

Note the signal voltage levels at Sx/Lx are determined by the logic levels of the connected bus signals and not by $V_{CC}$.

When working with very low logic signals, which could be 1.5 V or at any level below $V_{CC}$, full performance when handling those small logic signals can be maintained by using a $V_{CC}$ supply above 3.3 V.

## 10. Solution for Fast-mode systems that prohibit P82B715's internal clamp diodes from its bus lines to $V_{CC}$

P82B715 has internal diodes from the bus lines to $V_{CC}$ that will the clamp the bus lines at about 0.7 V if $V_{CC}$ = 0 V. Fast-mode and later versions of the I²C-bus specification no longer allow these diodes to be used, so strictly P82B715 should be applied only in Standard-mode I²C-bus designs. Users have found P82B715 is capable of operation to 400 kHz and many simply accept the non-conforming clamp diodes because they provide a high degree of ruggedness and ESD immunity. It is also of little relevance in systems that use only a single supply.

In designs where compliance with this Fast-mode requirement is required, the P82B715 may be 'paired' with another buffer that provides this feature but still uses I²C-bus compliant switching levels. PCA9521 and PCA9522 are examples and Figure 13 shows how they may be used with P82B715s, allowing a system designer to combine the special features of each part.

The P82B715 provides the 30 mA cable drive level. Its minimal offsets make it compatible with all logic levels including TTL and buffers that use special offsets for their operation (e.g., Sx/Sy of P82B96). The PCA9521 likewise has minimal offsets, typical 60 mV sinking 3 mA, preserving that compatibility but it is an isolating buffer so the Sx/Sy loading is not passed to the I²C-bus connected at SDA/SCL. Its loading on that bus is just a few pF, and it frees its I/Os when $V_{CC}$ = 0 V. The $V_{IL}$ of PCA9521 is minimum 0.3$V_{CC}$ and therefore I²C-bus compliant. Above 33 % $V_{CC}$ its outputs are released so the I²C rise time on the bus at SDA/SCL is not affected by the cable loadings or its slower rise times. It can therefore easily meet the Fast-mode 300 ns requirement.

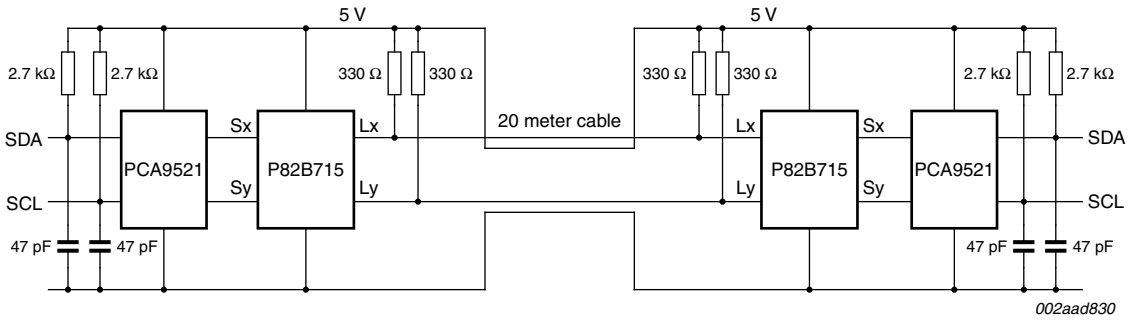
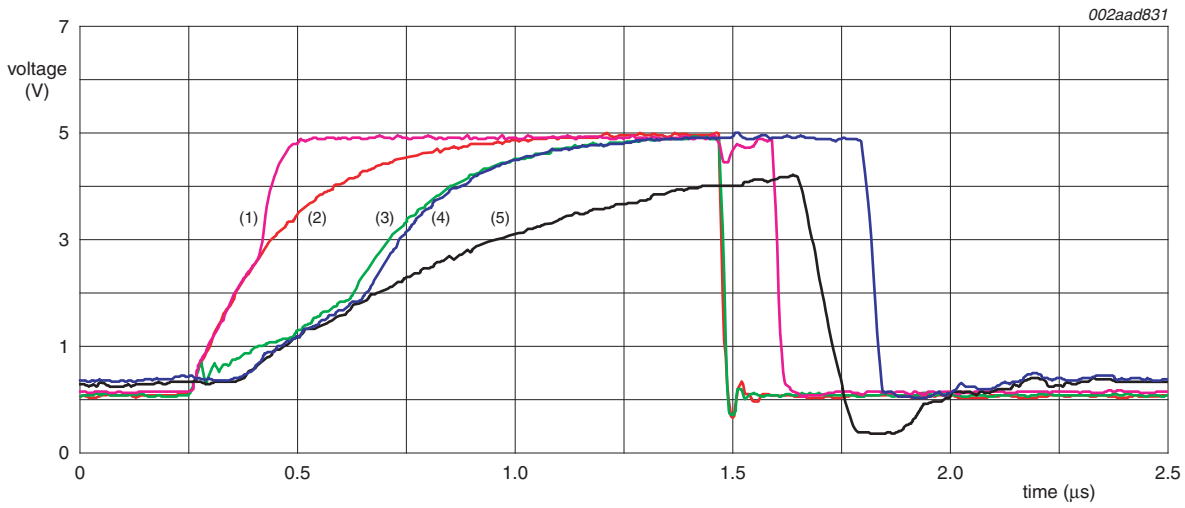



**Fig 13. P82B715 paired with PCA9521 provides bus release on $V_{CC}$ failure**

Figure 14 shows the SCL waveforms with a 20 m cable and clock speed about 400 kHz. The red trace shows how the drive signal into the PCA9521 at the sending end of the cable would look if there was a simple 1.5 kΩ pull-up at the PCA9521 output (e.g., Sx of the P82B715 was not connected). This represents our timing reference. The magenta trace shows the corresponding PCA9521 output. The release point of the PCA9521 output is at 33 % $V_{CC}$ (1.5 V) but the chip's propagation delay before actual release is about 100 ns, so the output follows the rising input up to about 3.7 V. That delay on the falling edge is clearer. With Sx connected to the PCA9521 output, the slow rise time of the cable load slows both the Sx and the drive signal as shown in the green trace. At the receiving end of the cable, the P82B715 Lx input has some ringing after the falling edge (black trace) and the I²C-bus rise time is about 570 ns. At the output of the PCA9521 (blue trace) the negative overshoot is removed and the I²C-bus rise time is now about 220 ns. Measured at $V_{CC}$ / 2 switching levels, the effective propagation delay due to the P82B715 and the 20 m cable is about 380 ns on the rising edge and about 350 ns on the falling edge. The total delay of an ACK, from a falling SCL to a rising SDA would be 730 ns. Working with Fm+ parts having a $t_{VD}$ of 450 ns maximum would allow guaranteed operation of this arrangement to at least 400 kHz. The total static offsets measured from either PCA9521 drive input to the corresponding far end output remain under 400 mV.




20 meter Cat5e cable.

(1) Magenta: PCA9521 driver output (for no Sx loading).

(2) Red: PCA9521 drive signal (for no Sx loading).

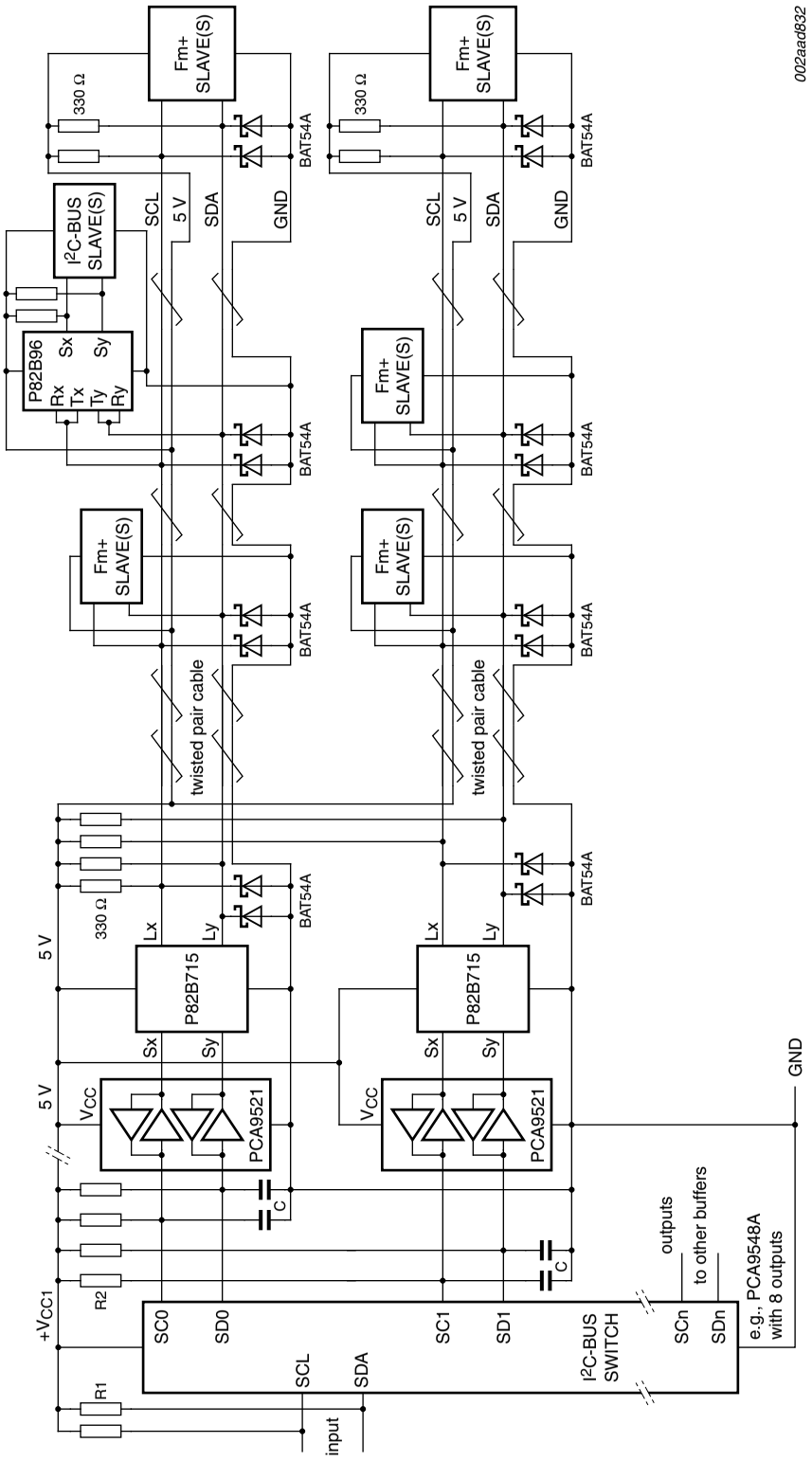
(3) Green: PCA9521 input when it has cable loading.

(4) Blue: PCA9521 receiver output.

(5) Black: Cable output to Lx.

**Fig 14. Traces from the arrangement in Figure 13**

## 11. P82B715 applied in very large I²C-bus signal distribution systems




Total system capacitance loading > 32,000 pF. (Also fully multi-master compliant; Fm+ masters also allowed at every slave position.)

**Fig 15. P82B715 driving twisted pair cables for a very large signal distribution system**

Figure 15 shows an example of a very large I²C-bus signal distribution system as used to control very large numbers of slave LED driver ICs in architectural lighting systems. The I²C-bus system is required to cover a very wide area and can require hundreds of meters of cable to be driven. Reusing the LED driver ICs will require bus switches to resolve the address conflicts but sometimes it is necessary to issue a 'GPIO All Call' command to control every slave at once. That requires that all the bus switch (PCA9548A) outputs are enabled at the same time. In turn that requires the device on the bus switch input to be able to drive all the 8 output buses in parallel. The large cable loading on each P82B715 means each Sx input will be a fully loaded 3 mA I²C-bus. Paralleling eight such buses could require an Sx I/O to drive at least 24 mA and it has only 3 mA capability. Even if a simple unbuffered Fm+ FET switch was available, and an Fm+ master used to drive the 24 mA load, that system would never allow selecting more than one switch output at any time when a slave response (ACK, data read, etc.) is required. Similarly P82B96 is precluded at the bus switch outputs because it is generally bad practice to parallel its Sx/Sy 3 mA I/Os.

Adding isolating buffers with I²C-bus compliant switching levels (PCA9521) places no restrictions on joining multiple buffer I/Os and reduces the loading on each bus switch output to just the buffer input capacitance (10 pF). The driver at the bus switch input can be any standard I²C-bus master. Further, when all outputs are selected together, the whole system could also be controlled by a master situated anywhere on any one of the 8 output buses.

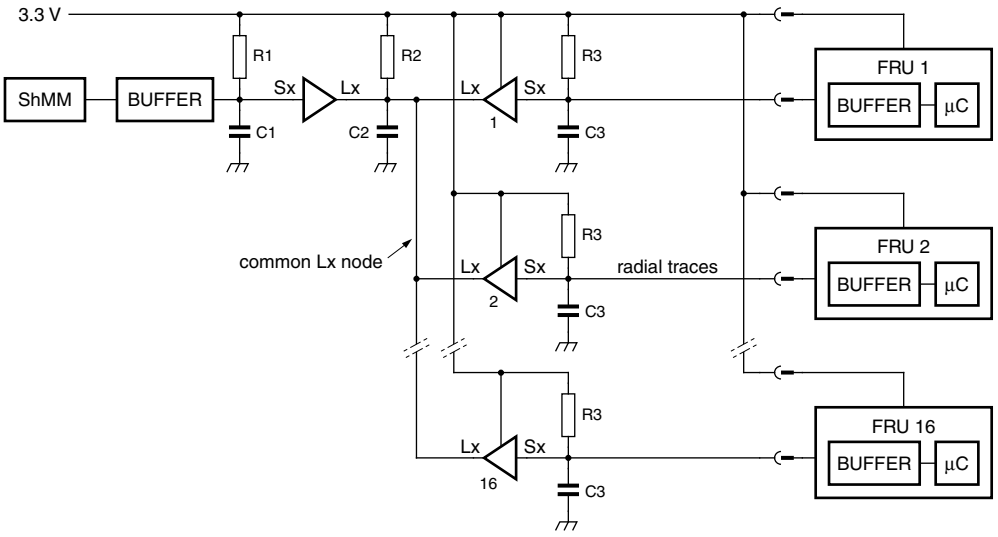
The pull-up resistors marked as R2 on each buffer input are only required to hold the buffer inputs HIGH when they are de-selected by the bus switch. A suitable value will be 100 kΩ to 470 kΩ so that, even when 8 outputs are selected, the contribution to the bus pull-up at the input is still greater than 12 kΩ. The total capacitance can be estimated as 10 pF per buffer, 3 pF per switch output, 20 pF for the switch input plus allowance for tracks. 20 pF per switch output should provide a conservative estimate, so just 160 pF for 8 branches. Each PCA9521output can drive at least 400 pF per branch, so when directly interfaced to P82B715 the Lx/Ly side of P82B715 can drive at least 4000 pF. With 8 branches, that allows 32 nF total system loading. With Cat5 twisted pair cable at 50 pF/m, that supports hundreds of metres of cabling. In practice, with the 5 V logic levels as shown, it is probably wise to restrict each branch to around 30 m but that still allows a system with more than 240 m of cabling.

330 Ω resistors, fitted at the two extreme ends of the cable, combine to provide the lowest allowed pull-up for 5 V and, together with the controlled slew of P82B715, control overshoot and ringing on the cable. The faster drivers such as P82B96 and PCA9600, and even the Fm+ parts, will cause some ringing and overshoot so it is always a good design rule to include the Schottky diode clamps at every node as shown.

Because the bus switch uses common gate FET amplifiers, a configuration selected for highest frequency RF amplifiers, it may be found necessary to add small capacitors (C) to avoid irregularities on rising bus edges. A suitable value will be around 33 pF to 100 pF depending on the number of FET switch outputs. Resistors R1 are chosen to provide the required rise time when **all** switch outputs are selected. The 8-output switch and buffers will contribute less than 160 pF and the total including capacitors (C) should be kept below the I²C-bus allowed 400 pF maximum.

I²C rise time = 0.85 × R × bus capacitance (R in ohms, Capacitance in Farads). Using the minimum R = (Bus supply / 3 mA) provides the fastest rise time.

## 12. Application in AdvancedTCA, in Radial IPMB signal distribution




Calculations to ensure rise time is met on each bus section:

| effective capacitance at ShMM buffer | | effective capacitance at common Lx node | | effective capacitance at average radial trace | |
|---|---|---|---|---|---|
| ShMM buffer | 10 pF | 17 × P82B715 | 170 pF | 1 × FRU | 25 pF |
| strays | 20 pF | trace capacitance | 30 pF | radial trace/connector | 125 pF |
| P82B715 | 10 pF | | | P82B715 | 10 pF |
| total capacitance C1 | 40 pF | total capacitance C2 | 200 pF | total capacitance C3 | 160 pF |

ShMM buffer pull-up

$$R1 = \frac{1\ \mu s}{40\ pF} = 25\ k\Omega$$

Lx common pull-up

$$R2 = \frac{1\ \mu s}{200\ pF} = 5\ k\Omega$$

radial trace pull-up

$$R3 = \frac{1\ \mu s}{160\ pF} = 6.2\ k\Omega$$

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Calculation of static loading at ShMM buffer and each FRU:

Loading on ShMM buffer = R1 || {10 (R2 || R3/16)} = 3.5 kΩ

Loading on each FRU = R3 || {10 (R1 || R2 || R3/15)} = 3.76 kΩ

**Fig 16. Typical arrangement and calculation for an IPMB analog radial shelf**

Figure 16 shows P82B715 in an analog Radial IPMB shelf application.

In this example the total system capacitance is 2800 pF but it is distributed over 18 different bus sections and no section has a capacitance greater than 200 pF. If every individual bus section is designed to rise at least as fast as the IPMB requirement then when any driver releases the bus all bus sections will rise together and no amplifiers in the P82B715s will be activated or, if one is activated, it can only slow the system bus rise to its own rate and that has been designed to meet the requirement. It is then only necessary to calculate the equivalent static bus pull-up loading and to ensure that it exceeds the specification requirement. The calculated loadings meet the requirements.

Note that in this example only one of the four IPMB lines is shown and the usual switching arrangements for isolating or cross-connecting bus lines are not shown. The typical offset (increase in the bus low level) measured between any two Sx points in this system is below 100 mV.

# 13. Short summary of characteristics and comparison with an 'isolating' buffer

**Table 1. Summary and comparison**

| Short summary of features | P82B715 | | P82B96 | |
|---|---|---|---|---|
| | Sx side | Lx side | Sx side | Tx/Rx side |
| **I/O switching level characteristics** | | | | |
| Input logic LOW switching level (min.) | n/a | n/a | 0.6 V | $0.42V_{CC}$ |
| Input logic LOW switching level (max.) | n/a | n/a | 0.7 V | $0.58V_{CC}$ |
| Compatible with I²C-bus logic levels | yes | n/a | yes | yes |
| Compatible with TTL logic levels | yes | n/a | typ. | yes |
| Output level can meet I²C-bus noise margins | yes[1] | n/a | $V_{CC}$ > 3.5 V | yes |
| Allowed to parallel several of these I/Os | yes | yes | no | yes |
| I/O sources current (> 10 μA I²C-bus spec.) | yes | yes | no | no |
| Drive has component due load on other I/O | yes | yes | no | no |
| **Drive** | | | | |
| Standard 3 mA sink capability | yes | n/a[2] | yes | yes |
| Enhanced 30 mA sink capability | no | yes | no | yes |
| Output suitable for driving long cables | no | yes | no | yes |
| **Other** | | | | |
| Logic level shifting capability | no | no | yes | yes |
| Connected bus voltage may exceed $V_{CC}$ | no | no | yes | yes |
| Noise on this I/O copied to other I/O | yes | yes | no | no |
| I²C-bus compliant noise margin on this I/O | yes | yes | no | yes |
| I²C-bus to/from unidirectional components | no | no | no | yes |
| Input (Rx) logic levels are I²C-bus compliant | | | | yes |
| Output (Tx) drive is I²C-bus compliant | | | | yes |
| Data suggests maximum bus speed | 100 kHz | 100 kHz | 400 kHz | 400 kHz |
| Approximate propagation delay, this input to output | (250 ns)[3] | 0 ns | 70 ns | 200 ns |
| Can be useful to at least this bus speed | 400 kHz | 400 kHz | 700 kHz | 700 kHz |

[1] Output level is related to the input level at Lx. It will not exceed the voltage at Lx by more than 0.1 V. If the input Lx level is designed to be below ($0.25V_{CC}$ – 0.1 V) then the Sx output will be I²C-bus compliant.

[2] Output may be used for any current up to a maximum static sink of 30 mA but there would be no advantage when using this output to sink 3 mA

[3] If measured conventionally, as the voltage delay input to output, the P82B715 will appear to have zero propagation delay in either direction. When active (Sx driving the LOW) it may cause a delay to both its input driving signal at Sx and its output at Lx as indicated by the figure in brackets. This is the delay in its current gain.

# 14. Appendix 1: Techniques for buffering I²C-bus signals (or, building a bidirectional bus buffer that does not simply latch at the first LOW)

The challenge in I²C-bus systems is to build a 'buffer' that can handle simultaneous bidirectional data flow without latching. It is easiest to illustrate the problem with an example, see Figure 17.

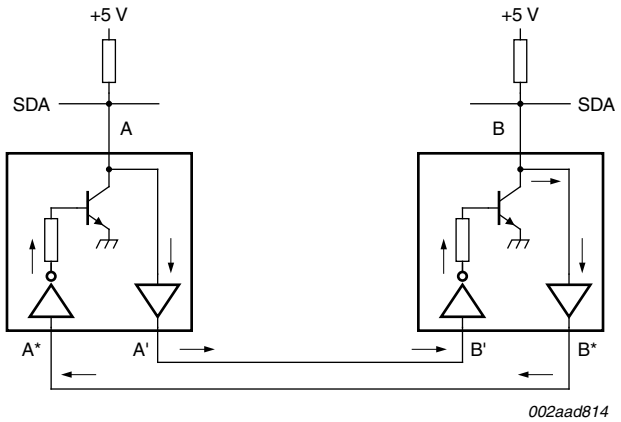


**Fig 17. Using conventional buffers with bidirectional I²C-bus signals just causes latching**

On the left side of Figure 17 part of an intended 'buffer' device is attached to the SDA wire of an I²C-bus at A. On the right, an equal arrangement is connected to the SDA wire of a second I²C-bus at B. The objective is to be able to reproduce the I²C-bus A signals on the second bus B, and also to be able to reproduce the I²C-bus signals from bus B back onto bus A. Figure 17 shows a conventional attempt to do this, using simple (uni-directional) open-collector logic buffers. The I²C-bus specifications do not allow the bus to be driven towards the 'HIGH' level, so only open-collector or open-drain buffer outputs may be connected to an I²C-bus. They are able to pull each I²C-bus LOW and it is pulled HIGH only in the normal way, by the passive pull-up resistors.

Here is what actually happens in the arrangement as shown. When I²C-bus line A is driven LOW by an I²C device connected to the bus, then that bus logic LOW signal appears at the input of a conventional buffer. It has a high input impedance and generates a logic LOW output on a new and different bus at A'. This is connected to the input of an inverter and open-collector transistor arrangement, equivalent to an open-drain, non-inverting buffer, between B' and bus B. The LOW input at B' will then drive the SDA line at B to LOW as required. Because the transfer of data must be bidirectional, the arrangement must be symmetrical. There must also be a buffer connected to bus B sensing that SDA bus. It will output a LOW at B*. That is connected back to the left side as a logic LOW input at A*. That input LOW means the inverter and open-collector transistor, equivalent to an open-drain, non-inverting, buffer connected to bus A, will also drive the I²C-bus A LOW. When the device that originally pulled bus A LOW releases that SDA line at A the buffer just holds that line LOW. The arrangement is essentially a latch configuration and once it is set LOW there is no mechanism to reset it HIGH again. Buffering of this type can only be used if the potential latching loop inside the buffering arrangement can be broken in some way. Different techniques to prevent latching may be

used but there is always some system performance compromise involved. The objective is to find techniques that avoid latching but minimize the consequences of their compromise on the system.

Another important point to note is that, within the constraints of simple binary logic, with just one HIGH and one LOW level, there is no way to build a buffer device that is truly bidirectional. It is simple to build a buffer than can be switched so that it can pass signals in each of two directions—but not in those two directions at the same time. Because the 'building blocks' for an I²C-bus buffer will be uni-directional, the challenge is to find ways to split the bidirectional I²C-bus signals into uni-directional data streams and recombine them again. Most of the solutions make use of analog techniques and one introduces an additional logic switching level and uses that to determine the origin of the signal that is driving the bus LOW. For example, if the buffer between A and A' is specially designed so that its input logic switching level is always slightly lower than the open-collector buffer's output logic LOW then when the open-collector buffer is driving the I²C-bus LOW at A then that LOW will not be recognized by the buffer sensing the I²C-bus at A and A' will not be driven LOW. The buffer output LOW at A can be designed to be, say 0.7 V by adding a series diode, and then the buffer's input switching level is set below that, say at 0.6 V. I²C-bus devices connected at A are guaranteed to recognize any voltage less than $0.3V_{CC}$ as being LOW, so the 0.7 V covers devices with $V_{CC}$ down to 2.3 V. The buffer's input can also be 'compatible' with I²C-bus driving devices connected at A because they must pull their outputs below 0.4 V. The buffer's output LOW can be I²C-bus 'compliant', because the requirement is $0.3V_{DD}$ or less. This compromise on logic levels therefore provides one solution to the latching problem. P82B715 does not attempt to 'buffer' or isolate the two buses A and B in that way. It provides a fully compliant bus interface to bus A but it is designed to interface on its other side with a bus that operates with a sink current that is 10 times greater than a normal I²C bus. The P82B715 is therefore not a symmetrical device. It has very different characteristics for signals passing in each direction. If bus A is connected to the Sx I/O and bus B is connected to the Lx I/O then it behaves as follows: It has an internal resistor, about 30 Ω, fitted between Sx and Lx. Clearly there cannot be any isolation between its I/Os! It senses the current in that resistor and when current flows from Lx to Sx (and out Sx to a driving I²C-bus device) it sinks a current to ground that is 9 times the sensed Lx-Sx current. This enables it to operate with a pull-up on Lx that could be 10 times smaller than the pull-up on a standard 3 mA I²C-bus. The lower impedance bus at Lx allows 10 times higher capacitance for a given bus rise time. Standard-mode I²C-bus devices cannot be connected to the low-impedance bus at B; a second P82B715 must be used to interface back to Standard-mode 3 mA I²C-bus levels. The I²C-bus specification (*UM10204, "I²C-bus specification and user manual"*) has added a 30 mA Fast-mode Plus bus that is a faster variant of the bus at Lx.

When the bus at Lx is pulled LOW by another device, the bus at Sx is pulled LOW via the internal 30 Ω resistor. There is no activation of the P82B715; it has the transfer characteristics of a passive 30 Ω resistor. If there is any pull-up on the bus A at Sx then it simply appears as additional loading in parallel with the pull-up on the bus at Lx, so its current must be included when designing for a maximum of 30 mA sink current on the low-impedance bus.

# 15. Abbreviations

**Table 2. Abbreviations**

| Acronym | Description |
|---|---|
| AdvancedTCA | Advanced Telecom Computing Architecture |
| DC | Direct Current |
| EMI | ElectroMagnetic Interference |
| ESD | ElectroStatic Discharge |
| FET | Field-Effect Transistor |
| FRU | Field Replaceable Unit |
| I/O | Input/Output |
| I2C-bus | Inter-Integrated Circuit bus |
| IC | Integrated Circuit |
| IPMB | Intelligent Platform Management Bus |
| LED | Light-Emitting Diode |
| PCB | Printed-Circuit Board |
| PMBus | Power Management Bus |
| RC | Resistor-Capacitor network |
| RF | Radio Frequency |
| ShMM | Shelf Management Module |
| SMBus | System Management Bus |
| TTL | Transistor-Transistor Logic |

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