AN11203

NTAG 5 - Use of PWM, GPIO and event detection

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530212 COMPANY PUBLIC

Document information

Information	Content
Keywords	GPIO, PWM, event detection, NTAG 5 switch, NTAG 5 link, NTAG 5 boost, ISO/IEC 15693, NFC Forum Type 5 Tag
Abstract	Guidelines for designing applications using general-purpose input/output, pulse width modulation and event detection capabilities.

Revision history

Rev	Date	Description
1.2	20200109	First official released version
1.1	20190923	Section 2 updated
1.0	20190917	Initial version

1 Abbreviations

Table 1. Abbreviations

Acronym	Description
~	Weak approximation (mathematical)
ALM	Active Load Modulation
ED	Event Detection
GPIO	General Purpose Input/Output
IC	Integrated Circuit
I^2C	Inter-Integrated Circuit
MCU	Microcontroller Unit
POR	Power On Reset
PLM	Passive Load Modulation
PWM	Pulse Width Modulation
VCD	Vicinity Coupling Device
VICC	Vicinity Integrated Circuit Card

2 Introduction

This document describes GPIO and PWM capabilities of NTAG 5 family ICs. The NTAG 5 provides the capability to harvest energy from the RF field, to use pins as GPIOs or to use them as PWM output channels. On top, event detection pin can be configured to notify peripheral devices on many RF events. This document focuses on showing, how to configure the IC for different use cases.

Important note 1: For GPIO, PWM functionalities, V_{CC} supply is mandatory. If functionality is configured but not working, status register A0h can be checked for VCC_SUPPLY_OK and VCC_BOOT_OK bits if set to 1b.

Important note 2: The Event Detection (ED) pin functionality is operated via the RF field power, the NTAG 5 VCC supply is not required. Only for pulse width modulation use case on ED pin, V_{CC} is a must.

In case of energy harvesting mode, note that signal on GPIO pins is available about 3 ms after NFC field is applied. For more details on energy harvesting, see [Application Note].

2.1 Potential applications

- Control PWM duty cycle, frequency over NFC, without an MCU
- Calibrate devices automatically without an MCU
- Verify the authenticity of the device through the value chain
- Calibrate the reference current without an MCU, or control and dim LEDs
- Use a cloud connection to enable new features, or power and configure a motor or LED

2.2 Configuration registers

After POR the configuration registers data available in EEPROM will be loaded into session registers.

2.3 Session registers

In the current session, the ICs behavior can be monitored and configured by writing into session registers. Access to session registers may be password protected.

2.4 Weak pull-up/pull-down

NTAG 5 IC has possibility to configure IO pins in the way to avoid floating state of the pin. NTAG 5 IC has a built-in a high value resistor, which can be enabled/disabled. Weak pull-up/pull-down means high value resistance, consequently less current flows.

Output driver of the cell is the push-pull kind of structure. Pull-up driver is created by PMOS and pull-down driver is created by NMOS. Receiver with (50 ns) spike filter. In case of external IO driver, in order to save power, disable the weak pull-up/down.

Low-pass filter (LPF) is implemented to cope with bouncing effects.

3 GPIO functionality

NTAG 5 may serve as a simple GPIO device, instead of need of external devices, e.g., MCU. There are two (2) pins that can be configured for GPIO purposes. These pins are also multiplexed with PWM functionality so both functionalities cannot exist at the same time - **PWM and GPIO features** on the same pin **cannot be combined**.

Configuration of GPIO functionality is located in user configuration memory [CONFIG_2 → address 37h]. Access to this memory area is only possible with READ_CONFIG and WRITE_CONFIG commands from RF perspective and normal read and write commands from I^2C perspective, but I^2C interface is not available if pins are used as GPIOs.

The pins can be configured either as:

- Input mode: the status of the pad is available in one of the session register bits [GPIO1_PAD_OUT_STATUS, GPIO0_PAD_OUT_STATUS, GPIO1_PAD_IN_STATUS, GPIO0_PAD_IN_STATUS]
- Output mode

After POR, then the pads are configured accordingly as per the configuration bits. During ongoing session, the update to GPIO configuration registers takes immediate effect.

At POR, the GPIO is set to High-Impedance state. Also the receiver mode of the pad is disabled. After NTAG 5 comes out of reset and reads configuration, the pad selection pins are controlled to behave as per the configuration.

GPIO can be configured by setting below properties:

- Input
  - Disabled (High-impedance in GPIO / I^2C mode)
  - Plain input with weak pull-up
  - Plain input (floating)
  - Plain input with weak pull-down
- Output
  - High
  - Low
- Slew rate

3.1 GPIO Registers location

Table 2. PWM and GPIO Configuration Location (PWM_GPIO_CONFIG)

Block Address		Byte 0	Byte 1	Byte 2	Byte 3
NFC	I^2C				
39h	1039h	PWM_GPIO_CONFIG_0	PWM_GPIO_CONFIG_1	RFU	

Table 3. PWM and GPIO Configuration Definition (PWM_GPIO_CONFIG_0)

Bit	Name	Value	Description
7	SDA_GPIO1_OUT_STATUS	0b	Output status on pad is LOW (default)
		1b	Output status on pad is HIGH

Bit	Name	Value	Description
6	SCL_GPIO0_OUT_STATUS	0b	Output status on pad is LOW (default)
		1b	Output status on pad is HIGH
5 to 4	RFU	00b	
3	SDA_GPIO1	0b	Output (Default)
		1b	Input
2	SCL_GPIO0	0b	Output (Default)
		1b	Input
1	SDA_GPIO1_PWM1	0b	GPIO (Default)
		1b	PWM
0	SCL_GPIO0_PWM0	0b	GPIO (Default)
		1b	PWM

Table 4. PWM and GPIO Configuration Definition (PWM_GPIO_CONFIG_1 and PWM_GPIO_CONFIG_1_REG)

Bit	Name	Value	Description
7	PWM1_PRESCALE	00b	Pre-scalar configuration for PWM1 channel (default 00b)
6			
5	PWM0_PRESCALE	00b	Pre-scalar configuration for PWM0 channel (default 00b)
4			
3	PWM1_RESOLUTION_CONF	00b	6-bit resolution (default)
		01b	8-bit resolution
2		10b	10-bit resolution
		11b	12-bit resolution
1	PWM0_RESOLUTION_CONF	00b	6-bit resolution (default)
		01b	8-bit resolution
0		10b	10-bit resolution
		11b	12-bit resolution

3.2 GPIO as Output

Each line can be configured independently from each other - e.g. one as GPIO Input, the other as GPIO Output.

Selection of GPIO (or PWM) depends on GPIO0_PWM0 and GPIO1_PWM1 configuration bits:

- **GPIO0_PWM0** = 0b pad configured for GPIO (GPIO0_PWM0 = 1b pad configured for PWM)
- **GPIO1_PWM1** = 0b pad configured for GPIO (GPIO1_PWM1 = 1b pad configured for PWM)

3.2.1 Example 1: GPIO0 as output, GPIO1 as output

3.2.1.1 Description

In this example, both GPIO pads are used as Outputs. Both pads will be set to 1b (HIGH), with effect that LED1 will be turned off, LED2 will be turned on.

3.2.1.2 Schematics

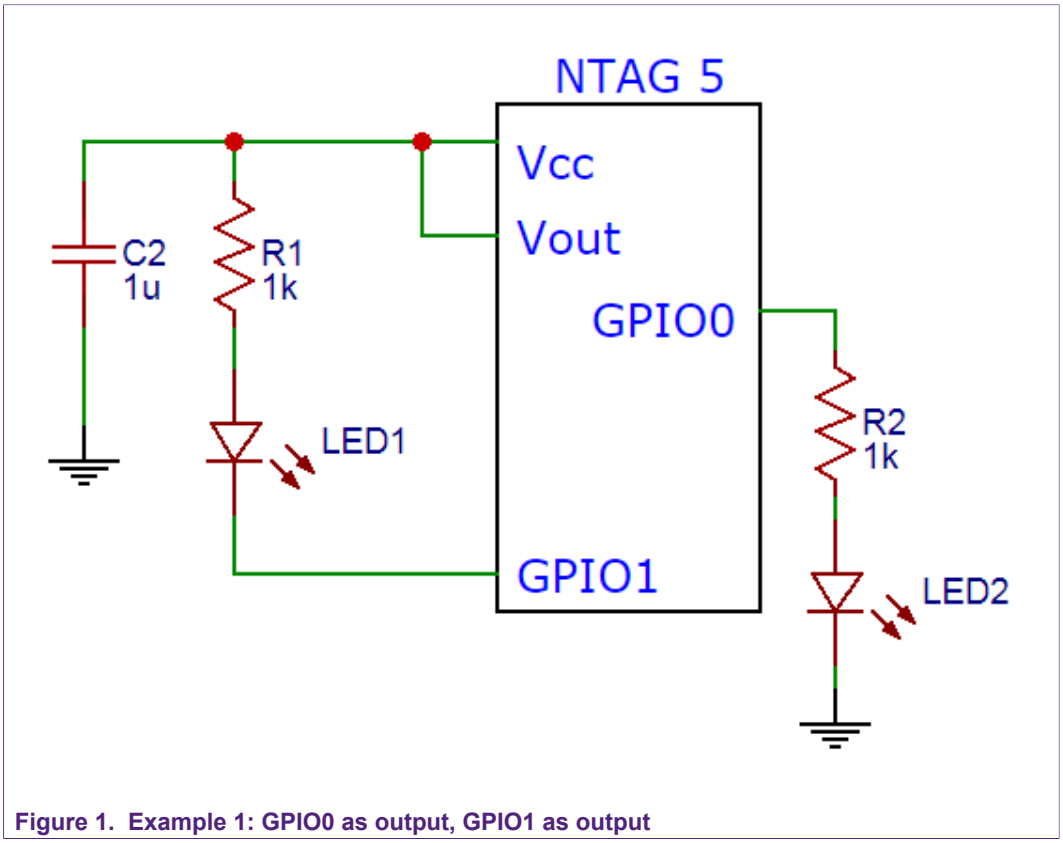

Figure 1. Example 1: GPIO0 as output, GPIO1 as output

3.2.1.3 Configuration bytes

Table 5. PWM and GPIO Configuration bytes Location (PWM_GPIO_CONFIG_REG)

Block Address		Byte 0	Byte 1	Byte 2	Byte 3
NFC					
A3h		C0	00	RFU	

3.2.1.4 RF command set

Response format as from Table 7 is expected on reader side, meaning the Tag responds with ACK. This response is expected in all Examples within this document if not written differently.

Table 6. RF Command: VCD to VICC

Flags	Command code	IC manuf. code	Block Address	Byte 0	Byte 1	Byte 2	Byte 3	CRC 0	CRC 1
02	C1	04	39	C0	00	00	00	12	F8

Table 7. RF Response: VICC to VCD - ACK

Flags	CRC 0	CRC 1
00	78	F0

3.2.1.5 Result

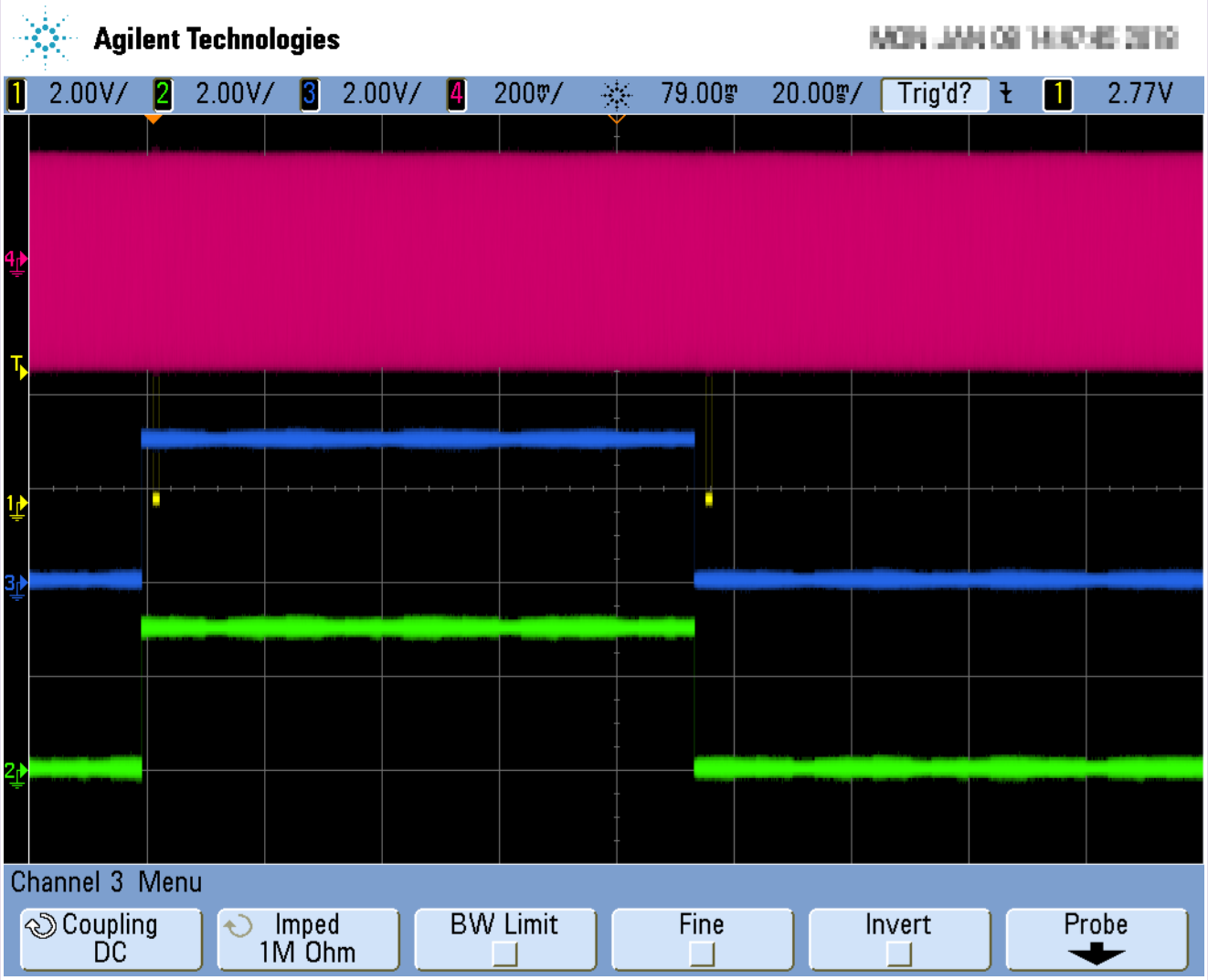

Figure 2. GPIOs set

3.3 GPIO as Input

GPIO Input logic HIGH is considered as V_{IL} > 1.62 V.

Status of GPIOs can be monitored in STATUS_REG:

- Address: A0h, Byte 0 and Byte1
  - Bit11: GPIO0_IN_STATUS:
    - 0b: GPIO0 input is LOW
    - 1b: GPIO0 input is HIGH
  - Bit12: GPIO1_IN_STATUS:
    - 0b: GPIO1 input is LOW
    - 1b: GPIO1 input is HIGH

3.3.1 Example 2: GPIO0 as INPUT

3.3.1.1 Description

In this example one of the GPIO pads - GPIO0 is used as Input. Status of (mechanical) switch, will be read out via RF interface. Capacitor value depends on final application.

GPIO0 pad will be configured as:

- GPIO0_SLEW_RATE: 1b - High-Speed GPIO
- GPIO0_IN: 01b - Plain input with weak pull-up
- GPIO0_PWM0: 0b - GPIO (Default)
- GPIO0: 1b - Input
- GPIO0_IN_STATUS: 1b - Enable input status, that will be reflected in Session register - STATUS_REG, A0h.

3.3.1.2 Schematics

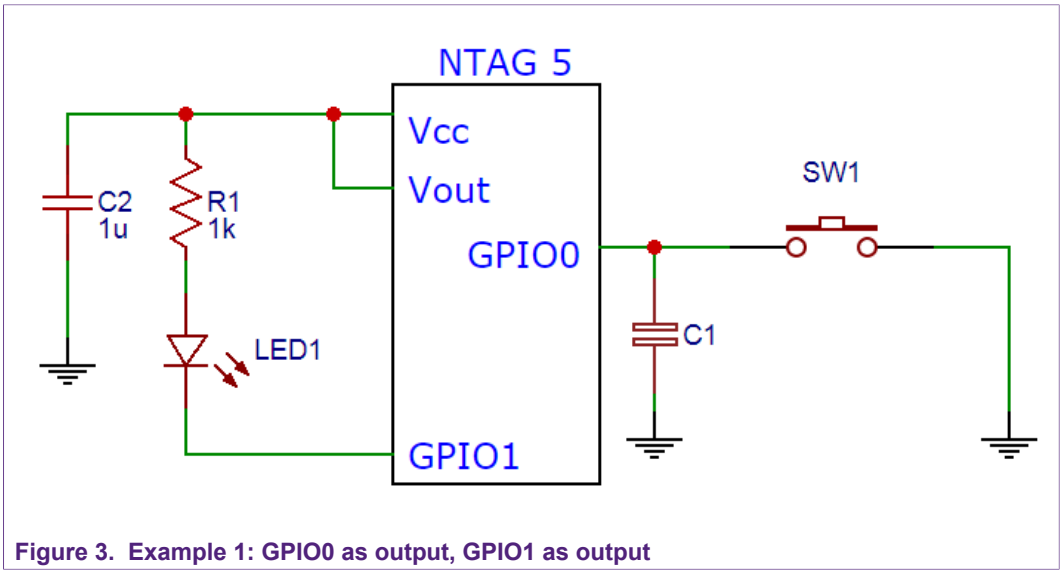

Figure 3. Example 1: GPIO0 as output, GPIO1 as output

3.3.1.3 Configuration bytes

Table 8. Configuration Bytes Location (CONFIG)

Block Address		Byte 0	Byte 1	Byte 2	Byte 3
NFC					
37h		XX	2X	1X	00

Table 9. PWM and GPIO Configuration Bytes Location (PWM_GPIO_CONFIG)

Block Address		Byte 0	Byte 1	Byte 2	Byte 3
NFC					
39h		14	00	00	00

3.3.1.4 RF command set

Write to Configuration registers to configure:

Table 10. RF Command: VCD to VICC

Flags	Command code	IC manuf. code	Block Address	Byte 0	Byte 1	Byte 2	Byte 3	CRC 0	CRC 1
02	C1	04	37	00	20	1F	00	11	B7
02	C1	04	39	14	00	00	00	86	72

Read out GPIO0_INPUT_STATUS - Input pulled-high internally by "weak pull-up". Button **not pressed**:

Table 11. RF Command: VCD to VICC

Flags	Command code	IC manuf. code	Command code	Block Address	CRC 0	CRC 1
02	C0	04	A0	00	83	45

Table 12. RF Response: VICC to VCD

Flags	Byte 0	Byte 1	Byte 2	Byte 3	CRC 0	CRC 1
00	03	C**C**	00	00	41	83

Meaning:

Byte 1 = CCh -> Bit 3 is GPIO0_IN_STATUS = 1b (GPIO0 input is HIGH).

Read out GPIO0_IN_STATUS - Input pulled to GND (button **pressed**):

Table 13. RF Response: VICC to VCD

Flags	Byte 0	Byte 1	Byte 2	Byte 3	CRC 0	CRC 1
00	03	C**4**	00	00	41	83

Byte 1 = C4h -> Bit 3 is GPIO0_IN_STATUS = 0b (GPIO0 input is LOW).

4 PWM functionality

The PWM output signal behavior can be configured independently with the help of configuration register. After configuration of PWM parameters and following POR, PWM will be available on pads as soon as V_{CC} will be applied.

Selection of PWM (or GPIO) depends on GPIO0_PWM0 and GIPO1_PWM1 configuration bits.

- USE_CASE_CONF [1:0] =10b
- GPIO0_PWM0 = 1b pad configured for PWM
- GPIO1_PWM1 = 1b pad configured for PWM

The ON time: PWM0_ON [11:0] or PWM1_ON [11:0]: Will be the time the PWM output will be asserted HIGH.

The OFF time: PWM0_OFF [11:0] or PWM1_OFF [11:0]: Will be the time when the PWM output will be de-asserted LOW.

By controlling the ON and OFF, phase shift becomes completely programmable. The resolution for the phase shift is $1/$PWM_RESOLUTION_CONF of the input frequency.

If PWM_RESOLUTION_CONF is 12 bit, then the PWM timer is 12 bit and PWM_ON and OFF registers will be of 12-bit resolution.

If PWM_RESOLUTION_CONF is 10 bit, then the PWM timer is 10 bit and PWM_ON and OFF registers will be of 10-bit resolution.

The same applies for 8-bit and 6-bit resolution.

The internal PWM input clock frequency is **1.69 MHz**.

4.1 PWM Registers location

Registers PWM_GPIO_CONFIG define the PWM/GPIO functionality. PWM-related registers can be found in Section 3.1.

4.2 PWM values calculation

Frequency

Frequency is defined by pre-scalar and resolution. Table of possible frequencies can be found in [datasheet].

Resolution

Defines the maximum number of pulses that can be available in the given PWM period, which depends on input clock frequency. Each PWM pin has its own configurable resolution.

12-bit resolution max. value 2^{12}= 4096

10-bit resolution max. value 2^{12}= 1024

8-bit resolution max. value 2^{12}= 256

6-bit resolution max. value 2^{12}= 64

Start time - PWMx_ON

The value (in HEX) to be set in registers, is calculated from desired period percentage. Therefore it depends on Frequency, Resolution. Calculated decimal values shall be rounded to nearest integer. PWM_ON value denotes the timing + 1.

$$Start\ \ time\ \ =\ \ 2^{Resolution} \times Percentage$$

Table 14. Examples of few Resolution vs. Start Time percentage values - PWMx_ON calculation

Percentag [%]	100		50		35		20		10	
Resolutio [bit]	[d]	[HEX]	[d]	[HEX]	[d]	[HEX]	[d]	[HEX]	[d]	[HEX]
12	4096	0FFF	2048	07FF	1434	0599	819	0332	410	0199
10	1023	03FF	512	01FF	358	0165	205	00CC	102	0065
8	256	00FF	128	007F	90	0059	51	0032	26	0019
6	64	003F	32	001F	22	0015	13	000C	6	0005

PWM Duty Cycle - PWMx_OFF

The value (in HEX) to be set in registers is calculated from desired period percentage. Therefore it depends on Frequency, Resolution, PWMx_ON. Calculated decimal values shall be rounded to nearest integer. PWM_OFF value denotes the timing + 1. PWM_ON shall be summarized to PWM_OFF value.

4.3 Example 3: PWM0 and PWM1 as PWM Output

4.3.1 Description

In this example, both GPIO/PWM pads are used as PWM Outputs.

PWM0 pad

- resolution (PWM0_RESOLUTION_CONF): 6bit
- start time (PWM0_ON): 0 %
- PWM duty cycle (PWM0_OFF): 30 %

PWM1 pad

- resolution (PWM0_RESOLUTION_CONF): 6bit
- start time (PWM0_ON): 10 %
- PWM duty cycle (PWM0_OFF): 40 %

4.3.2 Registers values

Table 15. PWM and GPIO Configuration Bytes Location (PWM_GPIO_CONFIG)

Block Address		Byte 0	Byte 1	Byte 2	Byte 3
NFC	I^2C				
39h	1039h	03	00	RFU	

Table 16. (PWM0_ON, PWM0_OFF, PWM1_ON, PWM1_OFF)

Block Address		Byte 0	Byte 1	Byte 2	Byte 3
NFC	I^2C				
3Ah	103Ah	00h	00h	13h	00h
3Ah	103Bh	06h	00h	1Fh	00h

4.3.3 RF command set

Table 17. RF Command: VCD to VICC

Flags	Command code	IC manuf. code	Block Address	Byte 0	Byte 1	Byte 2	Byte 3	CRC 0	CRC 1
02	C1	04	37	00	20	0F	00	80	22
02	C1	04	39	03	00	00	00	06	E6
02	C1	04	3A	00	00	13	00	FE	61
02	C1	04	3B	06	00	1F	00	80	88

4.3.4 Result

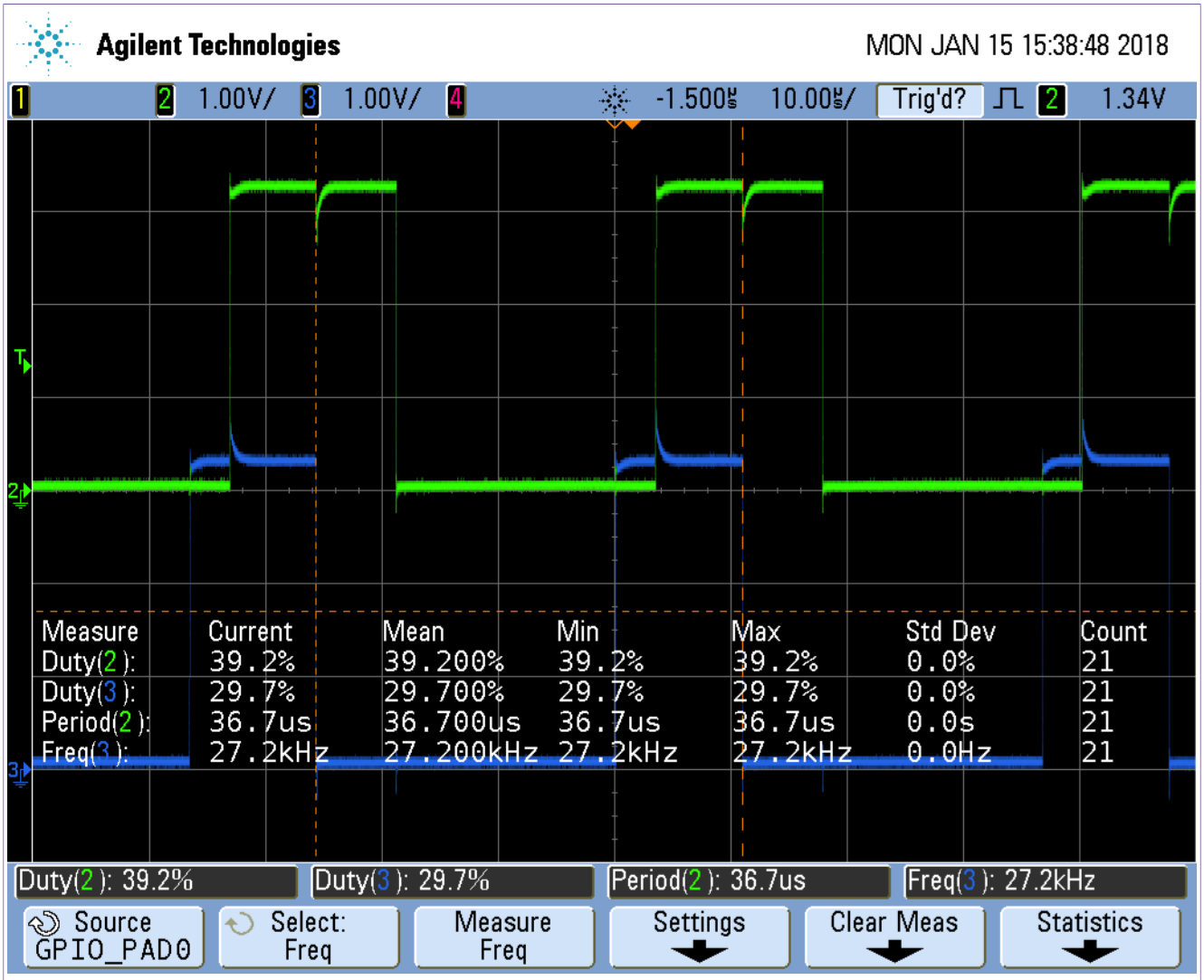

Figure 4. PWM Example 3: 6-bit resolution, PWM0 and PWM1 enabled as PWM Output

5 Event detection functionality

GPIO pins have push-pull architecture, **ED pin** is an **open-drain**, active low implementation. External pull-up resistor is required. This way, by default ED remains HIGH (Inactive) until one of the event detection conditions is *true*.

There are several events for ED pin to be triggered, depending on IC type. See data sheet [1] or [2] or [3] for more info.

- ED = ON means that external ED signal is pulled LOW
- ED = OFF means that external ED signal is released and HIGH

ED behavior can be controlled in two ways:

- ED can be configured to show the events inside the tag or
- ED pin can be released by writing to clear register for the specific events

ED pin characteristics V_{OL} LOW-level output voltage, I_{OL} = 3 mA @ 0.4 V. I_{IED} leakage current = 0.3 mA to 10 mA, V_{IN} = 0 V to 5.5 V.

NOTE: Measurements are done in following conditions:

- RF
  - 1 out of 4 data coding
  - uplink/downlink data rate of 26.48 kbits/s (f_c/512)
- I^2C data rate 400 kHz

5.1 Example 4 - NFC Field Detect

5.1.1 Description

ED pin can indicate presence of the NFC field - 13.56 MHz carrier frequency. Can be used in PLM and ALM modes.

ED=ON if field is switched ON.

ED=OFF if field is switched OFF.

5.1.2 Register values

ED_CONFIG(_REG) = 0001b

5.1.3 Results

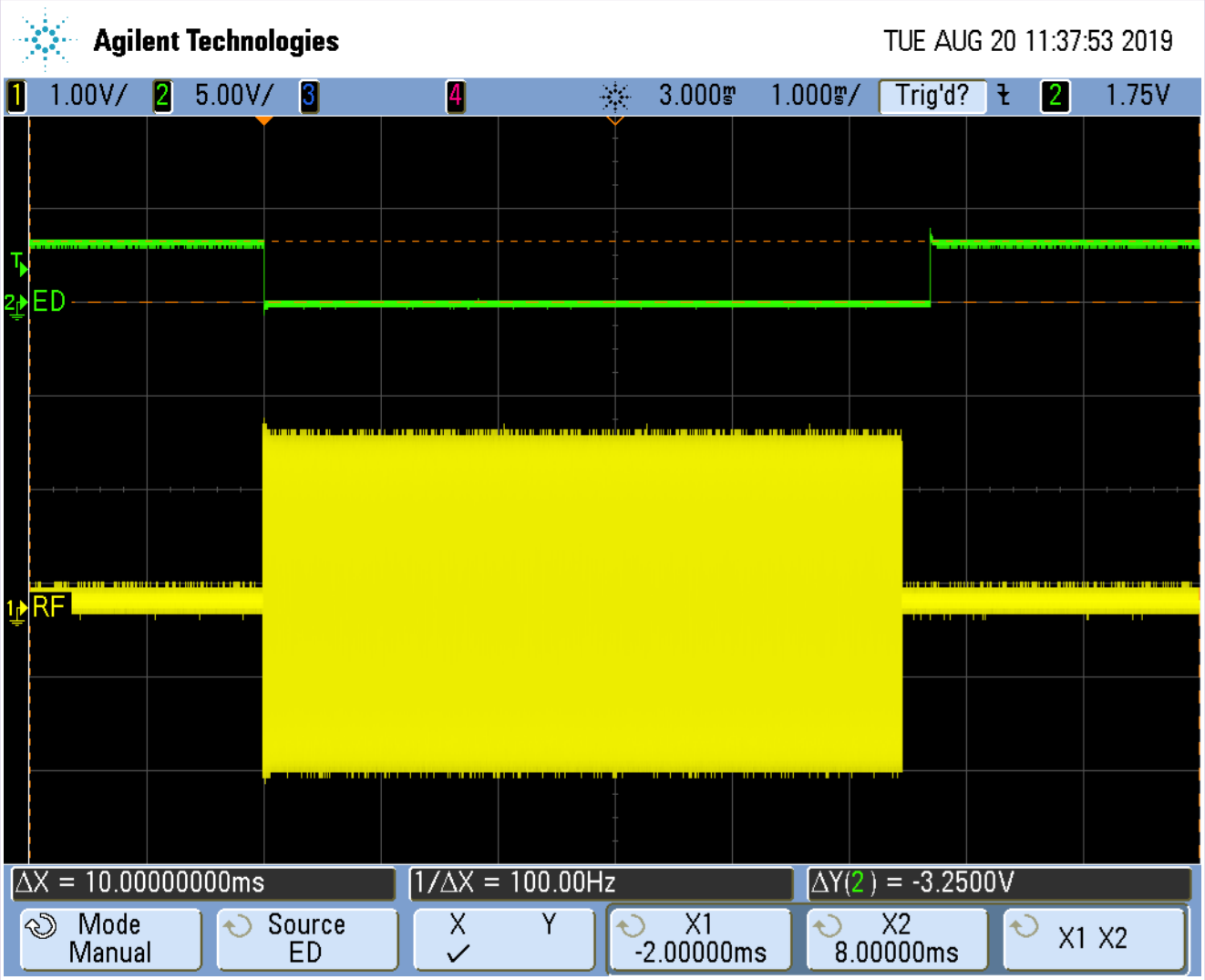

Figure 5. ED pin used for NFC field ON/OFF detection

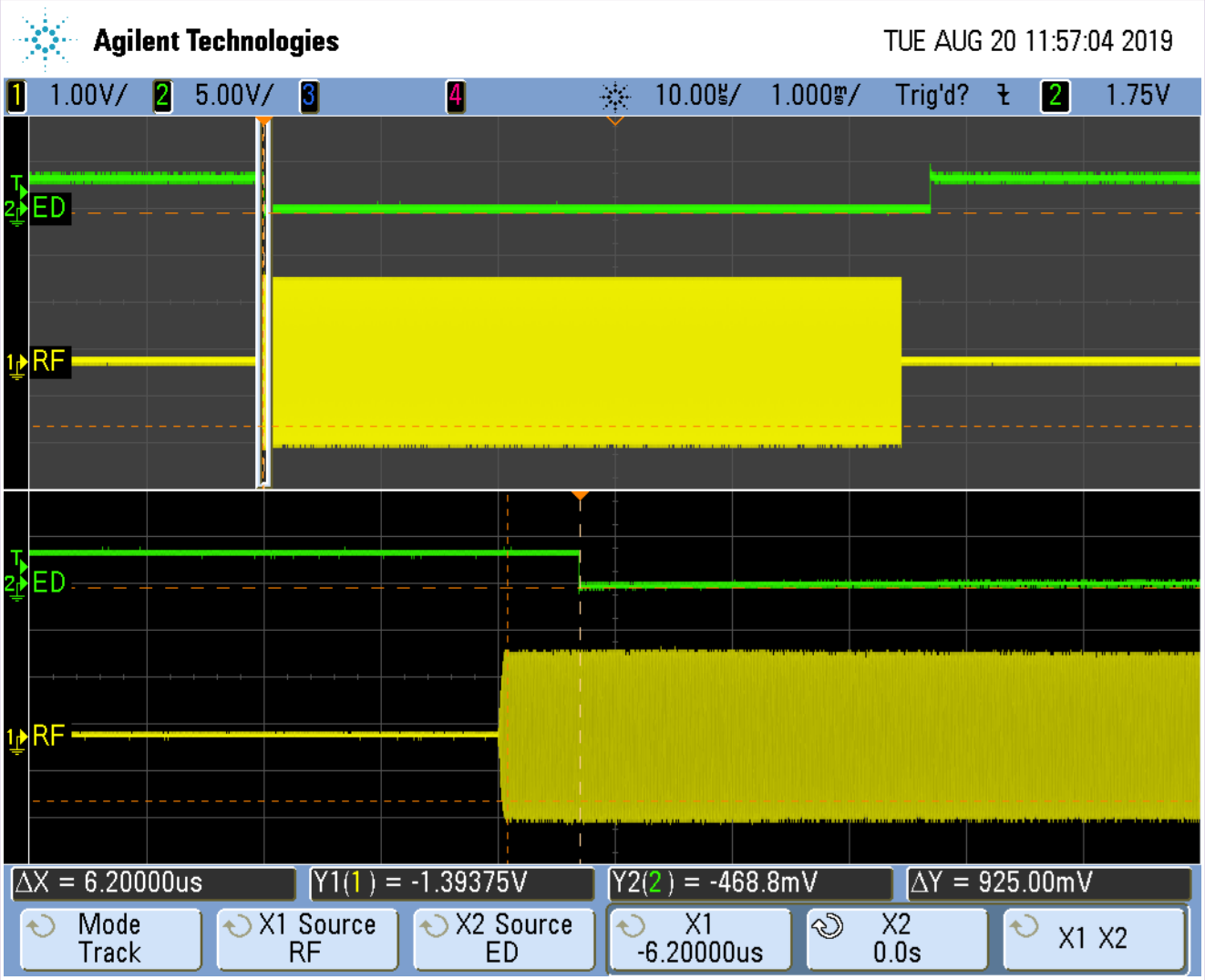

Figure 6. ED pin used for NFC field ON detection

ED pin is triggered (pulled LOW) ~6.2 µs after solid NFC field is present.

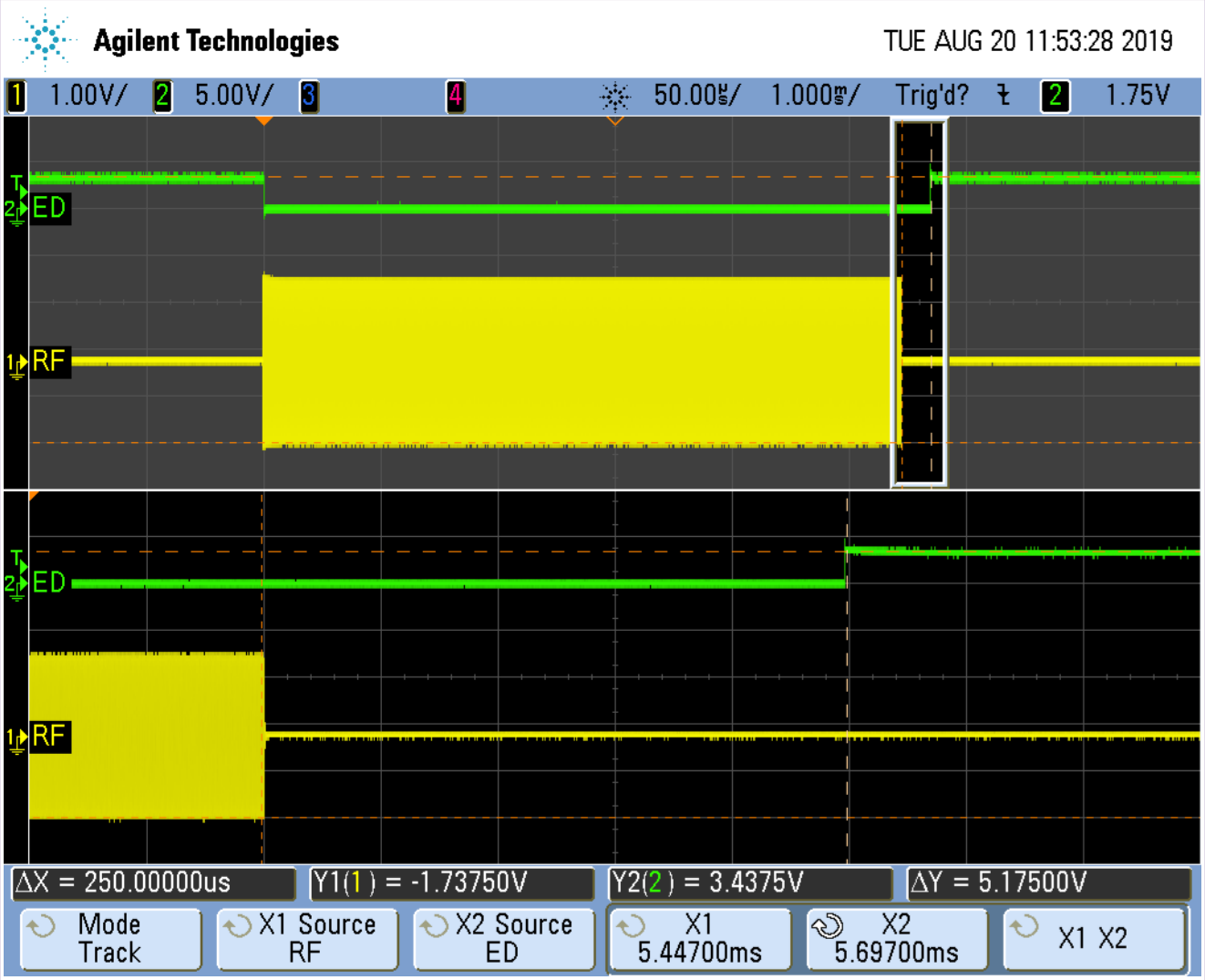

Figure 7. ED pin used for NFC field OFF detection

ED pin is released (transition to HIGH) ~250 µs after NFC field is turned-off / not present anymore.

5.2 Example 5 - PWM0 signal reflection on ED pin (PWM)

5.2.1 Description

ED pin can reflect PWM0 signal. PWM0 can be configured as PWM output on ED or SCL pin.

In following example the signal from GPIO0_PWM0 pin, duty cycle of it, is reflected to ED pin. Because ED pin is open-drain, it is pulled LOW during the OFF period of PWM0 signal.

5.2.2 Registers values

Table 18. ED_CONFIG_REG

Block Address		Byte 0	Byte 1	Byte 2	Byte 3
NFC	I^2C				
A8h	10A8h	02h	00h	00h	00h

5.2.3 Result

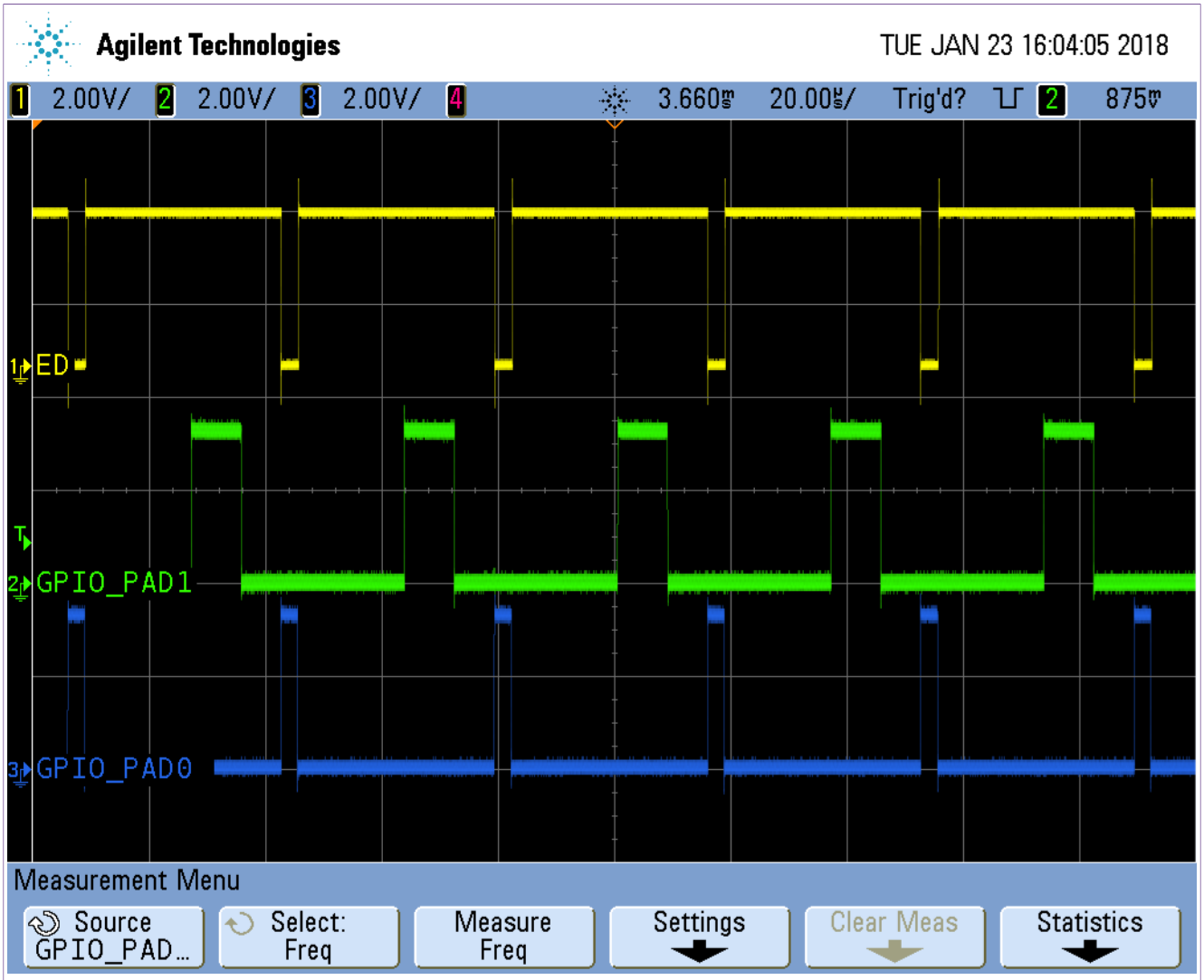

Figure 8. Example 5 - ED = ON during the off period of PWM0 signal

In above scope trace ED pin reflects the same PWM0 signal as the GPIO0 pad (named GPIO_PAD0).

5.3 Example 6 - $I^2C \rightarrow$ NFC Pass-through mode

5.3.1 Description

ED pin can be used to determine following states in Pass-through mode of operation:

- ED=ON: Last byte of SRAM data has been read by NFC, means host (I^2C) can start writing data to the SRAM.
- ED=OFF:
  - Last byte written by I^2C
  - or NFC is OFF or
  - I^2C supply is OFF

5.3.2 Register values

ED_CONFIG(_REG) = 0011b

5.3.3 Results

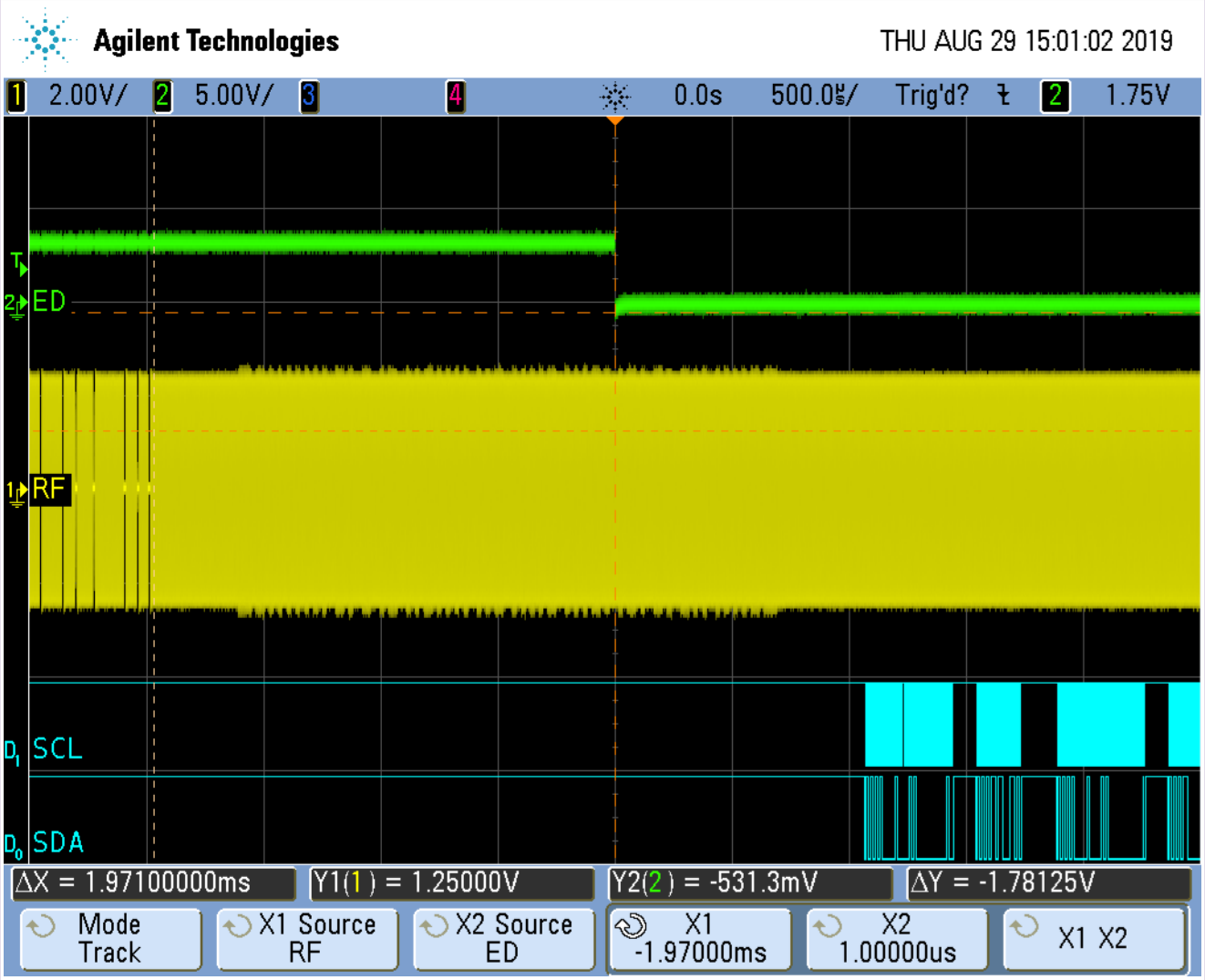

Figure 9. I²C -> NFC in Pass-though mode, ED on

ED pin is triggered (pulled LOW) when VICC responds to the NFC reader with the last SRAM byte (3Fh). ~1.98 ms after EOF of VCD READ_SINGLE_BLOCK command received, before VICC's responds with CRC bytes.

Arbiter locks to I2C interface:

- NFC_IF_LOCKED = 0b
- I²C_IF_LOCKED = 1b
- SRAM_DATA_READY= 0b

I²C host can start writing new data to SRAM.

Note: Optionally I²C host can poll for SRAM_DATA_READY= 0b instead of using ED pin in this configuration.

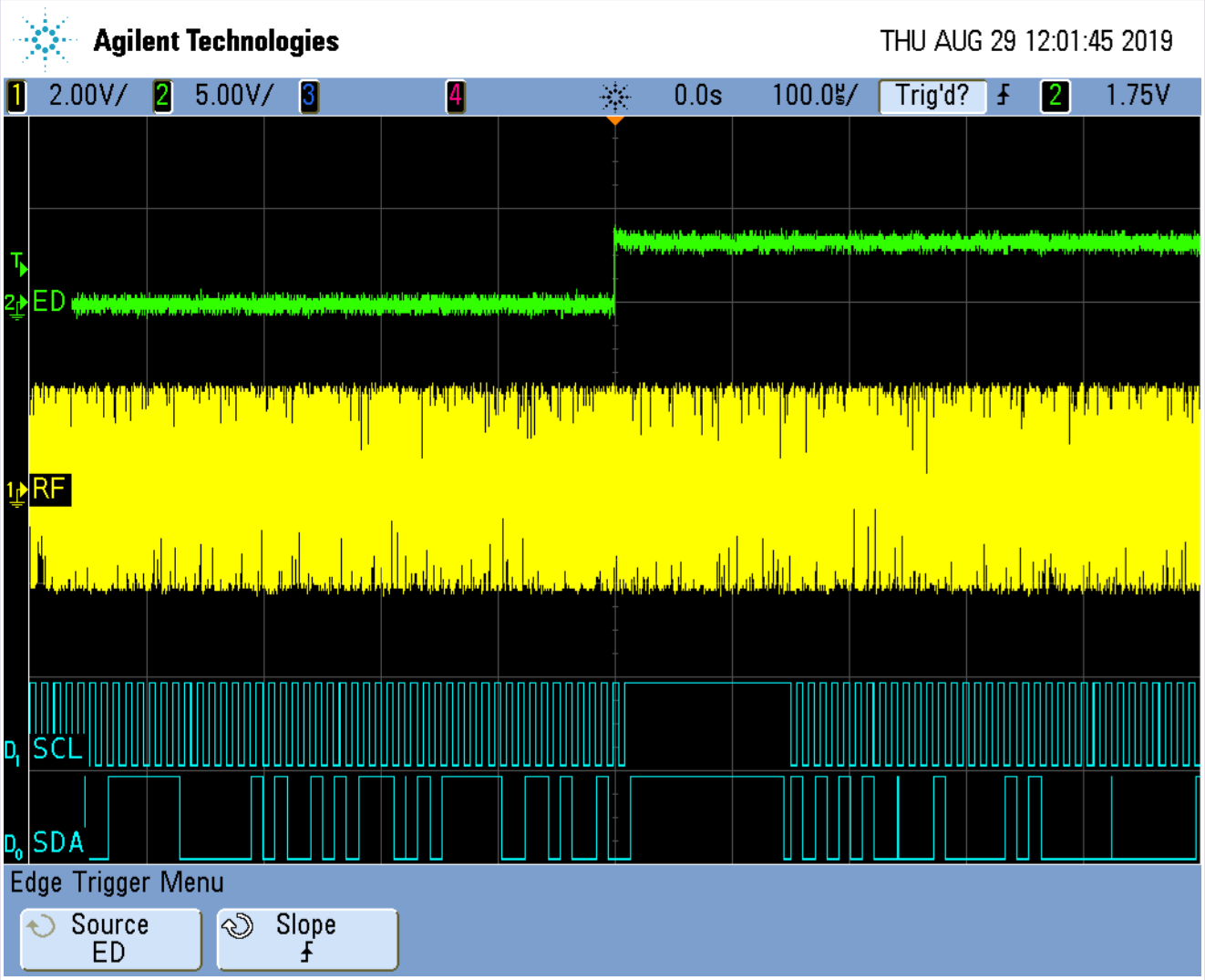

Figure 10. I^2C -> NFC in Pass-though mode, ED off

ED pin is released (transition to HIGH) on the last I^2C (SCL) clock cycle - before NTAG's ACK, when the last byte of SRAM (203Fh) is written.

5.4 Example 7 - NFC → I^2C Pass-through mode

5.4.1 Description

ED pin can be used to determine following states:

- ED=ON: Last byte is written by NFC, meaning that host can read data from SRAM
- ED=OFF:
  - Last byte is read from I^2C
  - or NFC OFF
  - or I^2C supply OFF

5.4.2 Register values

ED_CONFIG(_REG) = 0100b

5.4.3 Results

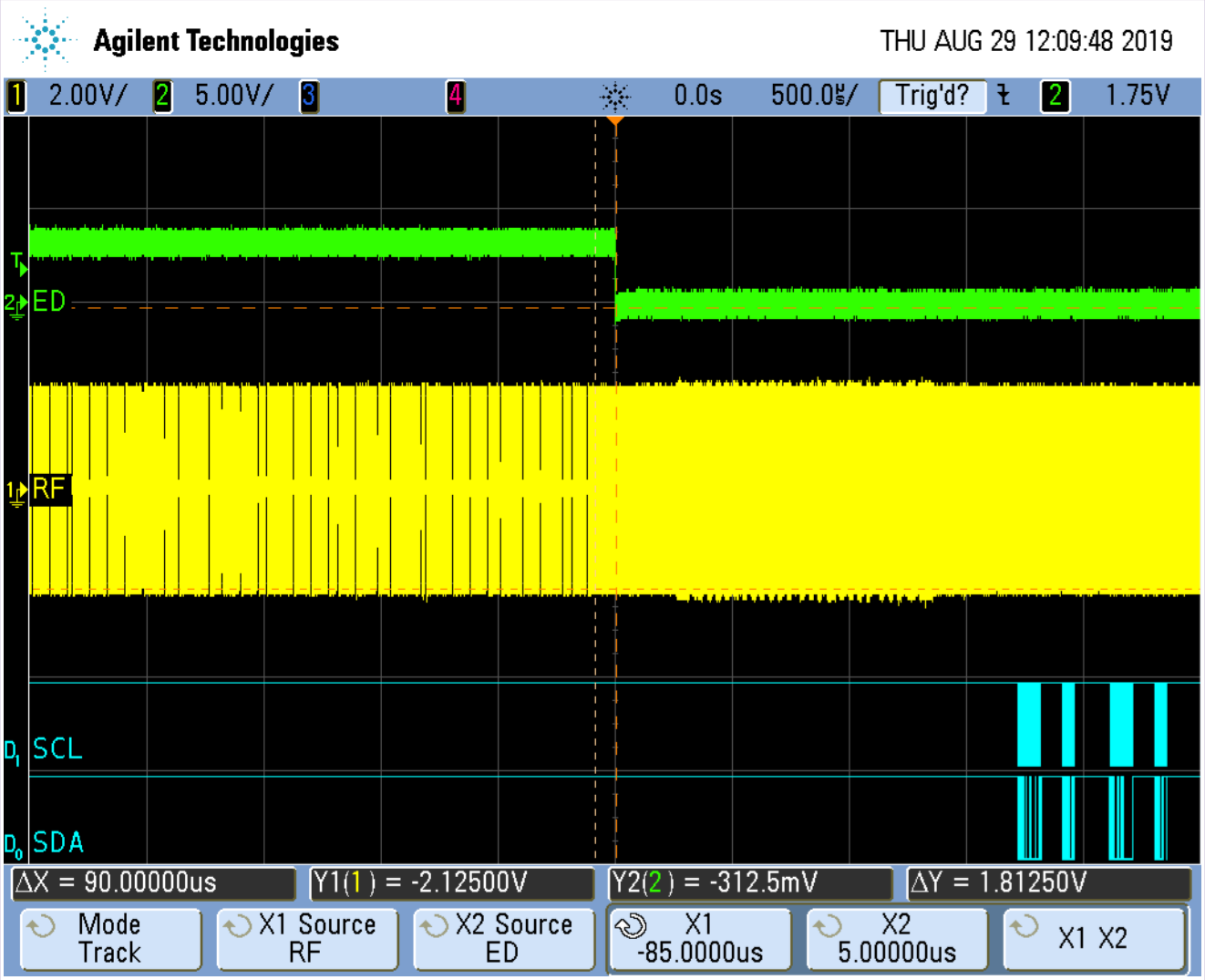

Figure 11. NFC → I²C in Pass-though mode - Last byte written by NFC, host can read data from SRAM

ED pin is triggered (pulled LOW) when last SRAM byte (3Fh) is written by NFC. I²C host can start reading SRAM data ~90 µs after VCD's EOF.

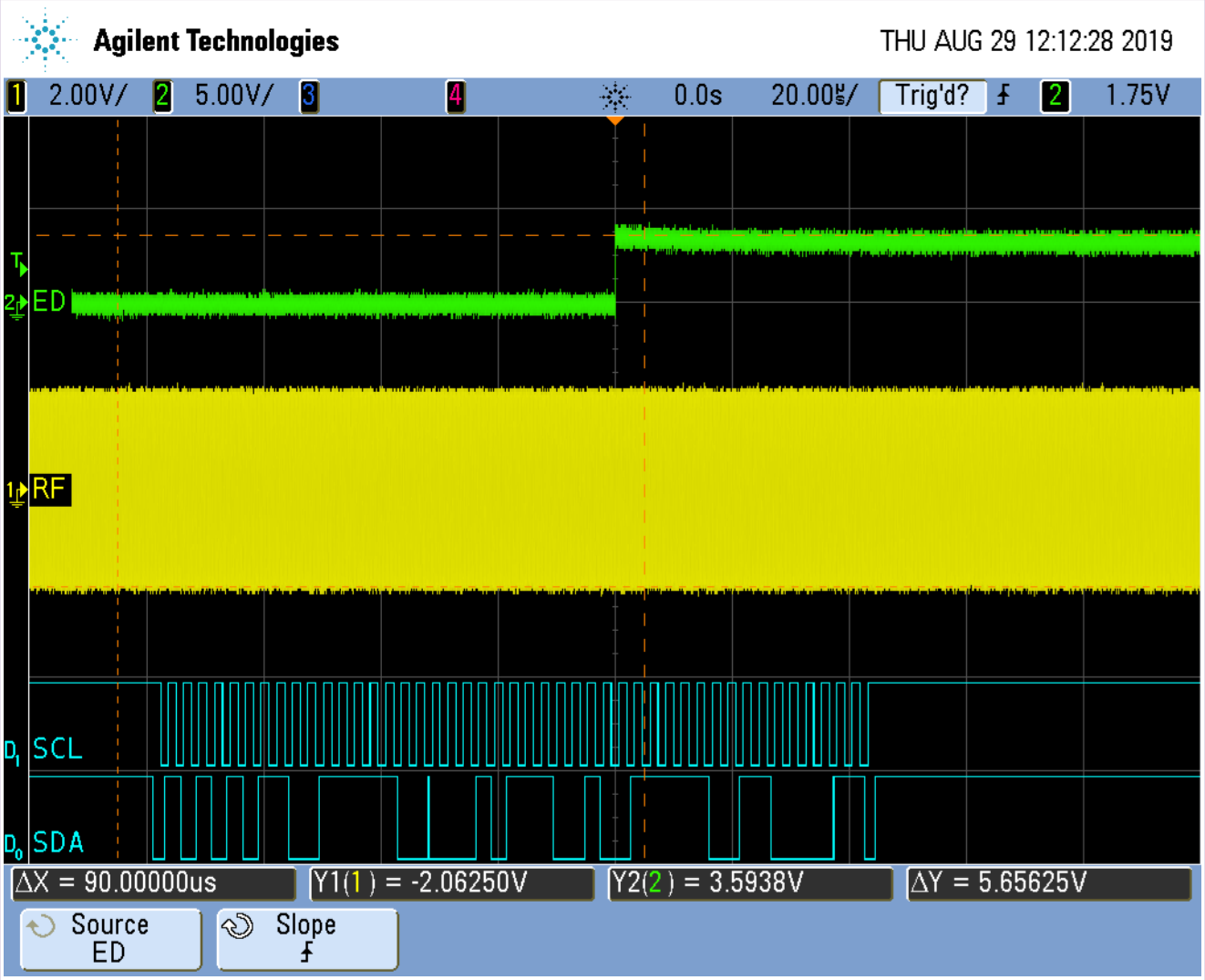

Figure 12. NFC → I²C in Pass-though mode - Last byte has been read from host (I²C), or NFC off or Vcc off.

ED pin is released (transition to HIGH) when I²C starts to read the last byte of SRAM (203Fh), with delay of ~90 µs.

5.5 Example 8 - Arbiter lock

5.5.1 Description

ED pin can be used also to determine whether Arbiter locked access for NFC interface or not.

- ED=ON: when NFC_IF_LOCKED =1b
- ED=OFF: when NFC_IF_LOCKED =0b

5.5.2 Register values

ED_CONFIG(_REG) = 0101b

5.5.3 Results

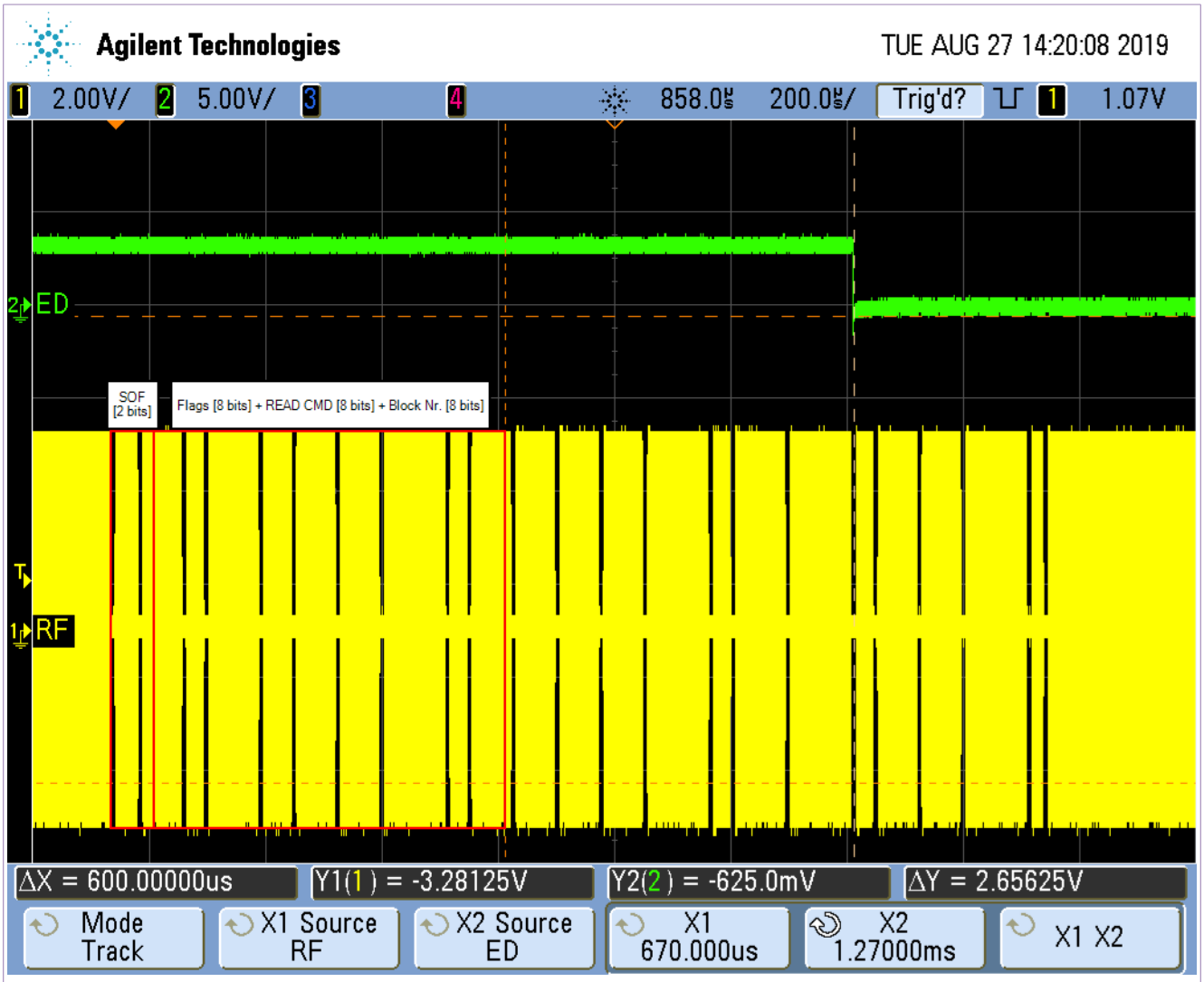

Figure 13. Arbiter locked access to NFC interface, ED on

ED pin is triggered (pulled LOW) when Arbiter locks to NFC interface ~600 µs after NTAG recognizes READ command and Block number to be read.

ED pin is released (transition to HIGH) when Arbiter releases access to NFC ~92 µs after VCD's EOF.

5.6 Example 9 - NDEF Message TLV length

5.6.1 Description

ED pin can be used also to determine if NDEF data length is ZERO or NON ZERO. As defined in [T5T], chapter 7.5.3 NDEF Write Procedure, before writing Terminator TLV (0xFE), Length value (of TLV) shall be updated. L byte is on T5Ts always in Block1:Byte1. Host can be informed when this is done through ED pin. Use case can be NFC Forum defined TNEP [TNEP].

- ED=ON: when Block 1 byte 1 i.e. NDEF length byte is non-zero during write command.
- either:
  - ED=OFF when Block 1 byte 1 i.e. NDEF length byte is zero during write command
  - NFC Field is OFF.

NOTE: Counting of blocks and bytes start from 0h.

5.6.2 Register values

ED_CONFIG(_REG) = 0110b

5.6.3 Results

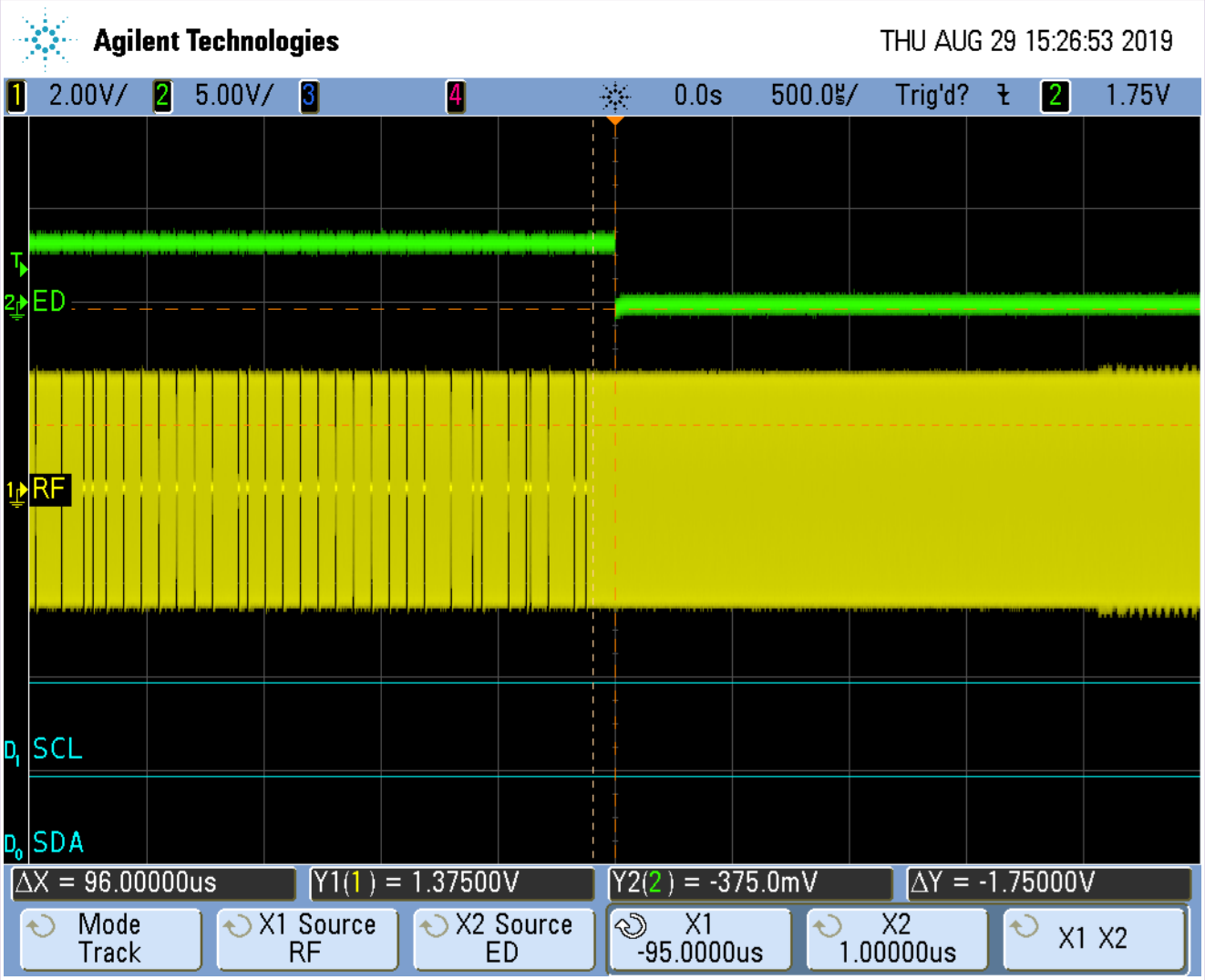

Figure 14. NDEF length byte written (value 02h) - After request's EOF, ED on

ED pin is triggered (pulled LOW) ~90 µs after VCD's WRITE command's EOF, addressing byte 1 in block 1.

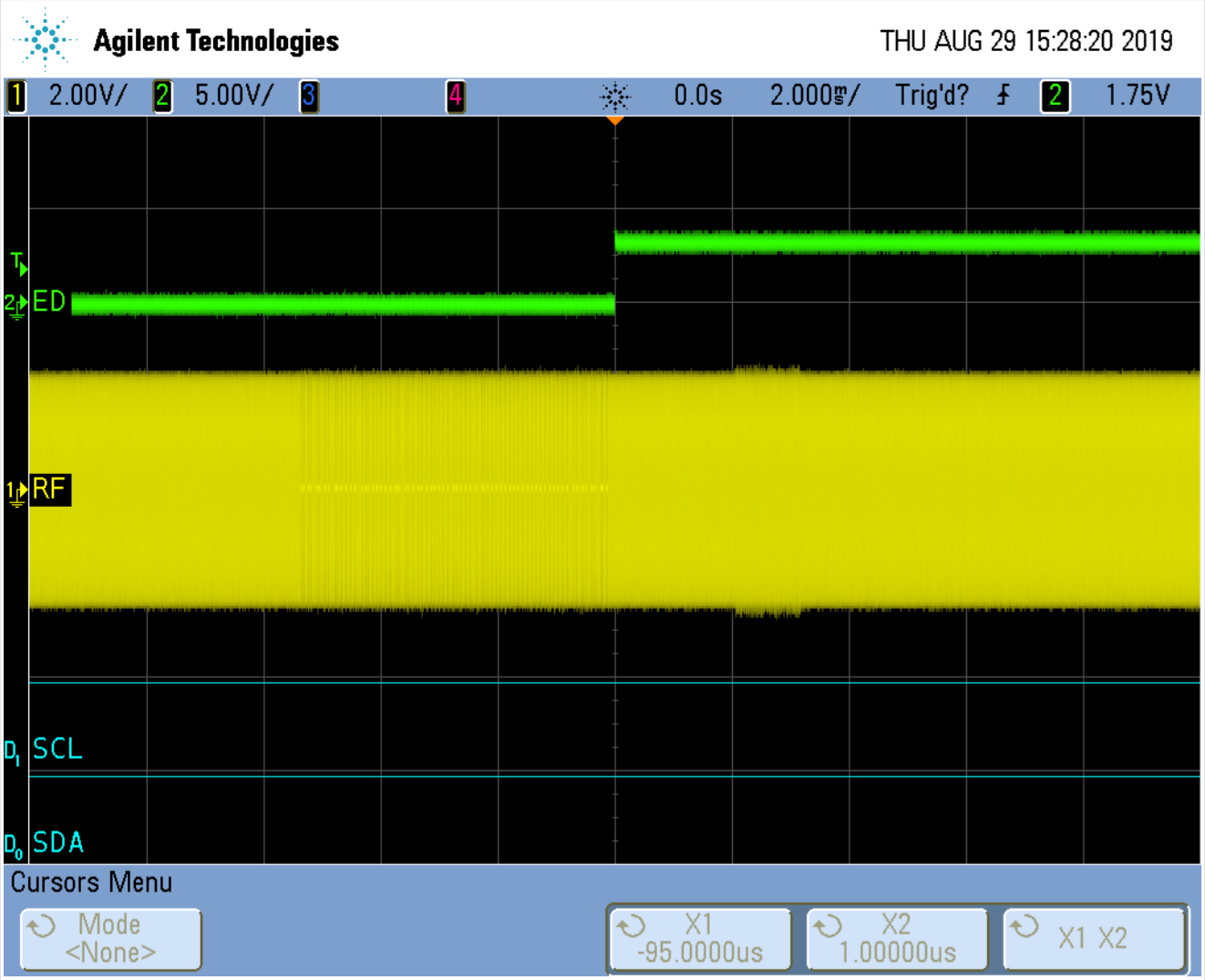

Figure 15. NDEF length byte is zero (00h) during WRITE SINGLE BLOCK to block1, values: 00h 00h 00h 00h command, ED off

ED pin is released (transition to HIGH) when value 00h is written to byte 1 in block 1.

5.7 Example 10 - Stand-by mode

5.7.1 Description

ED pin can be used to determine to Host, if NTAG 5 is in standby mode upon V_{CC} boot-up.

- ED=ON: when IC is not in standby mode
- ED=OFF when IC is in standby mode

5.7.2 Register values

ED_CONFIG(_REG) = 0111b

5.7.3 Results

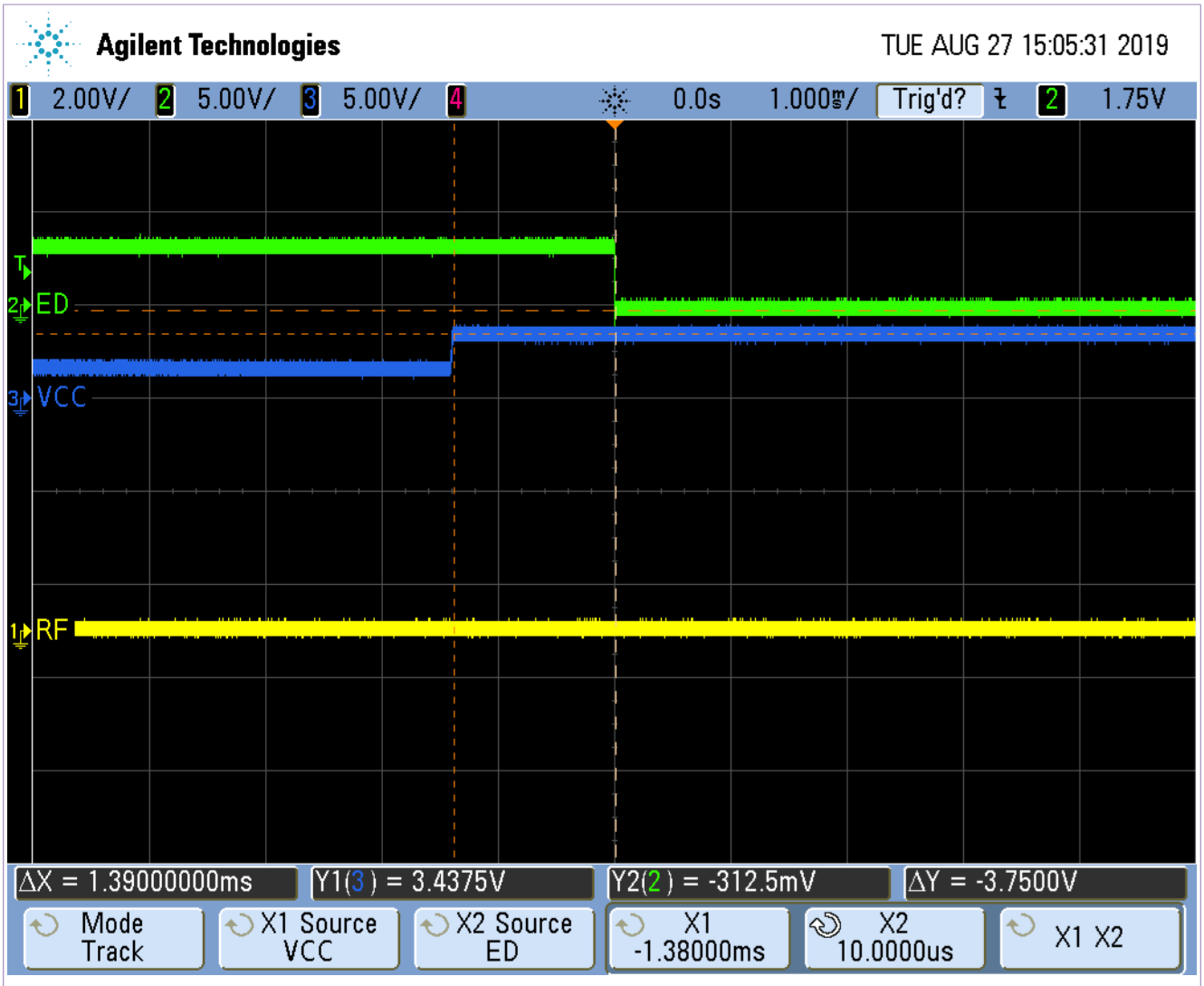

Figure 16. Indication to host that NTAG 5 is in automatic standby mode upon Vcc boot-up

ED pin is triggered (pulled LOW) ~1.39 ms after V_{CC} presence, to notify the I^2C host that NTAG entered standby mode.

5.8 Example 11 - WRITE command indication

5.8.1 Description

ED pin can be used as indication to host if there is any WRITE command ongoing to user memory, configuration bytes or SRAM.

- ED=ON: start of write command
- ED=OFF:
  - end of write command response
  - NFC Field is OFF.

5.8.2 Register values

ED_CONFIG(_REG) = 1000b

5.8.3 Results

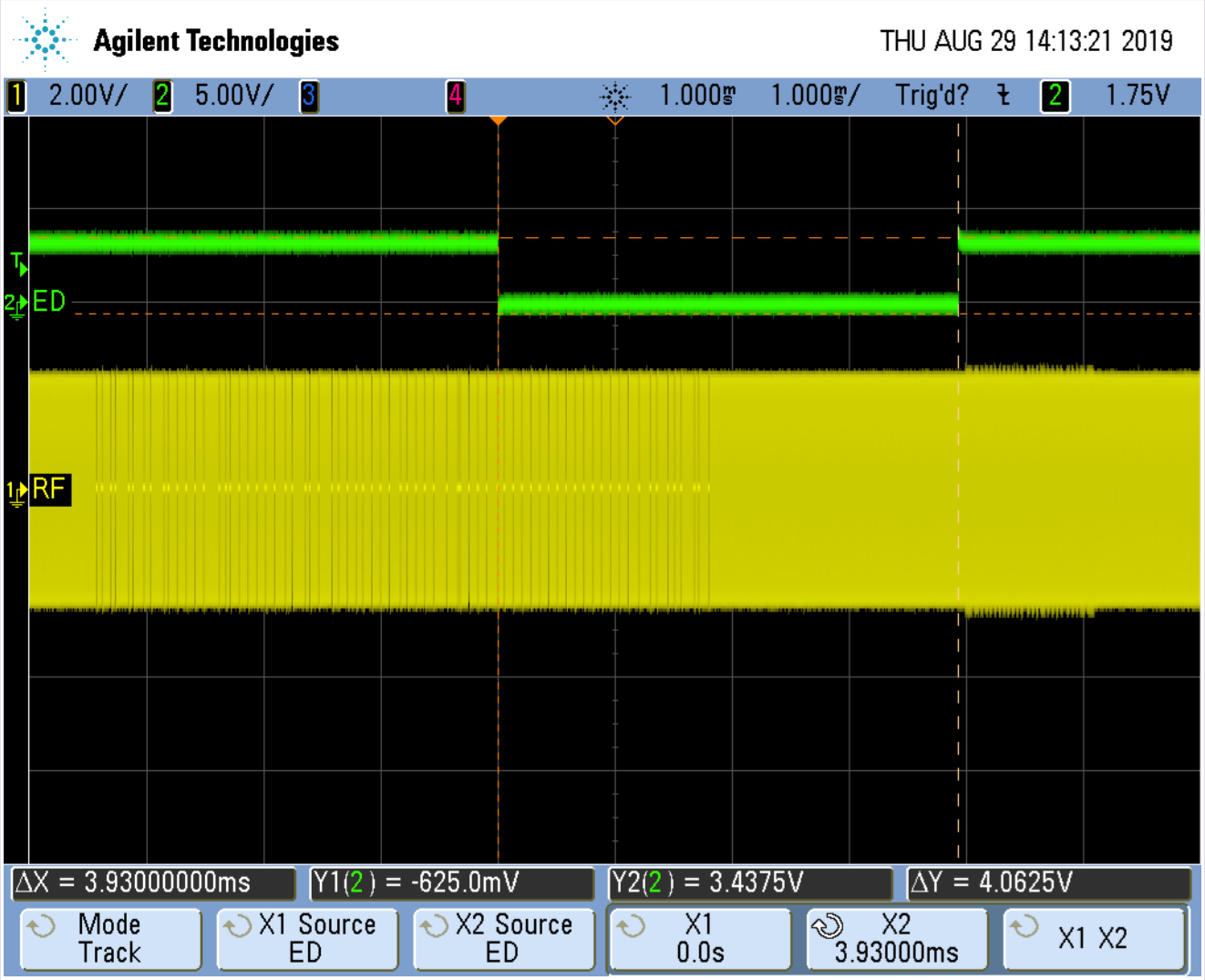

Figure 17. WRITE command (non Session register access) is ongoing, ED on/ED off

ED pin is triggered (pulled LOW) ~3.5 ms after VCD's WRITE command's SOF. ED pin is released (transition to HIGH) after ~3.93 ms after.

5.9 Example 12 - READ command indication

5.9.1 Description

ED pin can be used as indication to host if there is any READ command ongoing to user memory, configuration bytes or SRAM.

- ED=ON: start of READ command
- ED=OFF:
  - end of READ command response
  - NFC Field is OFF.

5.9.2 Register values

ED_CONFIG(_REG) = 1001b

5.9.3 Results

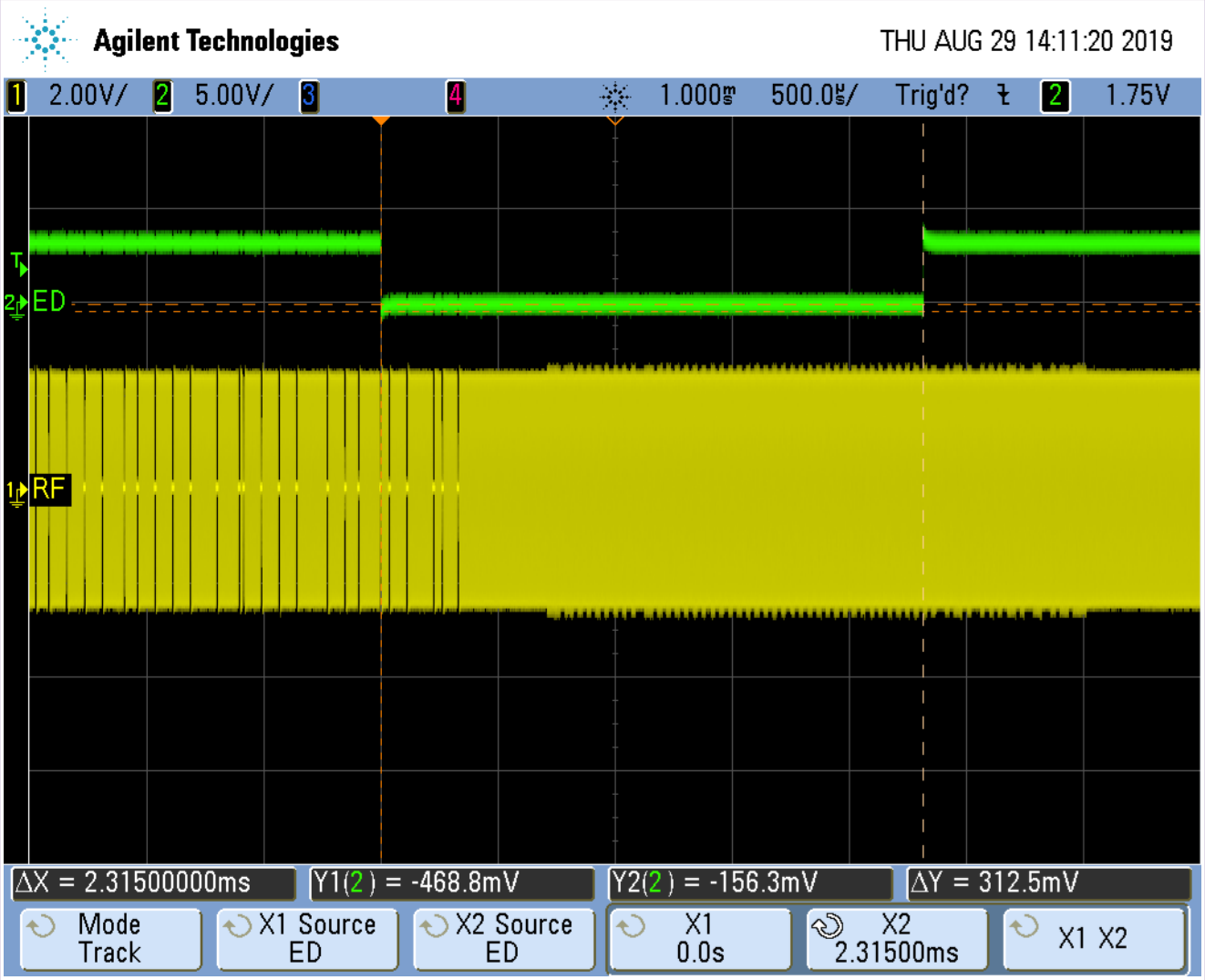

Figure 18. READ command (non-session register access) is ongoing, ED on/ED off

ED pin is triggered (pulled LOW) ~3.5 ms after VCD's READ command's SOF. ED pin is released (transition to HIGH) after ~2.32 ms after.

5.10 Example 13 - Start of command indication

5.10.1 Description

ED pin can be used as indication to host if there is any command ongoing.

- ED=ON: start (Start Of Frame) of any command
- ED=OFF:
  - end of any command response
  - NFC field is OFF.

5.10.2 Register values

ED_CONFIG(_REG) = 1010b

5.10.3 Results

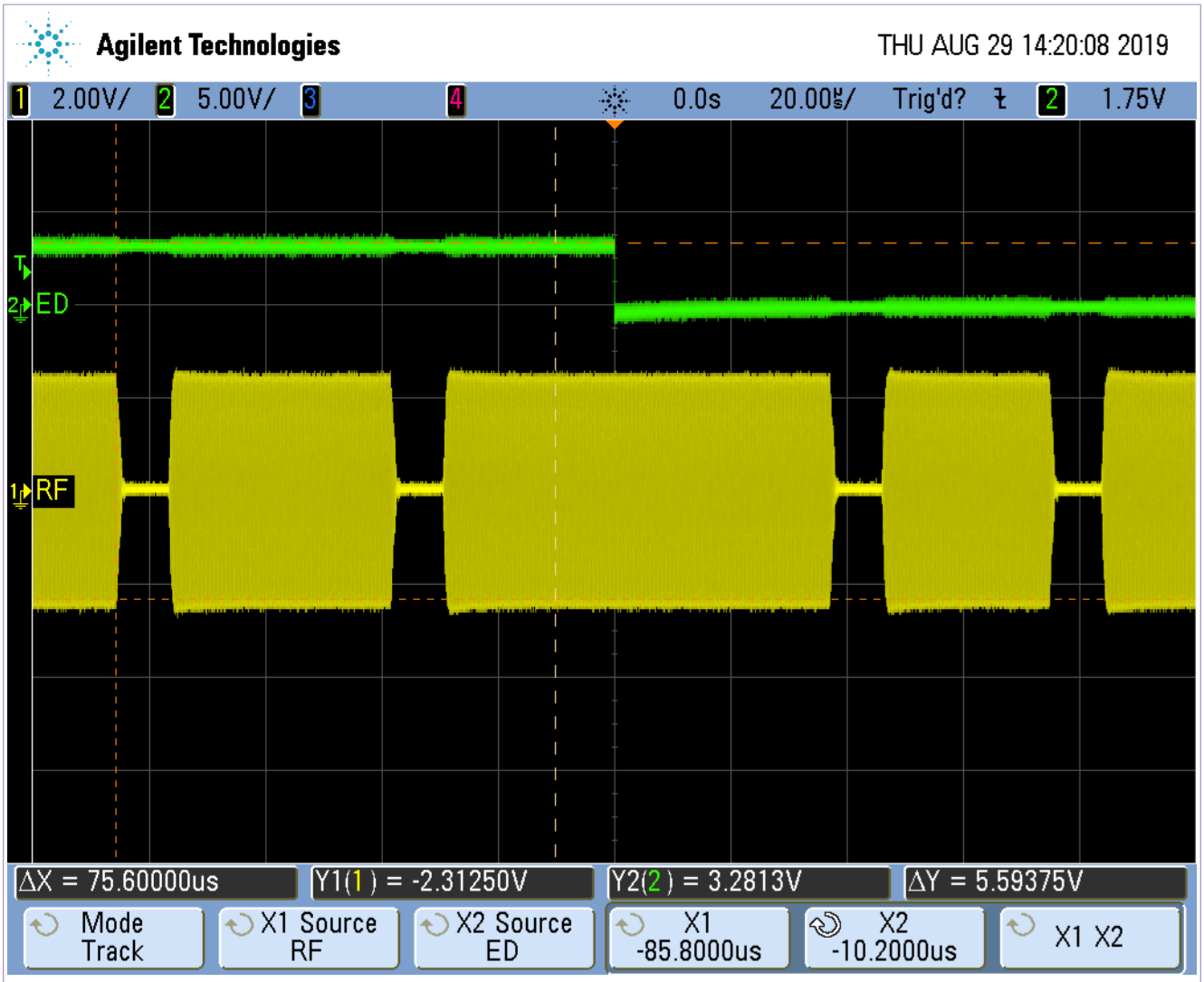

Figure 19. Start of any VCD Request (command) - SOF

ED pin is triggered (pulled LOW) ~10 µs after VCD's any command's SOF.

Note: X1 and X2 mark SOF coding.

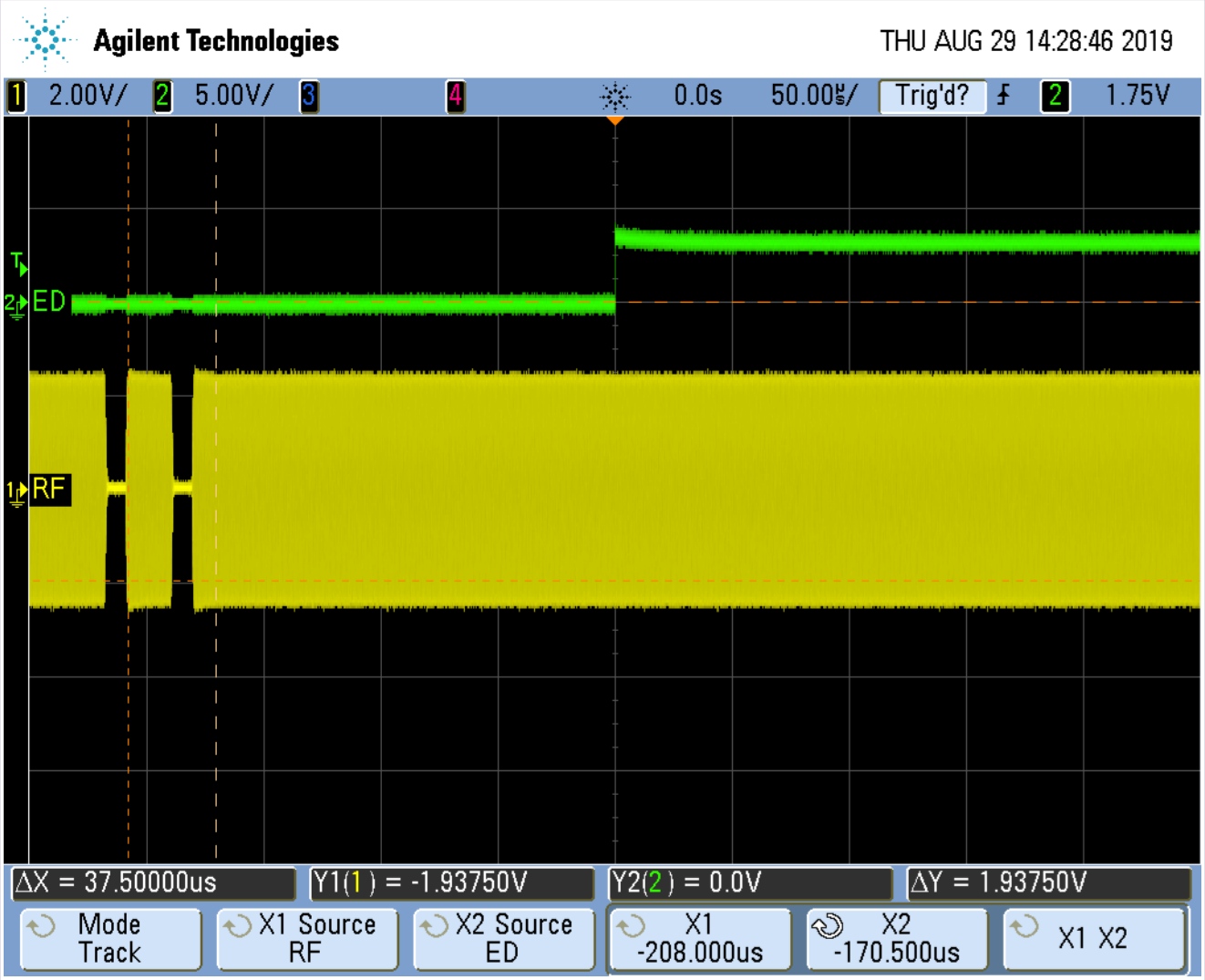

Figure 20. End of frame of any VCD Request (command) - EOF

ED pin is released (transition to HIGH) ~160 µs after VCD's any command's EOF.

Note: X1 and X2 mark EOF coding.

5.11 Example 14 - READ from SYNCH_DATA_BLOCK

5.11.1 Description

ED pin can be used as indication to host if data is READ from SYNCH_DATA_BLOCK.

- ED=ON if data is read from SYNCH_DATA_BLOCK
- ED=OFF:
  - Event needs to be cleared by setting b0 of ED_RESET_REG to 1b
  - NFC Field is OFF.

5.11.2 Register values

ED_CONFIG(_REG) = 1011b

5.11.3 Results

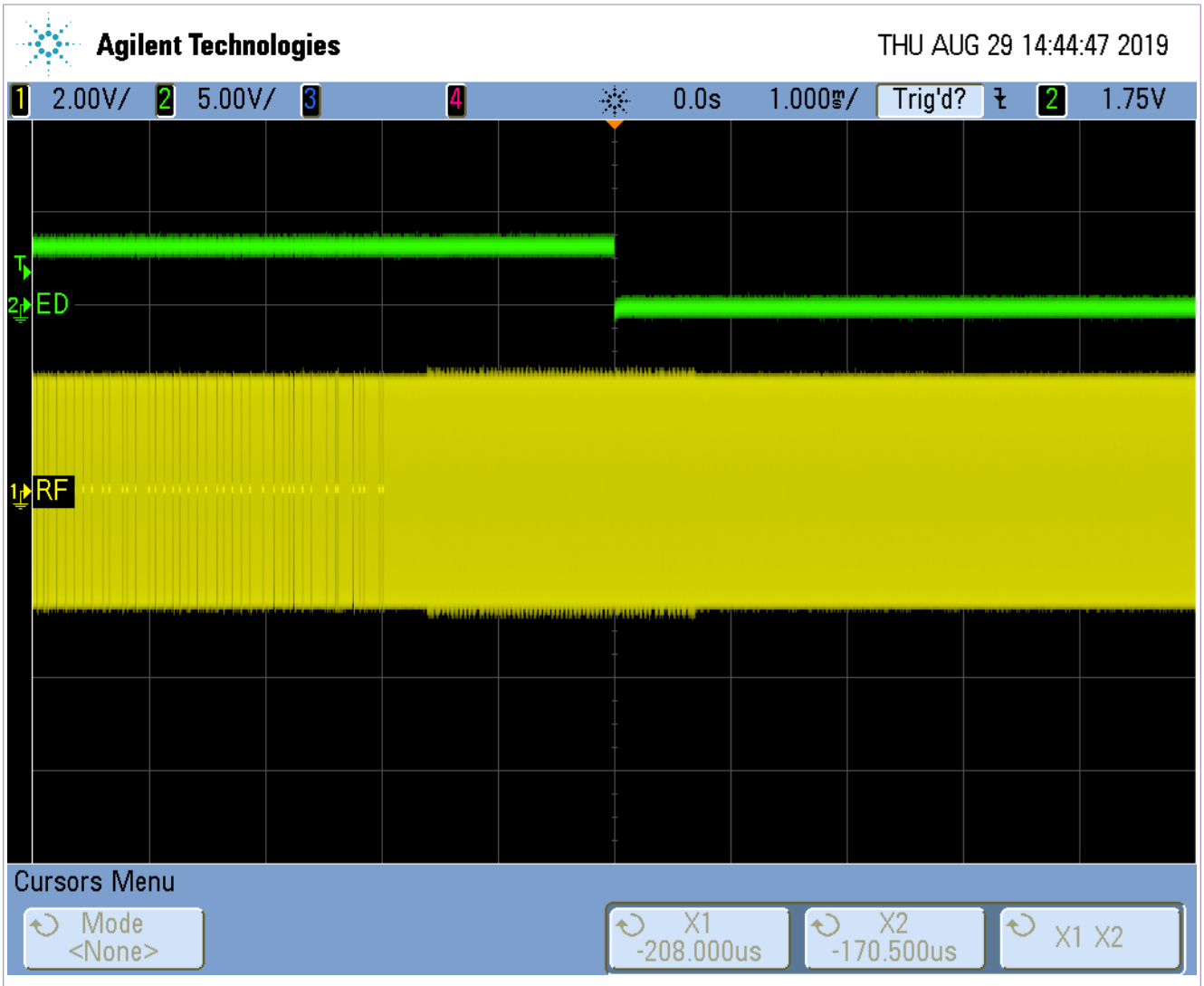

Figure 21. Data READ from SYNCH_DATA_BLOCK, ED on

ED pin is triggered (pulled LOW) when VICC returns last byte of SYNCH_DATA_BLOCK, before CRC.

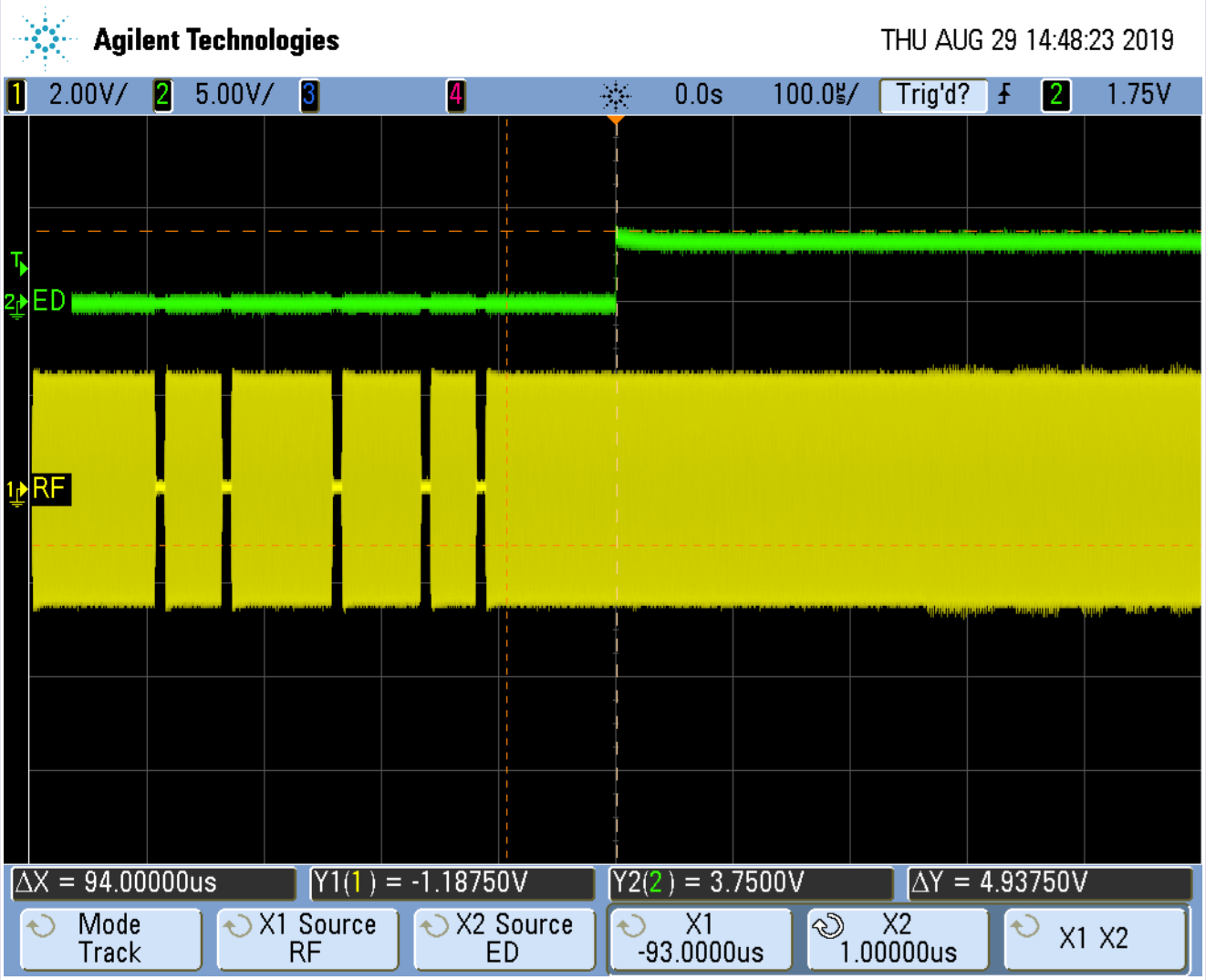

Figure 22. ED cleared by setting b0 of ED_RESET_REG to 1b

ED pin is released (transition to HIGH) when ED_RESET_REG is set to 1b with WRITE_CONFIG command, ~94 µs after it is EOF.

5.12 Example 15 - WRITE to SYNCH_DATA_BLOCK

5.12.1 Description

ED pin can be used as indication to host if data is written to SYNCH_DATA_BLOCK.

- ED=ON if data is written to SYNCH_DATA_BLOCK
- ED=OFF:
  - Event needs to be cleared by setting b0 of ED_RESET_REG to 1b
  - NFC Field is OFF.

5.12.2 Register values

ED_CONFIG(_REG) = 1100b

5.12.3 Results

Results look the same as in [Figure 21] and [Figure 22].

5.13 Example 16 - Software driven Interrupt

5.13.1 Description

ED pin can be triggered by:

- ED=ON when writing 1101b to ED_CONFIG_REG
- ED=OFF:
  - Event needs to be cleared by setting b0 of ED_RESET_REG to 1b

Remark: NFC Field is OFF does not toggle ED pin.

5.13.2 Register values

ED_CONFIG_REG = 1101b

5.13.3 Results

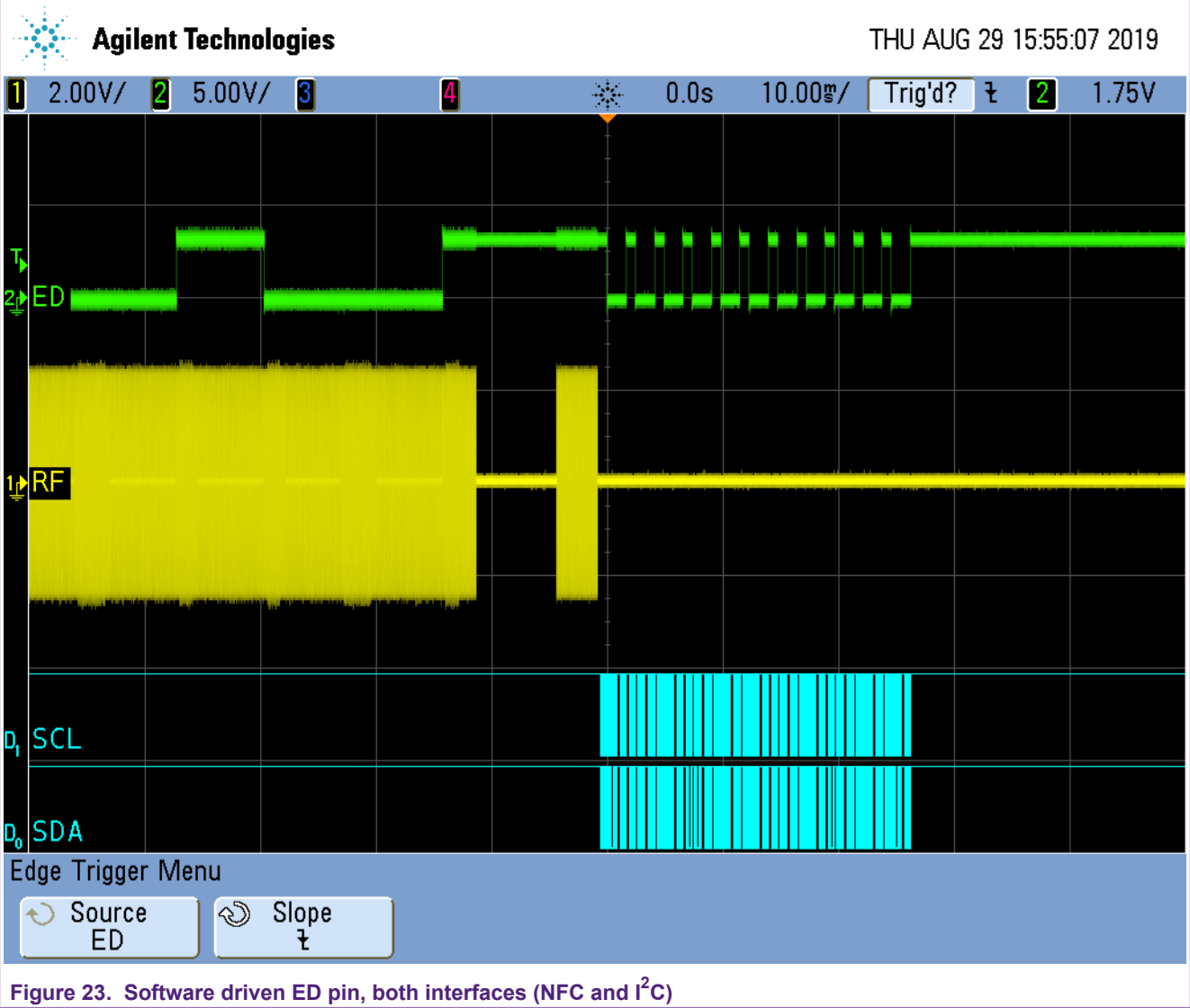

Figure 23. Software driven ED pin, both interfaces (NFC and I^2C)

ED pin is released (transition to HIGH) by writing 1101b to ED_CONFIG_REG from both NFC and I^2C interface.

6 References

[1] NTP5210 - NTAG 5 switch, NFC Forum-compliant PWM and GPIO bridge, doc.no. 5477xx
https://www.nxp.com/docs/en/data-sheet/NTP5210.pdf

[2] NTP53x2 - NTAG 5 link, NFC Forum-compliant I^2C bridge, doc.no. 5476xx
https://www.nxp.com/docs/en/data-sheet/NTP53x2.pdf

[3] NTA5332 - NTAG 5 boost, NFC Forum-compliant I^2C bridge for tiny devices, doc.no. 5475xx
https://www.nxp.com/docs/en/data-sheet/NTA5332.pdf

[4] NFC Forum specification, Type 5 Tag - Technical Specification Version 1.0 2018-04-27 [T5T] NFC Forum™
https://nfc-forum.org/product-category/specification/

[5] NFC Forum specification, Tag NDEF Exchange Protocol - Technical Specification Version 1.0 2019-04-24 [TNEP] NFC Forum™
https://nfc-forum.org/our-work/specifications-and-application-documents/specifications/nfc-forum-candidate-technical-specifications/

[6] AN11201 - NTAG 5 How to use energy harvesting, doc.no. 5304xx
https://www.nxp.com/docs/en/application-note/AN11201.pdf

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Figures

Contents

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