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Agile I/O Input / Output Characteristics

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Document information

Info	Content
Keywords	GPIO, Agile I/O, Input / Output Expanders,
Abstract	I^{2}C -bus GPIO devices are widely used and expand a control processor's pins to 8-, 16- or 24-bits of general-purpose input or output. The characteristic of these I/O needs to be accurately known to efficiently use them in a system. This application note will explore the actual electrical characteristics of Agile I/O GPIO pins.

Revision history

Rev	Date	Description
1.0	20140815	Initial Release

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1. Introduction

The I^{2}C-bus has been used for many years to communicate between chips using only two pins and a standard serial protocol. This is particularly useful in today's systems using microprocessors as the control element. Many times, the application outstrips the microprocessor's GPIO (general purpose input output) pins. An easy solution uses only two I^{2}C -bus pins and an I^{2}C I/O Expander to increase the number of input /output pins by 8, 16, or 24.

NXP has recently introduced a new family of I^{2}C Input / Output Expanders called Agile I/O GPIO which operate down to 1.65V power supply and have increased I/O functionality. This application note will explore the I/O pins capabilities and give information on the most efficient usage models.

2. Low Voltage I/O Device Overview

Devices in the LV GPIO family are differentiated by the number of I/O pins: eight or16. Other differences come from features like Reset and Interrupt. To aid in PCB layout, the device pinouts are similar. This lets the designer select the family and delay feature selection until later in the process. Low-voltage operation (1.65 to 5.5 V) and low current consumption make these devices ideal for a wide range of applications in portable, industrial, and automotive segments.

Table 1. Low Voltage Agile I/O Part Numbers

	Features	Industry-standard device (2.3 to 5.5 V)	NXP LV device (1.65 to 5.5 V)	NXP LV device with Agile I/O (1.65 to 5.5 V)	NXP LV device with dual V_{CC} for level translation
8-bit	Interrupt	PCA9534			PCA(L)6408A
	Interrupt & reset	PCA9538	PCA9538A	PCAL9538A	
	Interrupt & pull-up	PCA9554 PCA9554A	PCA9554B PCA9554C	PCAL9554B PCAL9554C	
16-bit	Interrupt	PCA9535	PCA9535A	PCAL9535A	PCA(L)6416A
	Interrupt & reset	PCA9539	PCA9539A	PCAL9539A	
	Interrupt & pull-up	PCA9555	PCA9555A	PCAL9555A	

2.1 Agile I/O Features

2.1.1 Selectable output drive strength

Drive strength control allows one to modify the current drive capability of the output pin from 25%, 50% or 75% to 100%. Reducing the current drive capability may be desirable to reduce system noise. When the output switches (transitions from H/L), there is a peak current that is a function of the output drive selection. Switching many outputs at the same time will create ground and supply noise. The output drive strength control allows the user to minimize simultaneous switching noise issues without any additional external components.

2.1.2 Output configuration

The output configuration customizes the outputs for optimum performance in the application. Previously, separate part numbers were needed for open-drain output versions or push-pull versions. With Agile I/O, outputs can be configured to either arrangement, which minimizes stocking levels and changes with a simple software configuration.

2.1.3 Input pull-up/pull-down resistors

Input pull-up/pull-down resistors are needed to guarantee that inputs are at a valid logic level. This usually involves external discrete components that complicate routing and take up PCB area. The internal pull-up or pull-down resistors are integrated, minimizing the bill of materials, and can be enabled with a simple software command.

2.1.4 Interrupt mask

The interrupt mask selects which inputs can cause an interrupt event on the output pin. Normally, any input transition will cause the pin to trigger an alert to the microprocessor. If one pin is connected to a signal that switches abnormally, this initiates a lot of unnecessary interrupt service software traffic on the microprocessor. By simply masking the abnormal input from generating an event on the pin, a large amount of software performance is saved with no extra hardware.

2.1.5 Interrupt status

The interrupt status register shows which input caused an event on the pin, simplifying the interrupt service routine software and minimizing software development and verification, and system testing.

2.1.6 Input latch

The input latch feature eliminates external hardware by implementing latches on all input pins. These lets the microprocessor sample inputs at a reduced rate and still determine which ones have changed states. This is important for interrupt service routines. Inputs can change states quickly, yet still require attention from the microprocessor software. The latch holds the input state until the software can read the input pins, putting fewer real-time demands on the microprocessor. This increases system reliability without additional hardware.

3. Physical Attributes of the Low Voltage Agile I/O Input & Output Pins

3.1 Input Structure

The input of a typical CMOS circuit is shown in Figure_1. Note the ESD (Electro Static Discharge) diodes connected from the package pin to VDD and VSS, limiting the input voltage swing to a diode drop away from these voltages.

The I^2C-bus should operate correctly even if a device on the bus is powered down, or VDD = 0V. If the input structures are constructed like the typical case, the bus would be held at ground in a power down situation.

Luckily, the input structure of the low voltage Agile I/O devices allow for overvoltage conditions – up to 5.5V as specified in the Limiting Conditions table of their datasheets. This overvoltage circuitry is proprietary to NXP and ensures maximum reliability of I^2C-bus systems. A curve tracer plot in Figure_2, shows a forward biased diode (approximately 0.6V) connected to ground and approximately a 10V breakdown voltage to V_{DD} on the SCL pin.

Besides presenting no load in a power down state, this overvoltage tolerance allows one to easily connect I^2C -bus devices operating at different power supply levels with no additional voltage level translators. Of course, a careful analysis of the input and output levels is required and this analysis is best left to another application note.

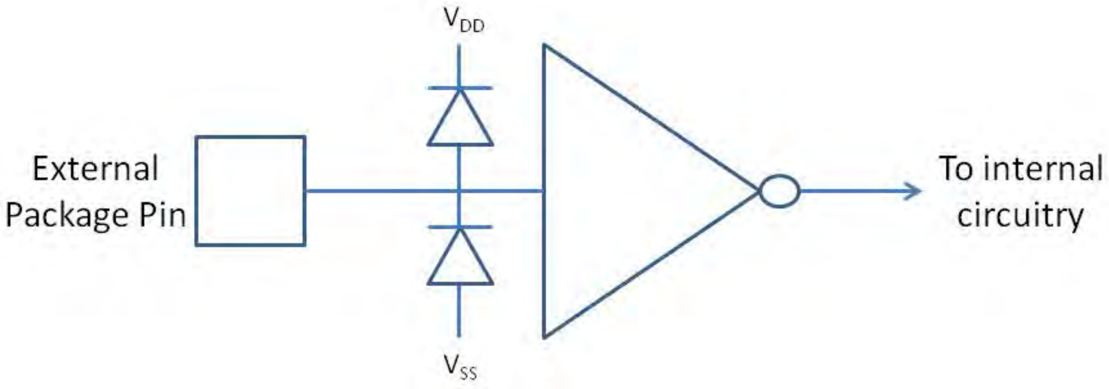

Fig 1. Typical CMOS Input Structure

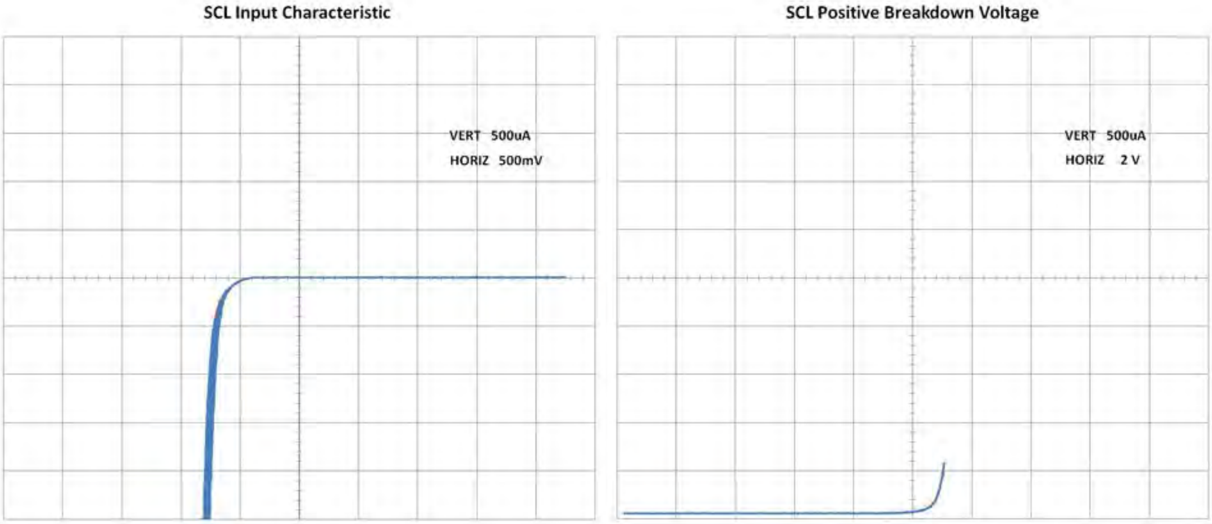

Fig 2. Curve Tracer Characteristic of Low Voltage Agile I/O Input (positive and negative direction

3.2 Input Voltage Levels

An important characteristic is the switching points of the input. The datasheet specifies V_{IH} (or the high level switch point) as 0.7 x V_{DD} and V_{IL} (or the low level switch point) as 0.3 x V_{DD}. These are guaranteed values. You can be assured that an input level above or below these points will be recognized as a high or low logic level.

We know, however, that the input structure is basically a CMOS inverter with a switching point around 0.5 x V_{DD}. The actual switch points of the general-purpose I/O is easy to measure, since any change on the input pin will trigger the $\overline{\text{INT}}$ Figure 3 shows a ramp connected to the I/O pin and the $\overline{\text{INT}}$ output. The switch point on the falling edge of the input ramp is approximately 1.7V (at a 3.3V V_{DD}) and 1.37V on the rising edge of the input ramp.

Fig 3. Input Voltage Level (channel 1 is the input voltage ramp, channel 2 is INT output)

The difference between the two switching levels is known as hysteresis – in this case approximately 350mV – and is useful to prevent false triggering when slowly varying signals are applied. The switching points and the hysteresis vary linearly with the power supply as shown in Table_2 .

Table 2. Typical Switching Points vs. Power Supply

Typical Values at 25°C

	VDD = 1.65V	VDD = 3.3V	VDD = 5.5V
V_{IH}	0.87	1.78	2.97
V_{IL}	0.75	1.43	2.3
Hysteresis	0.116	0.35	0.67

4. Output Structures

The standard totem pole or push-pull output structure of a CMOS device is show in Fig_4. A large p-channel transistor connects between V_{DD} and the output pin, while a large n-channel transistor connects between V_{SS} and the output pin. When the internal logic drive signal goes toward V_{DD}, the n-channel transistor turns on and sinks current from the output pin to V_{SS}. When the internal logic drive signal moves toward V_{SS}, the p-channel device turns on and it sources current out of the output pin.

There are parasitic connections to each power supply rail thru diodes that are integral to the physical construction of the output transistor. These diodes limit any external voltage applied to the output pin to a diode drop (approximately 0.6V) above V_{DD} and below V_{SS}. There are some cases where you would like the voltage on the output pin to be higher than V_{DD} of the driving circuit. An example would be an LED drive application Figure_6. The forward voltage drop of a simple LED is approximately 2V which would be impossible to drive correctly if the IC operating voltage is 1.8V. In fact, there can be significant current flow through the parasitic diode of the p-channel transistor to the 1.8V VDD pin upsetting any low power applications.

In this case, an open-drain driver Figure_5 has no diode to V_{DD} since there is no p-channel transistor. In the LED application case noted above, one could use a 3.3V supply connected to the LED current limit resistor and drive it correctly with the driver chip operating at 1.8V.

4.1 Output Characteristics

The pertinent specifications for an output, which are very clearly defined in the datasheet, are the output voltage (V_{OH} and V_{OL}) when sinking or sourcing a certain current and the output current (I_{OH} and I_{OH}) at a certain voltage. These specifications are holdovers from logic days and are very useful to determine the number of logic gates that can be connected to an output pin and still be reliably triggered.

Today’s I/O requirements are much more complex and more analog oriented. The previous LED example is a good example. If the current capacity of the n-channel output transistor is too low, it will be impossible to generate enough voltage drop across the LED to light it or light it bright enough. The rest of this section will discuss the analog output characteristics of Agile I/O GPIO Expander devices.

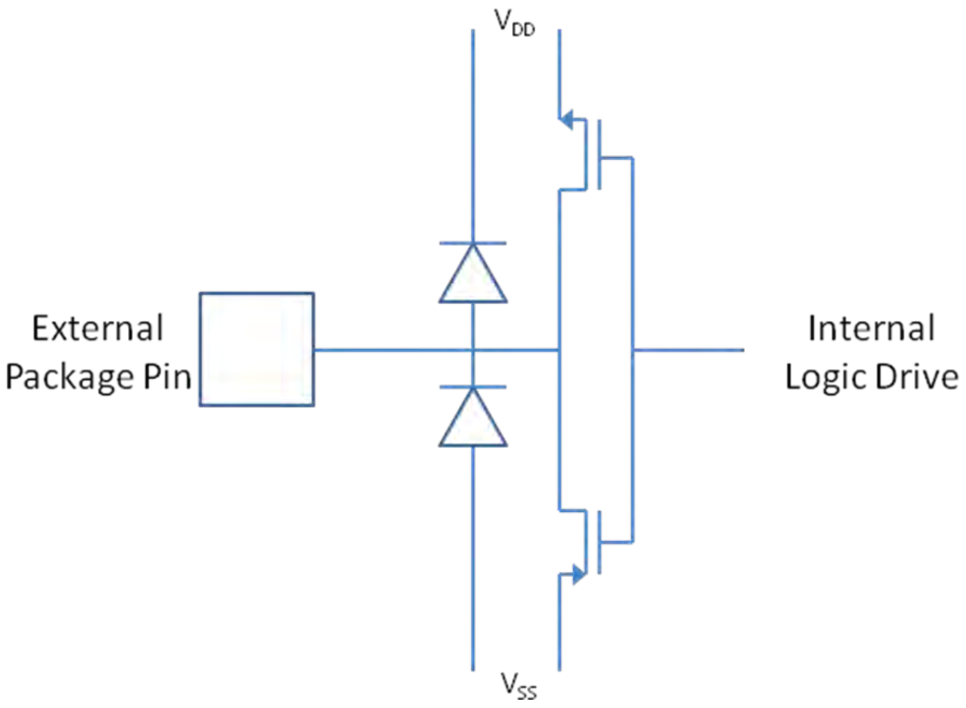

Fig 4. Standard CMOS totem pole or push-pull output

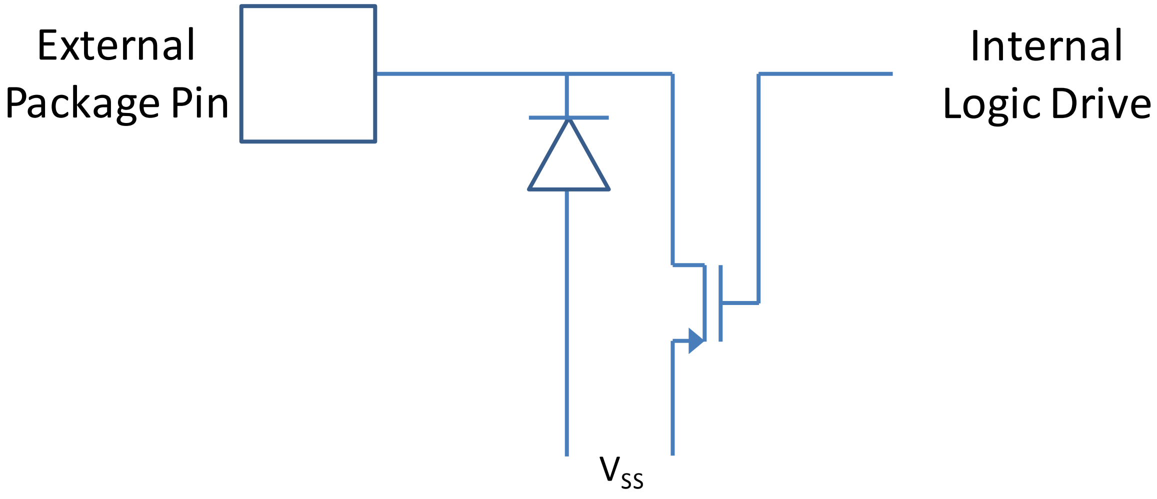

Fig 5. Standard CMOS open-drain output (no diode to V_{DD})

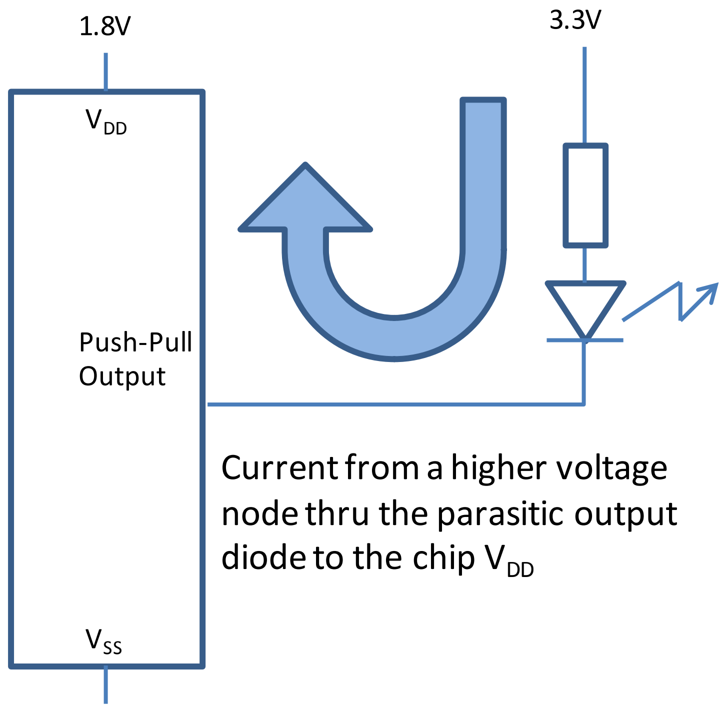

Fig 6. LED drive application showing large current flow caused by LED voltage at 3.3V due to V_f of the LED (approx. 2V) flowing to the lower VDD of the driving device through the parasitic diode of the P-channel transistor

4.2 CMOS FET Principles

The output drivers of the Agile I/O devices are simply large n-channel and p-channel MOSFET devices and they behave exactly like generic MOSFET devices Figure_7 . The drain current is limited in the saturation region and is somewhat linear, like a gate voltage controlled resistor, in the linear region. The main difference between the drain current vs. drain voltage graph in Figure_7 and the Agile I/O device is the gate voltage – the Agile I/O device only has two gate voltage states: 0V and $V_{DD.}$

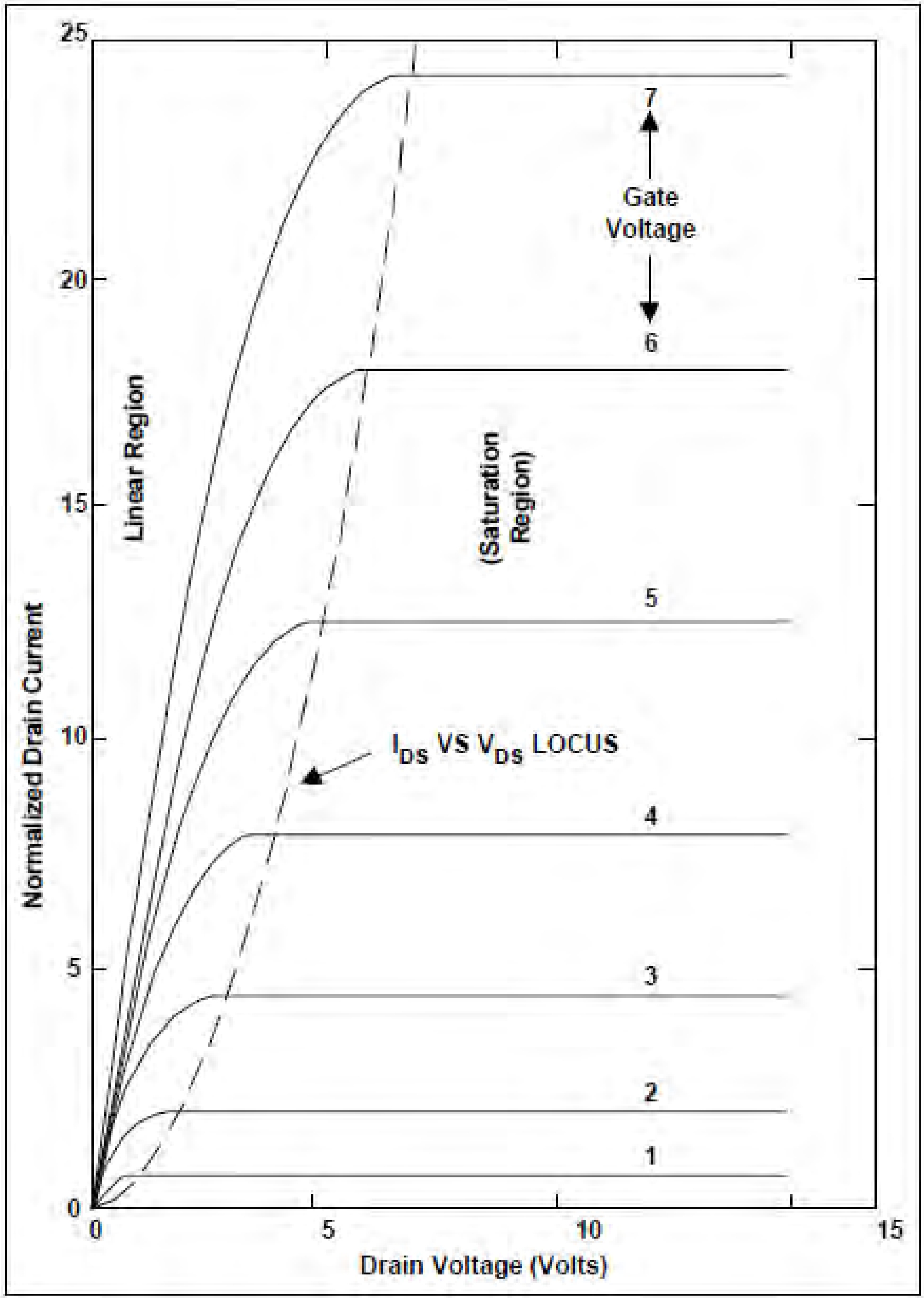

Fig 7. Generic n-channel MOSFET Drain Current vs. Drain Voltage at various Gate Voltages

In the 0V gate voltage state, the n-channel device passes no current from drain to source no matter the drain voltage. In the VDD gate voltage state, the drain current is only limited by the saturation current for that gate voltage – essentially a short circuit at low V_{DS}. An interesting point is the term R_{DSON} or on resistance of the MOSFET. It can be easily calculated graphically by looking at the slope of the device in the linear region. The example device shown in Figure_7, with a gate voltage (V_{GS}) of 7V, the I_{DS} = 20mA at a V_{DS} = 4V which is an R_{DSON} of 200 ohms.

4.3 Actual Agile I/O Output Characteristics

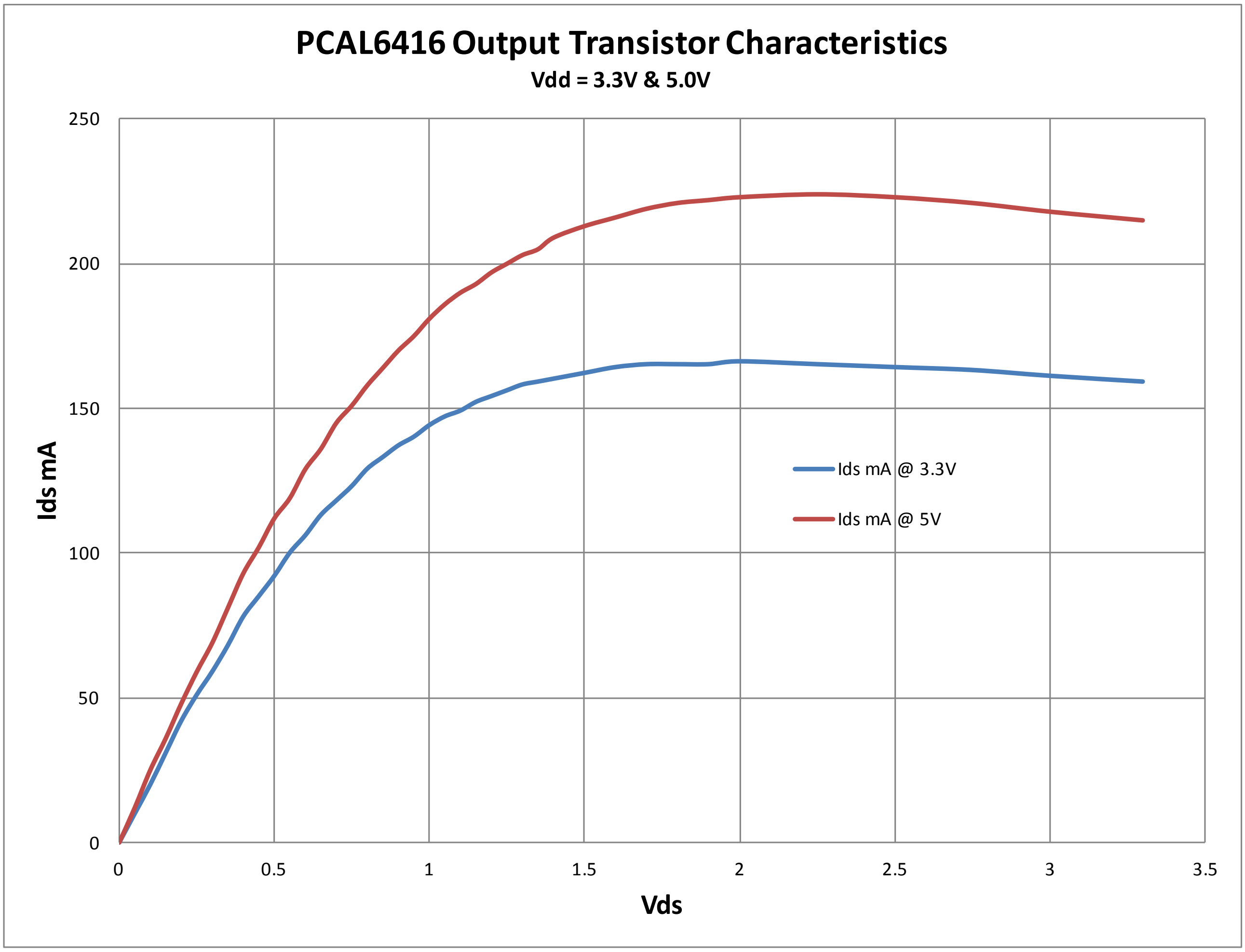

Fig 8. Agile I/O Output Current with V_{DD} (and V_{GS}) at 3.3V and 5V

As stated in the previous section, the output current is only dependent on V_{DD} since V_{GS} is always the same as V_{DD}. Figure_8 shows the n-channel I_{DS} vs V_{DS} curves for an actual Agile I/O device. The saturation current difference is over 50mA, but the RDSON is hardly different in the linear region. Notice the slight decrease in saturation current around 2V to 3.3V. You would expect the saturation current to be constant, but in practice, the current decreases due to self heating of the silicon die from power dissipation across the output transistor – almost 700mW.

4.3.1 Output Drive Strength Control

A novel feature of the Agile I/O devices is the ability to program the size of the output transistors, thereby decreasing their saturation current. Figure 9 shows the p-channel output characteristics and Figure 10 shows an n-channel device of an actual Agile I/O output. The four curves correspond to the four programmable drive levels.

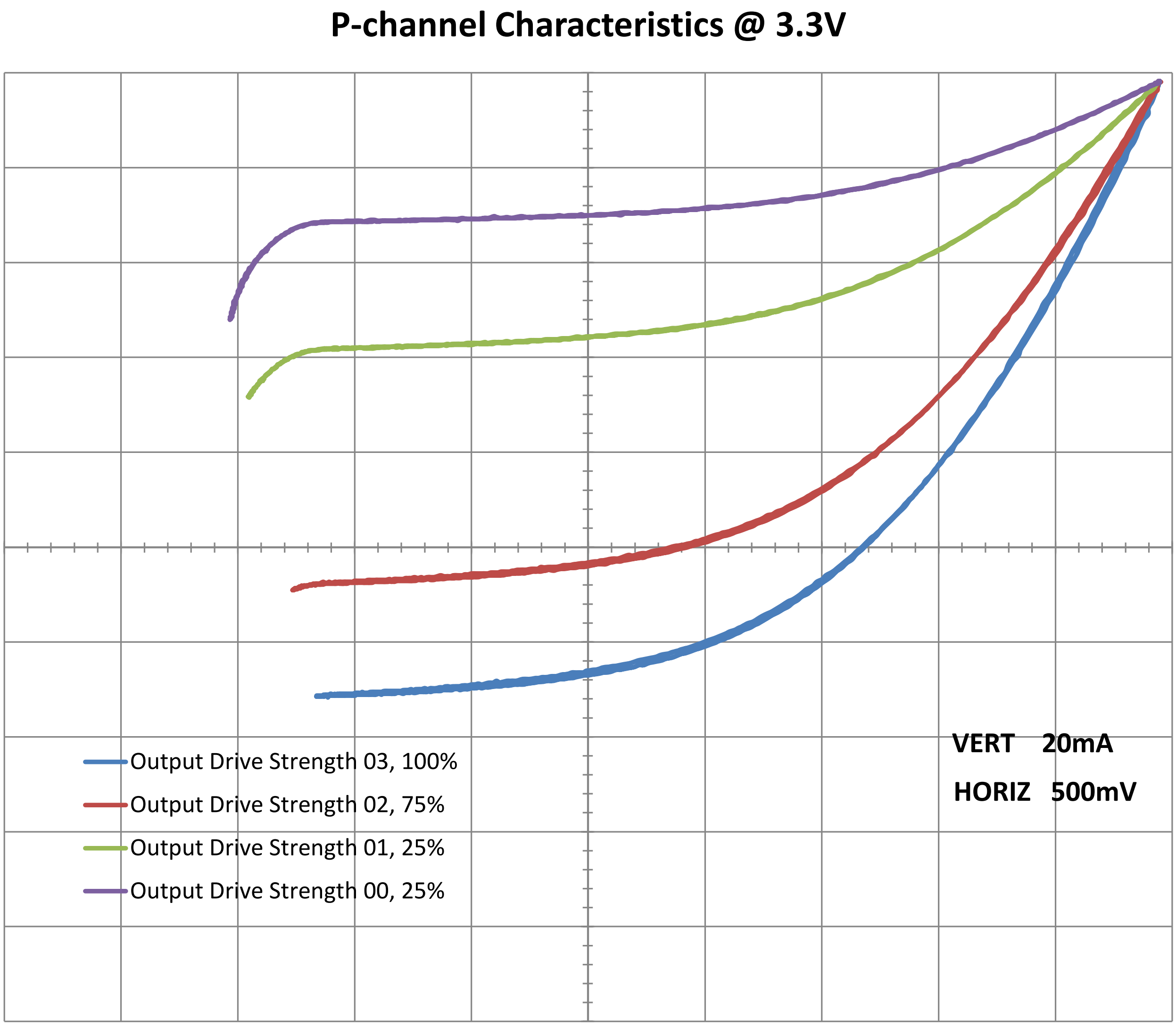

Fig 9. Agile I/O p-channel output transistor with drive strength control

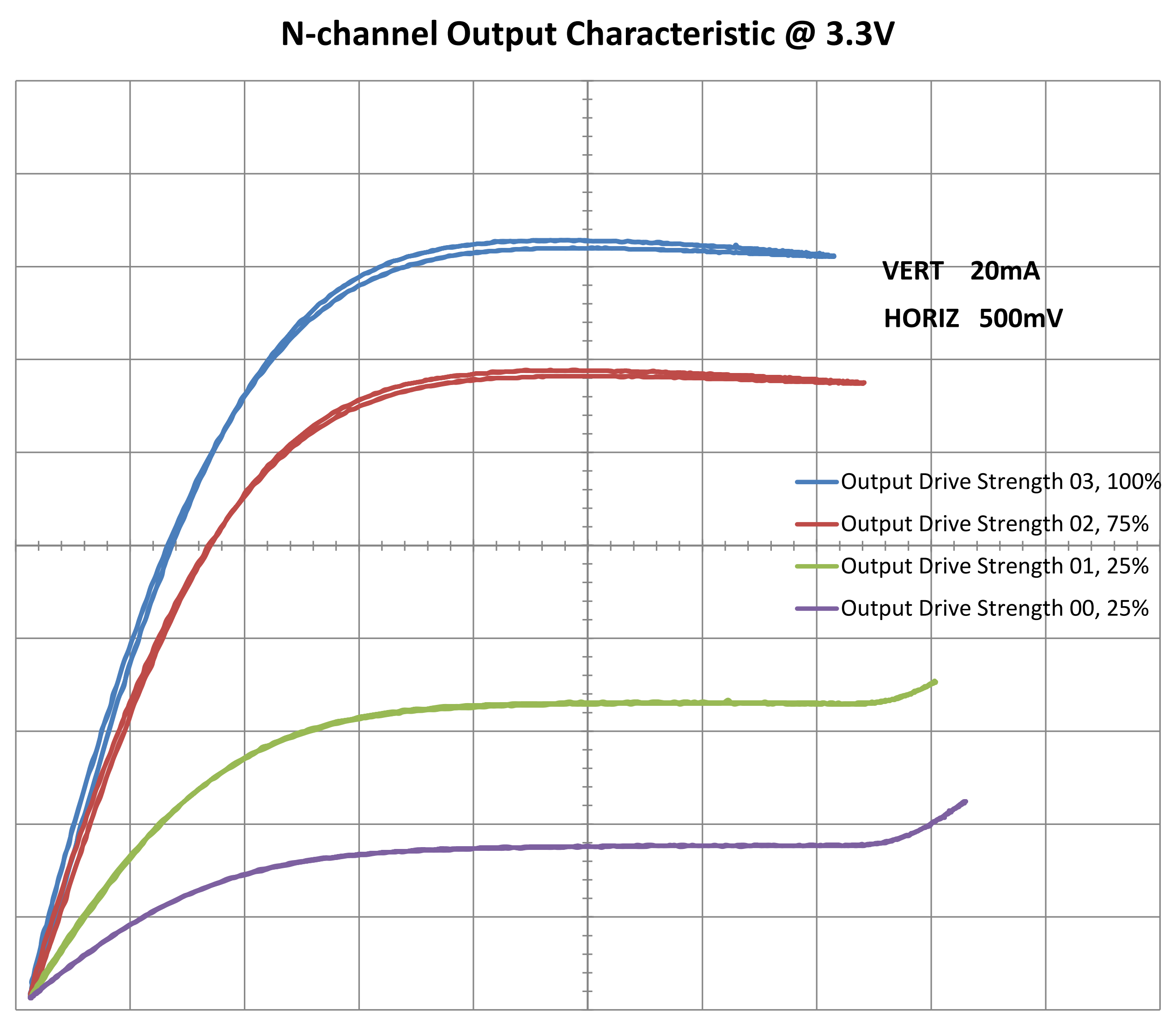

Fig 10. Agile I/O n-channel output transistor with drive strength control

All of this discussion about output drive strength may leave one wondering “why?” But, there is an easy, graphical way to plot the load onto the characteristics and determine the voltage and current delivered to the load and ensure the output transistors are not overtaxed.

First, one must calculate the I-V curve of the load. To simplify this discussion, we’ll use a resistor. This is a linear load with a straight line as a characteristic. A certain voltage across the resistor will draw a current specified by Ohm’s law (I = V / R).

Figure_11 shows a load connected to V_{DD} and switched by the n-channel output transistor. The I – V characteristics are shown next to each component, however there is a twist. Since the resistor is connected between V_{DD} and VDS, the load line is not exactly correct. Zero current flows when V_{DS} equals V_{DD} and maximum current flows when V_{DS} equals V_{SS}. The resistor load line then must be reversed to correctly overlay on the transistor characteristic curve as shown in Figure_12 .

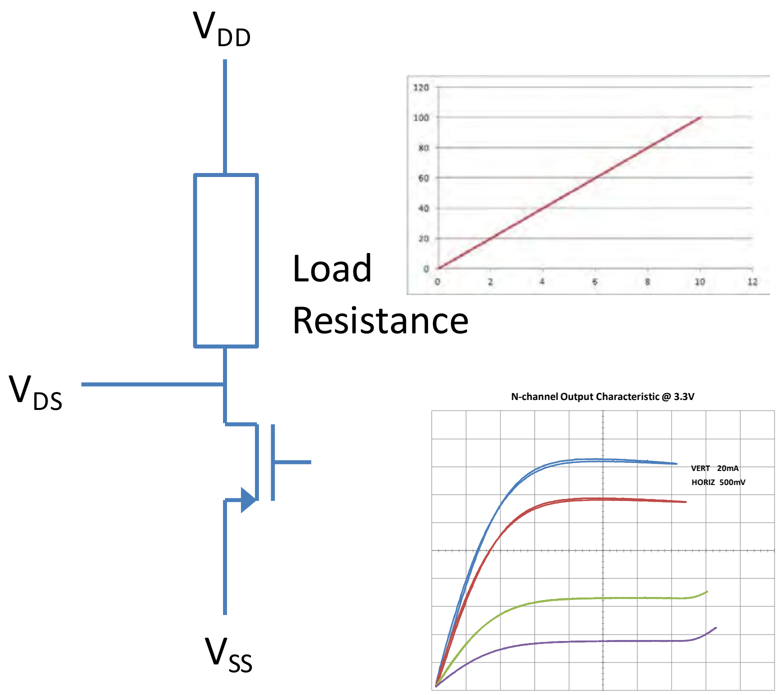

Fig 11. Graphical method for output load design

Figure_12 shows two load lines for this output configuration with resistance of 20 and 200 ohms and completely defines the voltage and current for each resistive load. This graphical method is an easy way to design output drives for complex loads if you have a well behaved and repeatable load line.

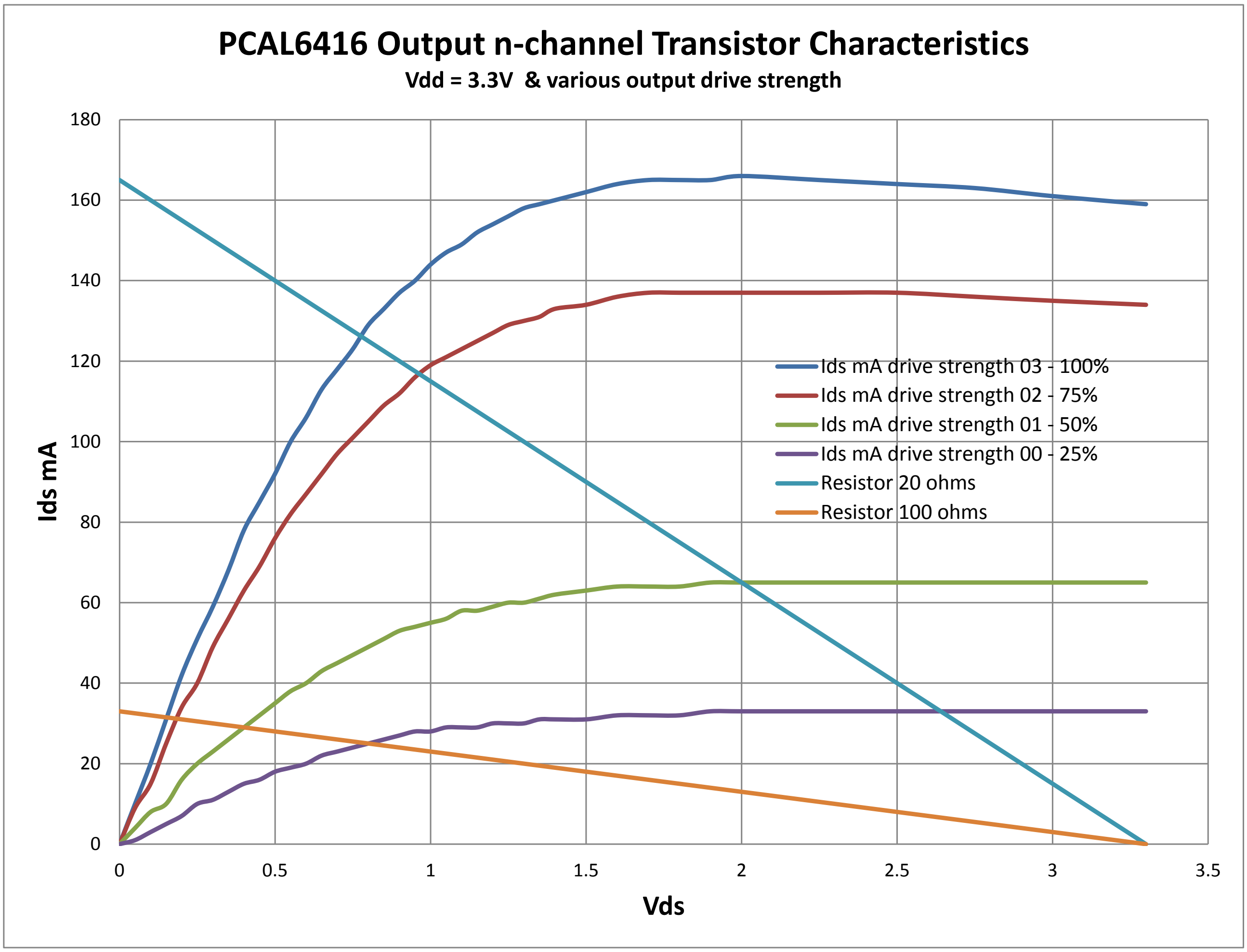

Fig 12. Agile I/O Output transistor characteristic with a resistor load line

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6. List of figures

7. List of tables

8. Contents

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