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CBTL08GP053 Programmer's Guide

Rev. 1 — 18 June 2015   **Application note**

Revision history

Rev	Date	Description
1	20150618	Initial release

Contact information

For more information, please visit: http://www.nxp.com

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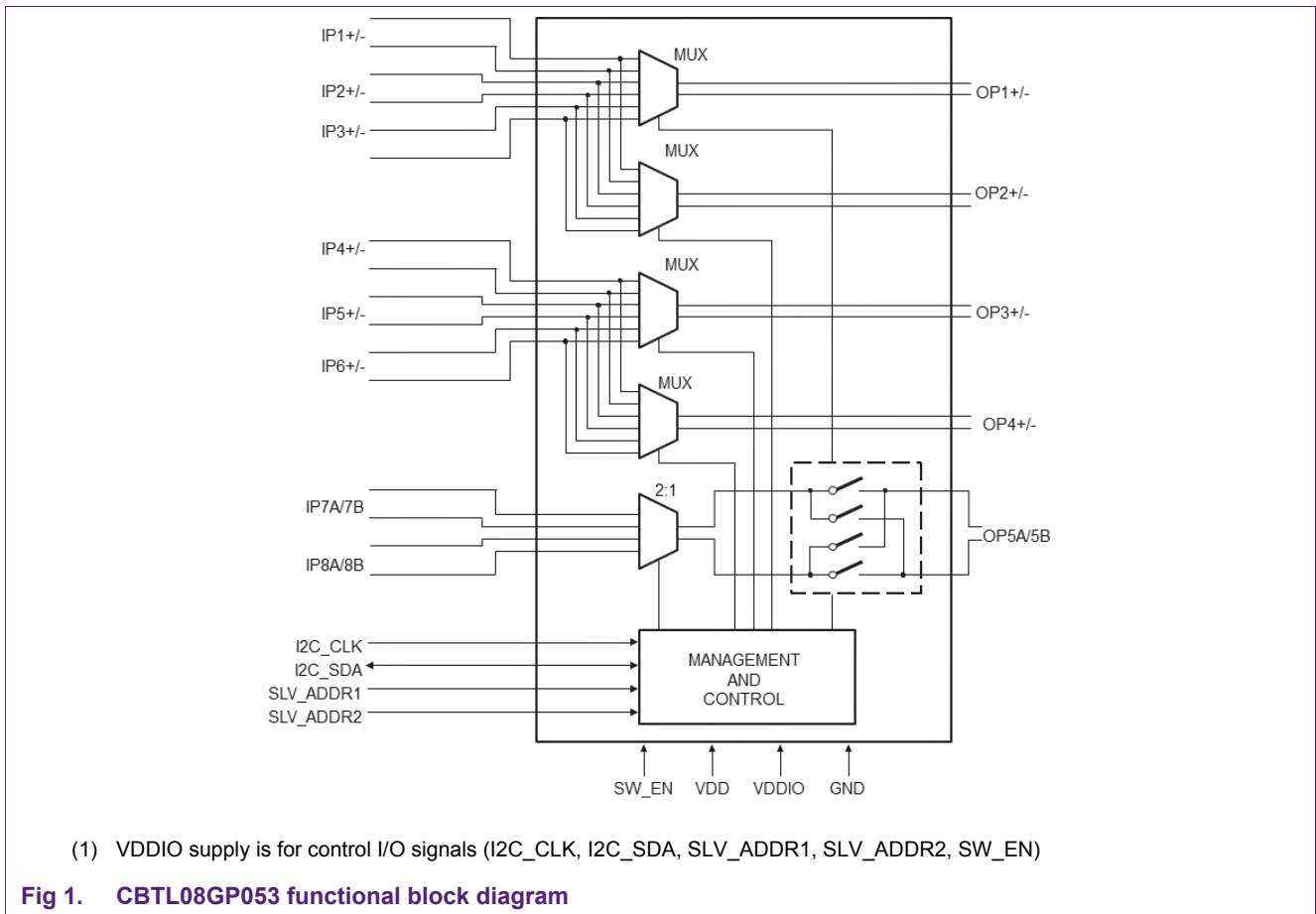
1. Introduction

The CBTL08GP053 is a high performance integrated circuit (IC) capable of switching high-speed differential signals in a variety of USB Type-C systems. The CBTL08GP053 device allows a variety of system side signals to interface with USB Type-C connectors, including:

- USB 3.1
- DisplayPort 1.3 and DP++
- PCIe 3.0
- Differential AUX or single-ended signals (UART, I^{2}C, etc.)

The CBTL08GP053 is controllable via an I^{2}C interface and can be used with downward facing ports (DFP) or upward facing ports (UFP) in laptop and desktop PCs, tablets, smartphones, display monitors, and other peripherals or accessories containing a USB Type-C connector. All of the functionality is available in a low power and space-saving VFBGA package. Please refer to CBTL08GP053 datasheet [1] for more details.

2. CBTL08GP053 description

Fig 1 is the functional block diagram of the CBTL08GP053.

(1) VDDIO supply is for control I/O signals (I2C_CLK, I2C_SDA, SLV_ADDR1, SLV_ADDR2, SW_EN)

Fig 1.   CBTL08GP053 functional block diagram

The CBTL08GP053 contains four high-speed 3:1 multiplexers to support bidirectional high-speed differential signaling up to 8 GHz. There is also a single 2:1 multiplexer with a full crossbar switch to support bidirectional differential and single-ended signals up to 750 MHz. Typically OP1 to OP5 are connected to the USB Type-C connector while IP1 to IP8 along with the I^{2}C-bus signals (I2C_CLK, I2C_SDA) are connected to the local system.

2.1 I^{2}C Interface

CBTL08GP053 supports a maximum of four I^{2}C-bus slave address options. The 7-bit address is selected through the SLV_ADDR1 and SLV_ADDR2 pins. Table 1 shows the different I^{2}C-bus device address options based on pin values.

Table 1. CBTL08GP053 slave addresses

SLV_ADDR2	SLV_ADDR1	I^{2}C-bus device address (write/read)
LOW	LOW	0x60/0x61
LOW	HIGH	0x64/0x65
HIGH	LOW	0x68/0x69
HIGH	HIGH	0x6C/0x6D

CBTL08GP053 supports data transfers at both Standard-mode (100 kHz) and Fast-mode (400 kHz) clock rates as defined in the I^{2}C-bus specification (see UM10204). An example of a typical I^{2}C write and read sequence is shown in Fig 2. Please refer to CBTL08GP053 datasheet for complete list of supported I^{2}C-bus transactions.
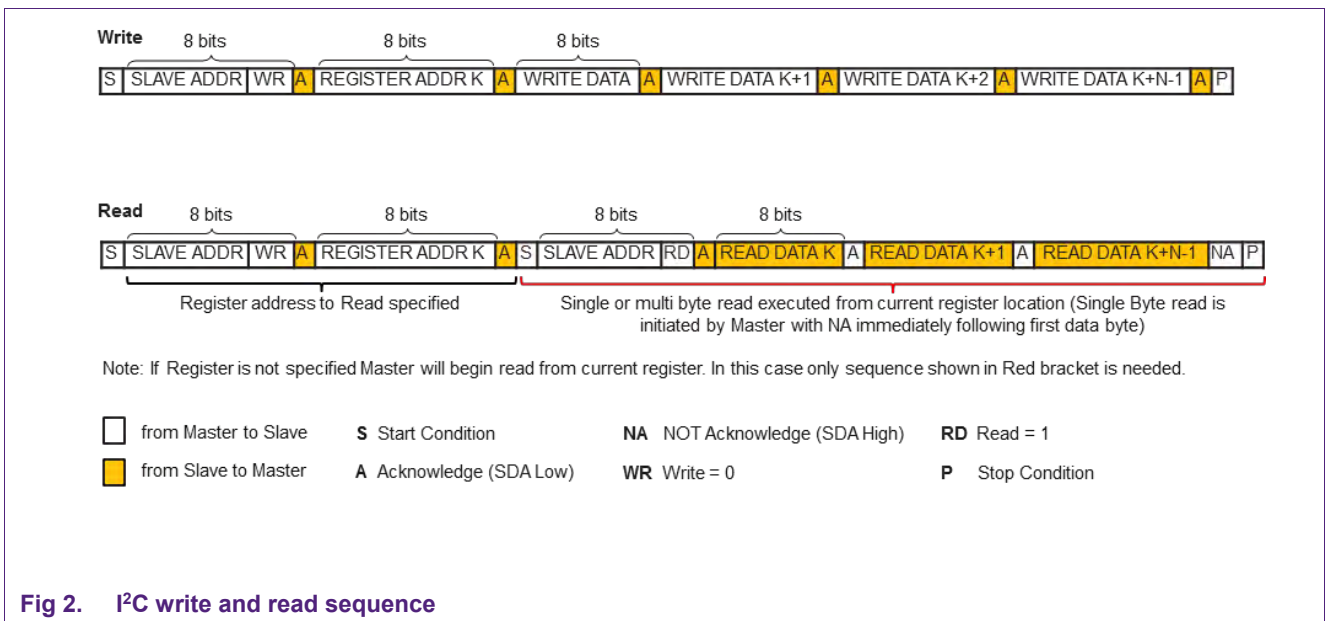

Fig 2. I^{2}C write and read sequence

2.2 Operating modes

The register map for CBTL08GP053 is presented in Table 2. After power up, the default register values initialize the device in a lower power standby mode where all signal pathways are not connected (Hi-Z state). I^{2}C write commands are then required to put

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the device into active mode operation with a valid switch configuration for a specific customer application scenario.

Table 2.   CBTL08GP053 Register Map
'R'- Read only register, 'W'-Write only register, 'RW' – Read/Write register

Address Offset	Register Name	Access	Default POR Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x01	SYS_CTRL	RW	0x00	SWITCH_EN							
0x02	OP1_CTRL	RW	0x00						IP3	IP2	IP1
0x03	OP2_CTRL	RW	0x00						IP3	IP2	IP1
0x04	OP3_CTRL	RW	0x00			IP6	IP5	IP4			
0x05	OP4_CTRL	RW	0x00			IP6	IP5	IP4			
0x06	OP5_CTRL	RW	0x00	IP8	IP7						
0x07	CROSS5_CTRL	RW	0x01							CROSS	PASS
0x08	SW_CTRL	W	0x00			X5_SET	OP5_SET	OP4_SET	OP3_SET	OP2_SET	OP1_SET
0x09	REVISION	R	0xA0	REVISION ID							
0x0A to 0xFF	Reserved	-	-	RESERVED							

[1]   Reserved bit fields are shaded. Reads will be zeros and writes do not have any effect.

CBTL08GP053 active mode operation requires that both the SW_EN pin be set to logical "high" voltage level and the SWITCH_EN bit (SYS_CTRL[7]) set to '1'. Subsequent changes to either the SW_EN pin or the SWITCH_EN bit will return the device to standby condition but the remaining register contents will remain unchanged. Please refer to CBTL08GP053 datasheet for start-up time ($t_{startup}$) characteristics when switching between standby and active modes of operation.

During active mode operation the customer application may want to change the switch configuration using an I^{2}C write command to the SW_CTRL register. A reconfiguration time interval (t_{rcfg}) from the final I^{2}C clock bit is required before the switch starts operating with the new settings.

Note: Usually OP1_CTRL, OP2_CTRL, OP3_CTRL, OP4_CTRL, OP5_CTRL, and CROSS5_CTRL should be preloaded with required and valid settings before writing to SW_CTRL.

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3. Application Use Cases: DisplayPort Alt Mode for USB Type-C

CBTL08GP053 is ideally suited for applications where a variety of different high-speed signals have to be routed over a single connector. One major application example is using DisplayPort as an Alternate Mode for USB Type-C connectors. This specification [2] defines the connectivity between the USB Type-C receptacle pinout and DisplayPort (DP) high-speed signals along with the number of lanes and signaling rates for various scenarios. The DP Alt Mode standard also specifies the pin configurations for both downward facing ports (DFP) and upward facing ports (UFP). DFP are typically found in host systems such as laptop/desktop PCs and tablets while UFP are located in peripheral systems such as display monitors and docks. Please contact NXP for examples of application reference designs for both DFP and UFP Type-C systems.

Fig 3 shows the front view of a DFP or UFP USB Type-C receptacle. There are four high-speed differential pairs (TX1+/-, TX2+/-, RX1+/-, RX2+/-) that support DP 1.3 data signaling rates. In addition SBU1 and SBU2 are lower bandwidth pathways that can be used for DP AUX signaling. USB 2.0 traffic is carried by the D+/- signals while the remaining signals (VBUS, CC1, CC2, GND) must support and be compatible with the USB Power Delivery (PD) specification [3] and Universal Serial Bus Type-C Cable and Connector Specification [4].

A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2	D-	D+	CC2	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

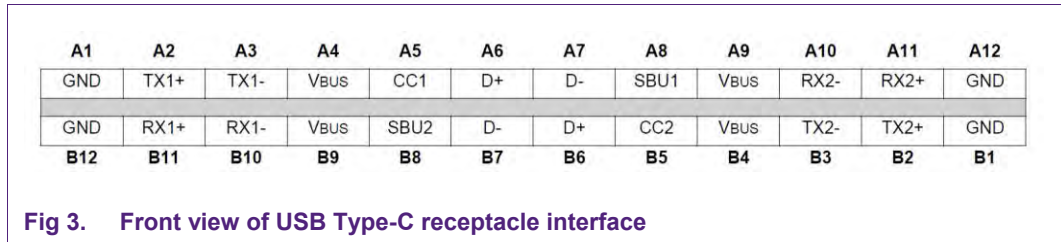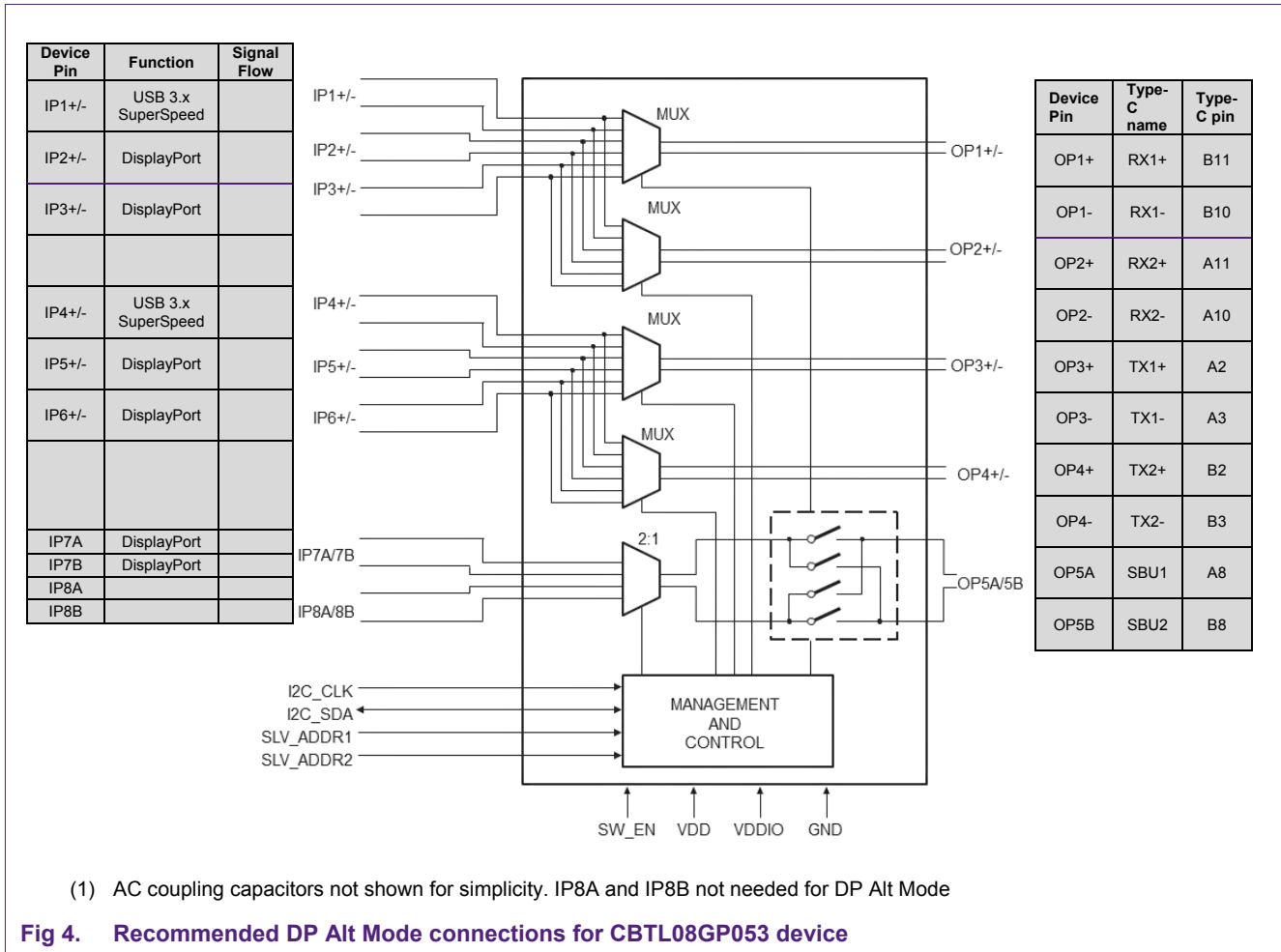**Fig 3.** **Front view of USB Type-C receptacle interface**

Table 3 lists the DP Alt Mode usage cases supported by the CBTL08GP053. Please refer to DP Alt Mode specification [2] and the CBTL08GP053 datasheet for more details.

Table 3. **CBTL08GP053 for DisplayPort Alt Mode**

DP Alt Mode Pin Assignment	USB type-C plug orientation	Number of DisplayPort lanes	USB 3.x SuperSpeed
DFP pin Assignment C (and E)	Normal	4	-
"	Flipped	4	-
DFP pin Assignment D (and F)	Normal	2	Active
"	Flipped	2	Active
UFP pin Assignment C	Normal	4	-
"	Flipped	4	-
UFP pin Assignment D	Normal	2	Active
"	Flipped	2	Active
UFP pin Assignment E	Normal	4	-
"	Flipped	4	-

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The CBTL08GP053 is a versatile high performance switch that can be used in a variety of configurations and applications. A recommended connection to support most DP Alt Mode usage cases is presented in Fig 4. The described interface between a USB Type-C receptacle and CBTL08GP053 is valid for both DFP and UFP applications. The recommended pinout maintains good signal integrity in the printed circuit board (PCB) layout by minimizing signal transitions for the high-speed signal pathways.

(1) AC coupling capacitors not shown for simplicity. IP8A and IP8B not needed for DP Alt Mode

Fig 4.   Recommended DP Alt Mode connections for CBTL08GP053 device

The various DP Alt Mode usage cases will be shown in the following sections with the associated CBTL08GP053 register maps and signal flow direction based on the above implementation. If a different connectivity is used the software and firmware should adjust the CBTL08GP053 settings accordingly. Please refer to CBTL08GP053 datasheet for more information.

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3.1 DFP Pin Assignment C (and E)
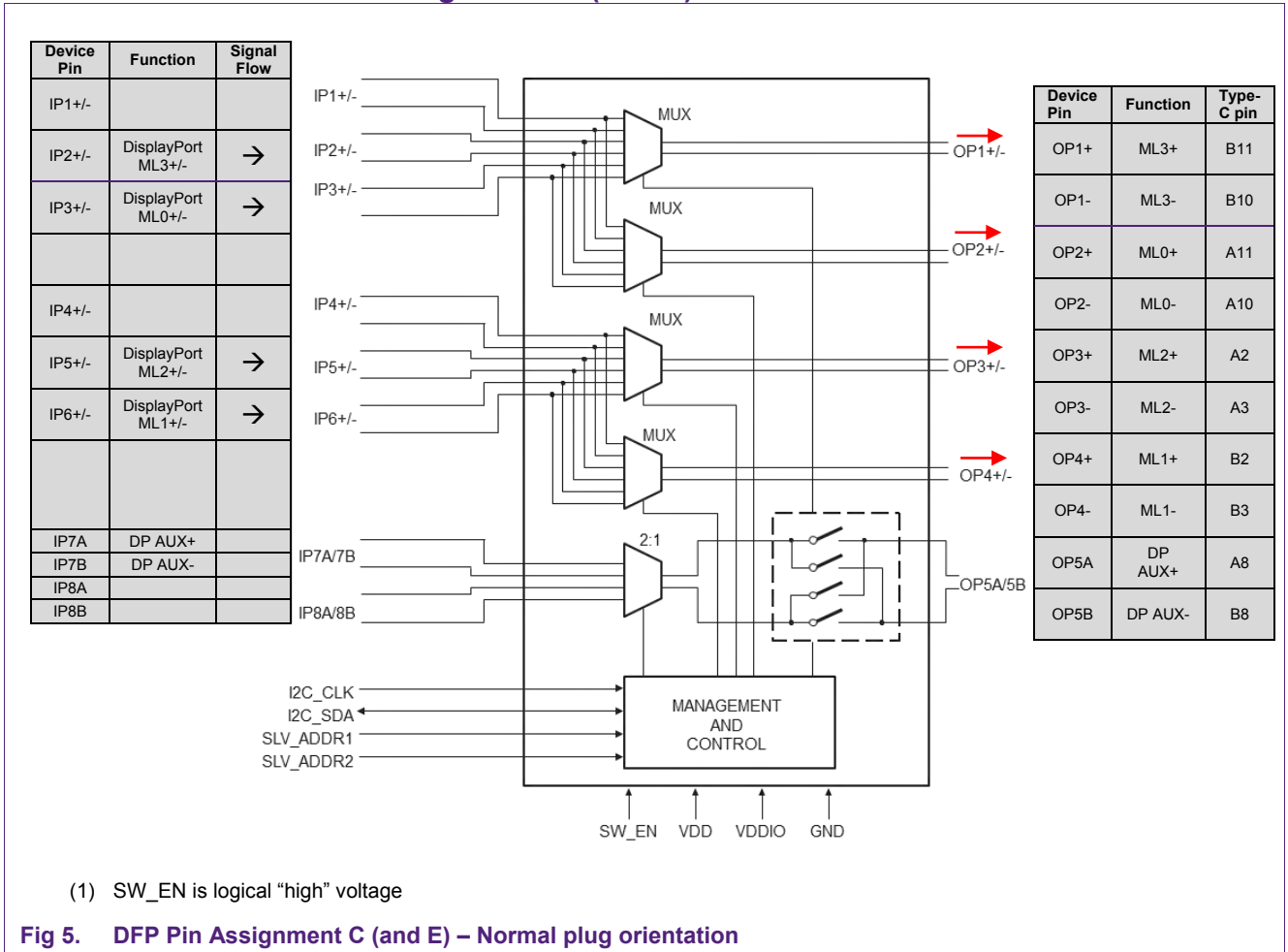

(1) SW_EN is logical "high" voltage

Fig 5. DFP Pin Assignment C (and E) – Normal plug orientation

Table 4. Register Map: DFP Pin Assignment C (and E) – Normal plug orientation
Reserved bit fields are shaded. Reads will be zeros and writes do not have any effect

Address Offset	Register Name	Access	Hex Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x01	SYS_CTRL	RW	0x80	1							
0x02	OP1_CTRL	RW	0x02						0	1	0
0x03	OP2_CTRL	RW	0x04						1	0	0
0x04	OP3_CTRL	RW	0x10			0	1	0			
0x05	OP4_CTRL	RW	0x20			1	0	0			
0x06	OP5_CTRL	RW	0x40	0	1						
0x07	CROSS5_CTRL	RW	0x01							0	1
0x08	SW_CTRL	W	0x3F			1	1	1	1	1	1

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(1) SW_EN is logical "high" voltage

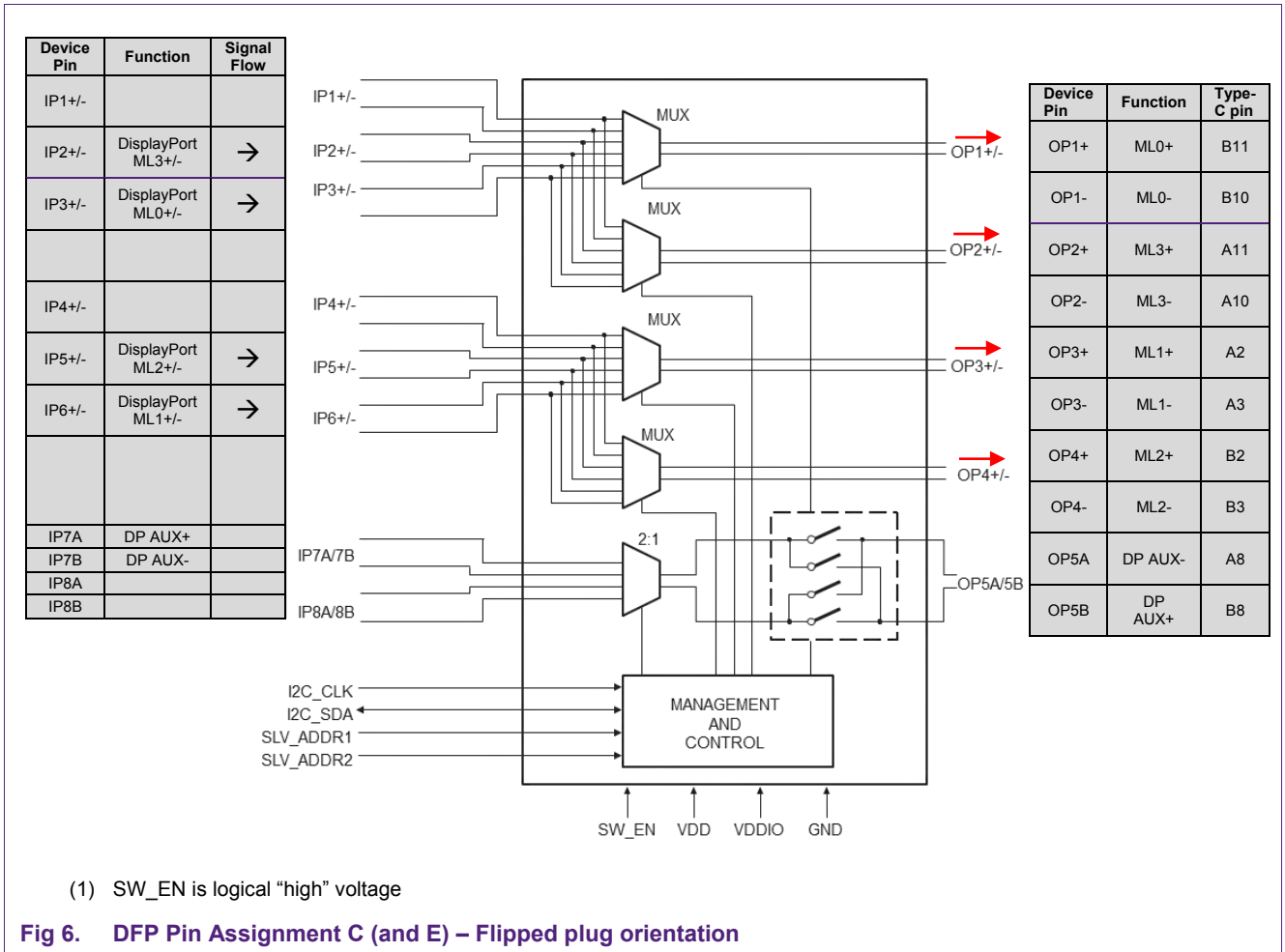**Fig 6.   DFP Pin Assignment C (and E) – Flipped plug orientation**

Table 5.   Register Map: DFP Pin Assignment C (and E) – Flipped plug orientation
Reserved bit fields are shaded. Reads will be zeros and writes do not have any effect

Address Offset	Register Name	Access	Hex Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x01	SYS_CTRL	RW	0x80	1							
0x02	OP1_CTRL	RW	0x04						1	0	0
0x03	OP2_CTRL	RW	0x02						0	1	0
0x04	OP3_CTRL	RW	0x20			1	0	0			
0x05	OP4_CTRL	RW	0x10			0	1	0			
0x06	OP5_CTRL	RW	0x40	0	1						
0x07	CROSS5_CTRL	RW	0x02							1	0
0x08	SW_CTRL	W	0x3F			1	1	1	1	1	1

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3.2 DFP Pin Assignment D (and F)

(1) SW_EN is logical "high" voltage

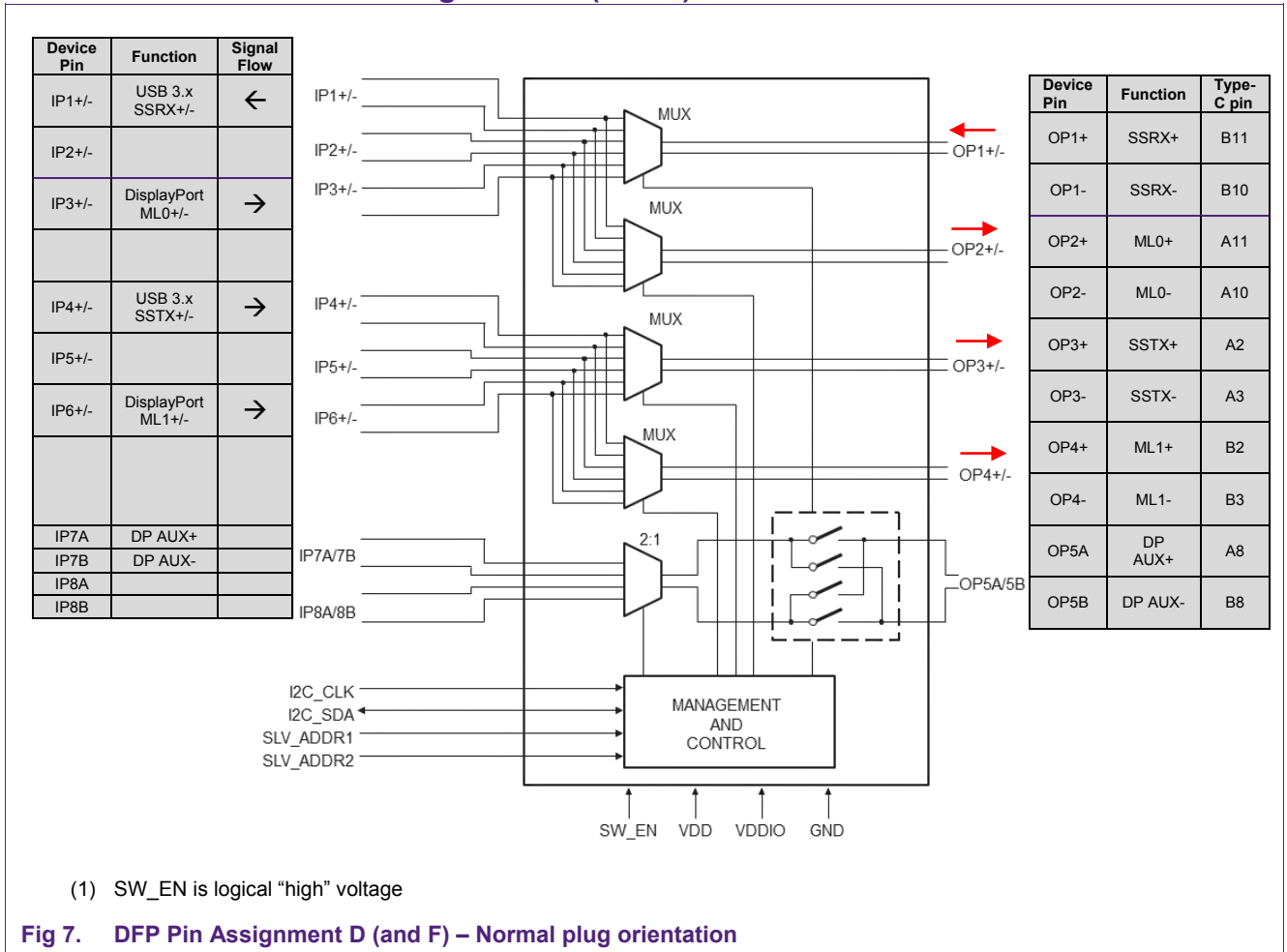**Fig 7.** **DFP Pin Assignment D (and F) – Normal plug orientation**

Table 6. **Register Map: DFP Pin Assignment D (and F) – Normal plug orientation**
Reserved bit fields are shaded. Reads will be zeros and writes do not have any effect

Address Offset	Register Name	Access	Hex Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x01	SYS_CTRL	RW	0x80	1							
0x02	OP1_CTRL	RW	0x01						0	0	1
0x03	OP2_CTRL	RW	0x04						1	0	0
0x04	OP3_CTRL	RW	0x08			0	0	1			
0x05	OP4_CTRL	RW	0x20			1	0	0			
0x06	OP5_CTRL	RW	0x40	0	1						
0x07	CROSS5_CTRL	RW	0x01							0	1
0x08	SW_CTRL	W	0x3F			1	1	1	1	1	1

(1)   SW_EN is logical "high" voltage

Fig 8.   DFP Pin Assignment D (and F) – Flipped plug orientation
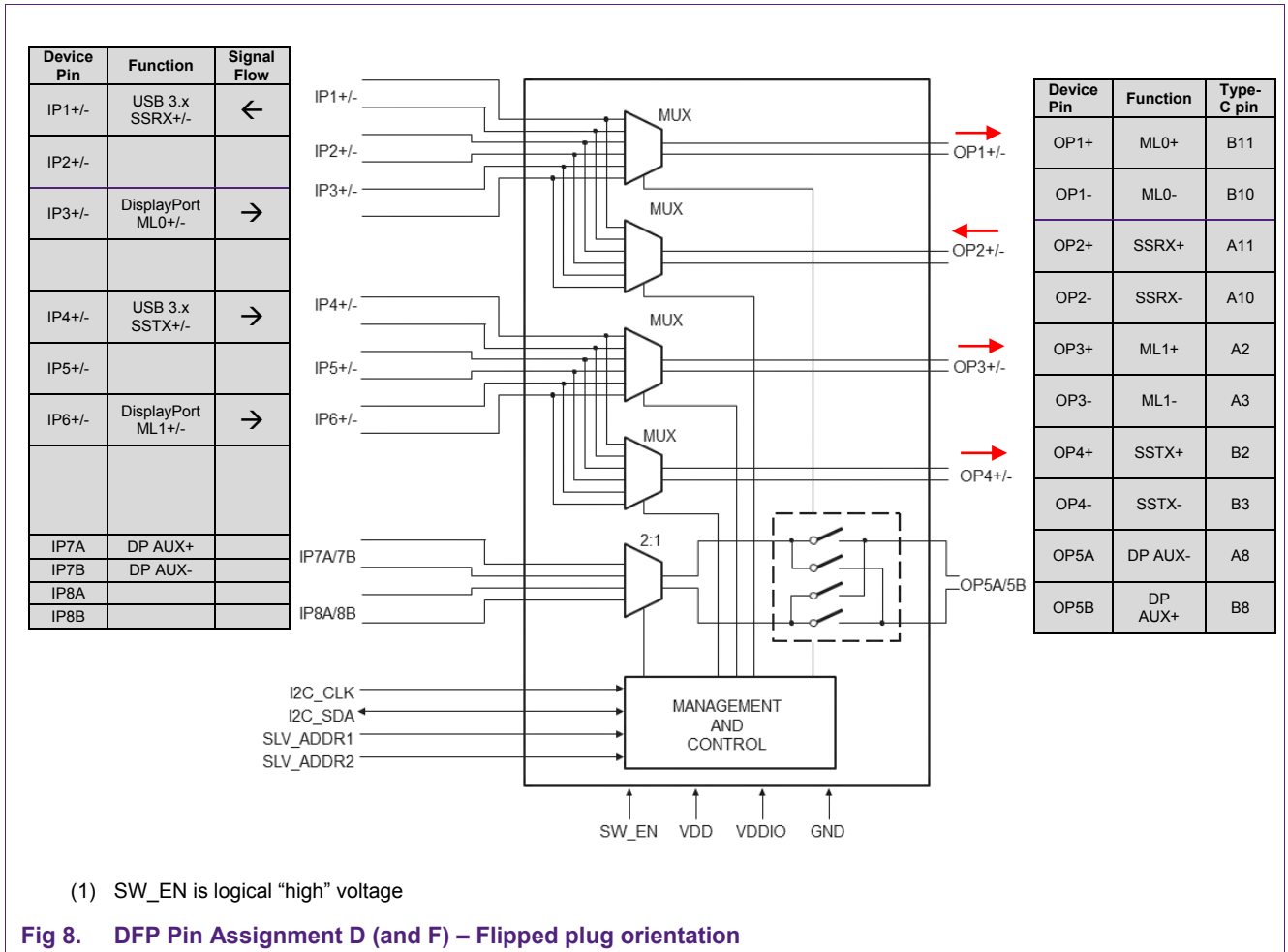
Table 7.   Register Map: DFP Pin Assignment D (and F) – Flipped plug orientation
Reserved bit fields are shaded. Reads will be zeros and writes do not have any effect

Address Offset	Register Name	Access	Hex Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x01	SYS_CTRL	RW	0x80	1							
0x02	OP1_CTRL	RW	0x04						1	0	0
0x03	OP2_CTRL	RW	0x01						0	0	1
0x04	OP3_CTRL	RW	0x20			1	0	0			
0x05	OP4_CTRL	RW	0x08			0	0	1			
0x06	OP5_CTRL	RW	0x40	0	1						
0x07	CROSS5_CTRL	RW	0x02							1	0
0x08	SW_CTRL	W	0x3F			1	1	1	1	1	1

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3.3   UFP Pin Assignment C

(1)   SW_EN is logical "high" voltage

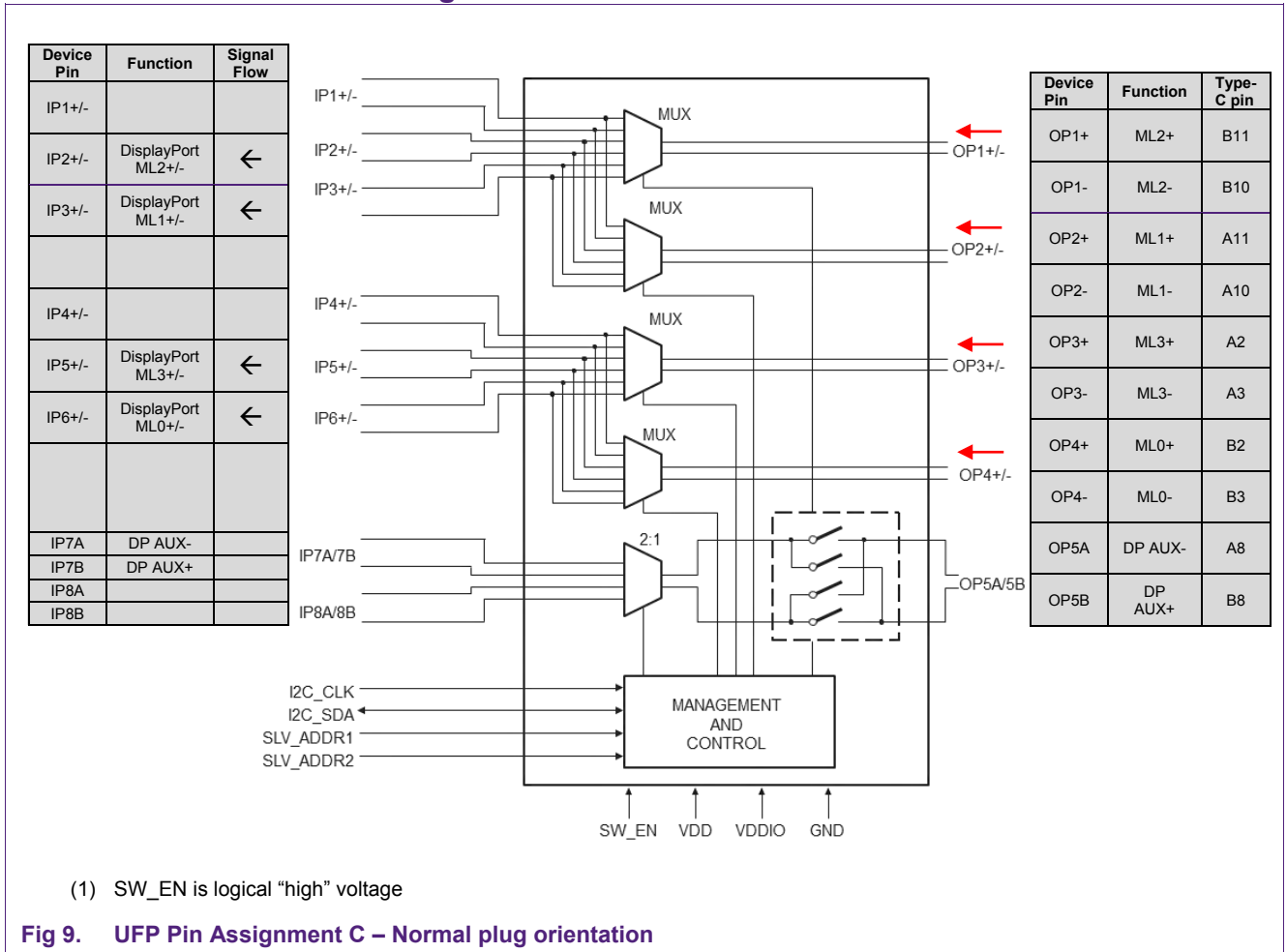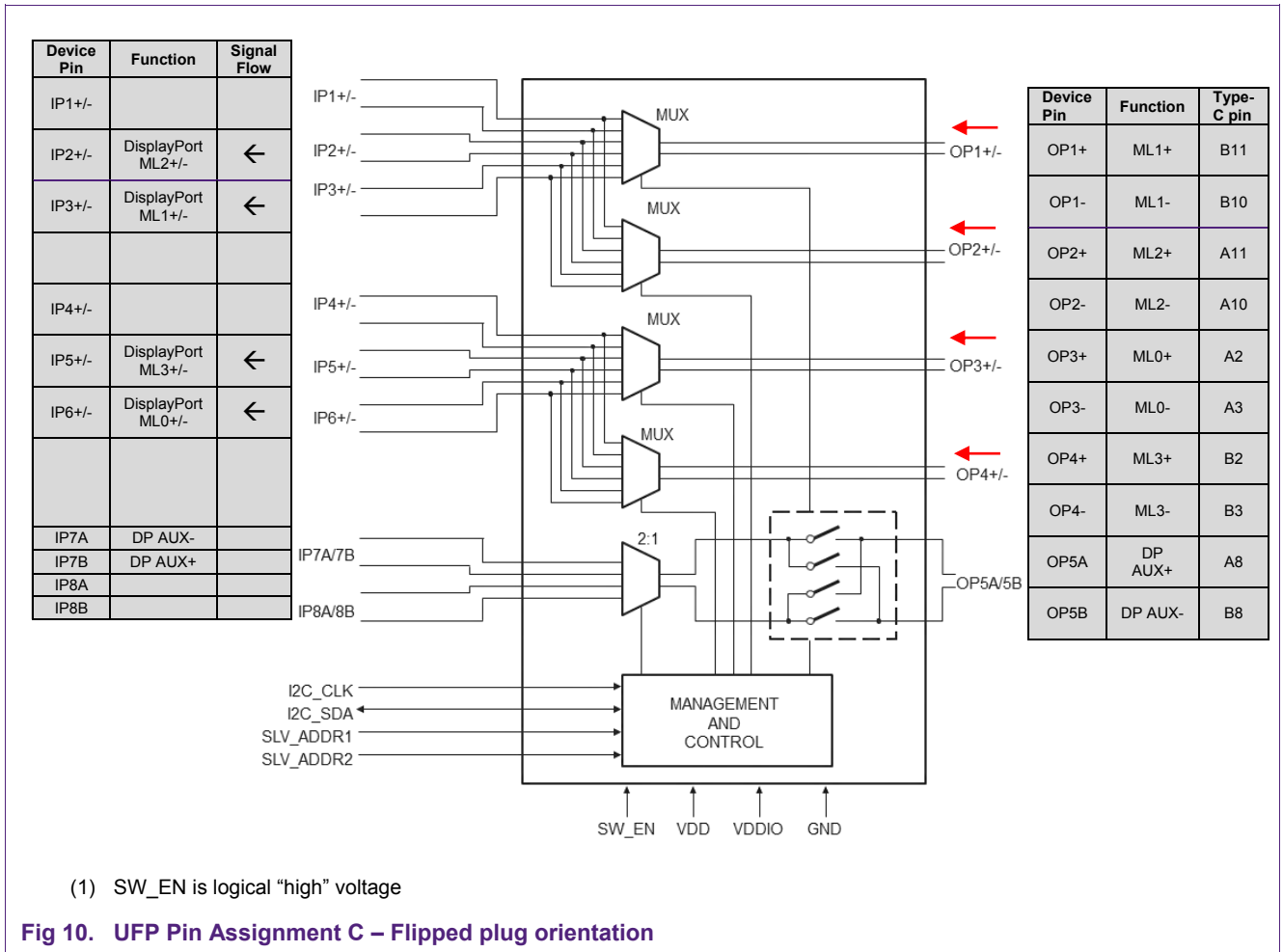**Fig 9.**   **UFP Pin Assignment C – Normal plug orientation**

Table 8.   **Register Map: UFP Pin Assignment C – Normal plug orientation**
Reserved bit fields are shaded. Reads will be zeros and writes do not have any effect

Address Offset	Register Name	Access	Hex Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x01	SYS_CTRL	RW	0x80	1							
0x02	OP1_CTRL	RW	0x02						0	1	0
0x03	OP2_CTRL	RW	0x04						1	0	0
0x04	OP3_CTRL	RW	0x10			0	1	0			
0x05	OP4_CTRL	RW	0x20			1	0	0			
0x06	OP5_CTRL	RW	0x40	0	1						
0x07	CROSS5_CTRL	RW	0x01							0	1
0x08	SW_CTRL	W	0x3F			1	1	1	1	1	1

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Device Pin	Function	Signal Flow
IP1+/-		
IP2+/-	DisplayPort ML2+/-	←
IP3+/-	DisplayPort ML1+/-	←
IP4+/-		
IP5+/-	DisplayPort ML3+/-	←
IP6+/-	DisplayPort ML0+/-	←
IP7A	DP AUX-	
IP7B	DP AUX+	
IP8A		
IP8B		

Device Pin	Function	Type-C pin
OP1+	ML1+	B11
OP1-	ML1-	B10
OP2+	ML2+	A11
OP2-	ML2-	A10
OP3+	ML0+	A2
OP3-	ML0-	A3
OP4+	ML3+	B2
OP4-	ML3-	B3
OP5A	DP AUX+	A8
OP5B	DP AUX-	B8

(1) SW_EN is logical "high" voltage

Fig 10. UFP Pin Assignment C – Flipped plug orientation

Table 9. Register Map: UFP Pin Assignment C – Flipped plug orientation
Reserved bit fields are shaded. Reads will be zeros and writes do not have any effect

Address Offset	Register Name	Access	Hex Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x01	SYS_CTRL	RW	0x80	1							
0x02	OP1_CTRL	RW	0x04						1	0	0
0x03	OP2_CTRL	RW	0x02						0	1	0
0x04	OP3_CTRL	RW	0x20			1	0	0			
0x05	OP4_CTRL	RW	0x10			0	1	0			
0x06	OP5_CTRL	RW	0x40	0	1						
0x07	CROSS5_CTRL	RW	0x02							1	0
0x08	SW_CTRL	W	0x3F			1	1	1	1	1	1

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3.4 UFP Pin Assignment D

(1) SW_EN is logical "high" voltage

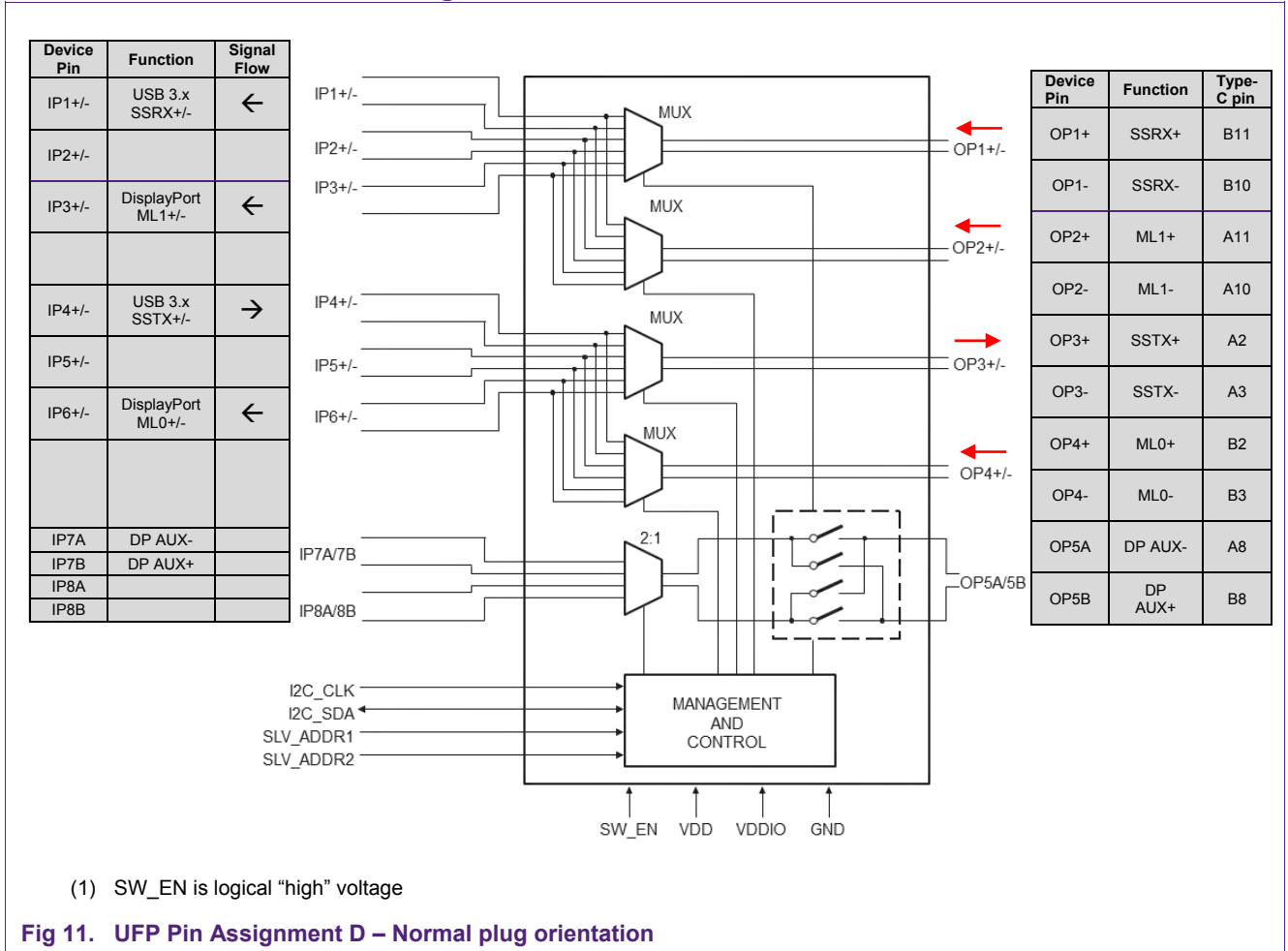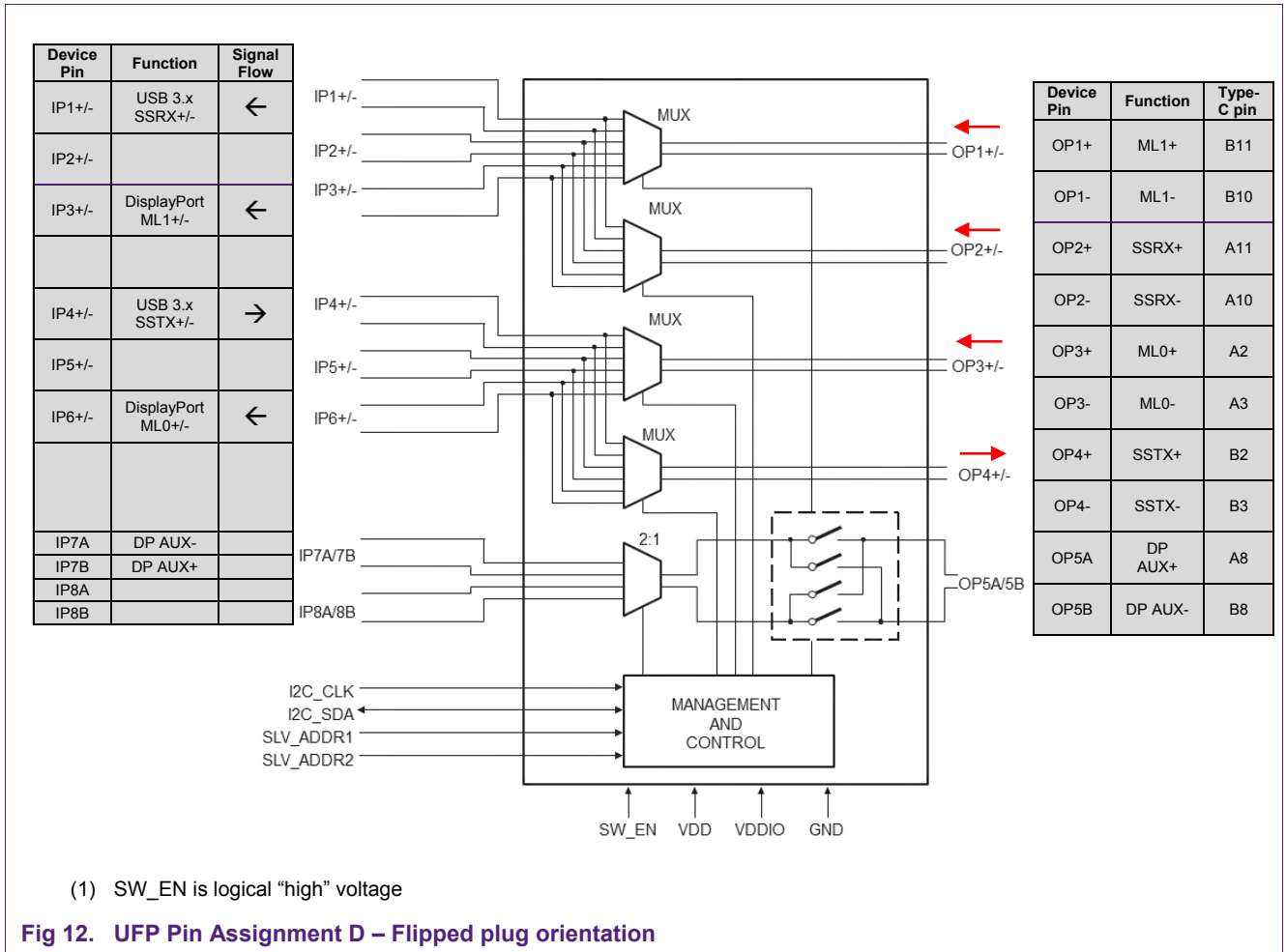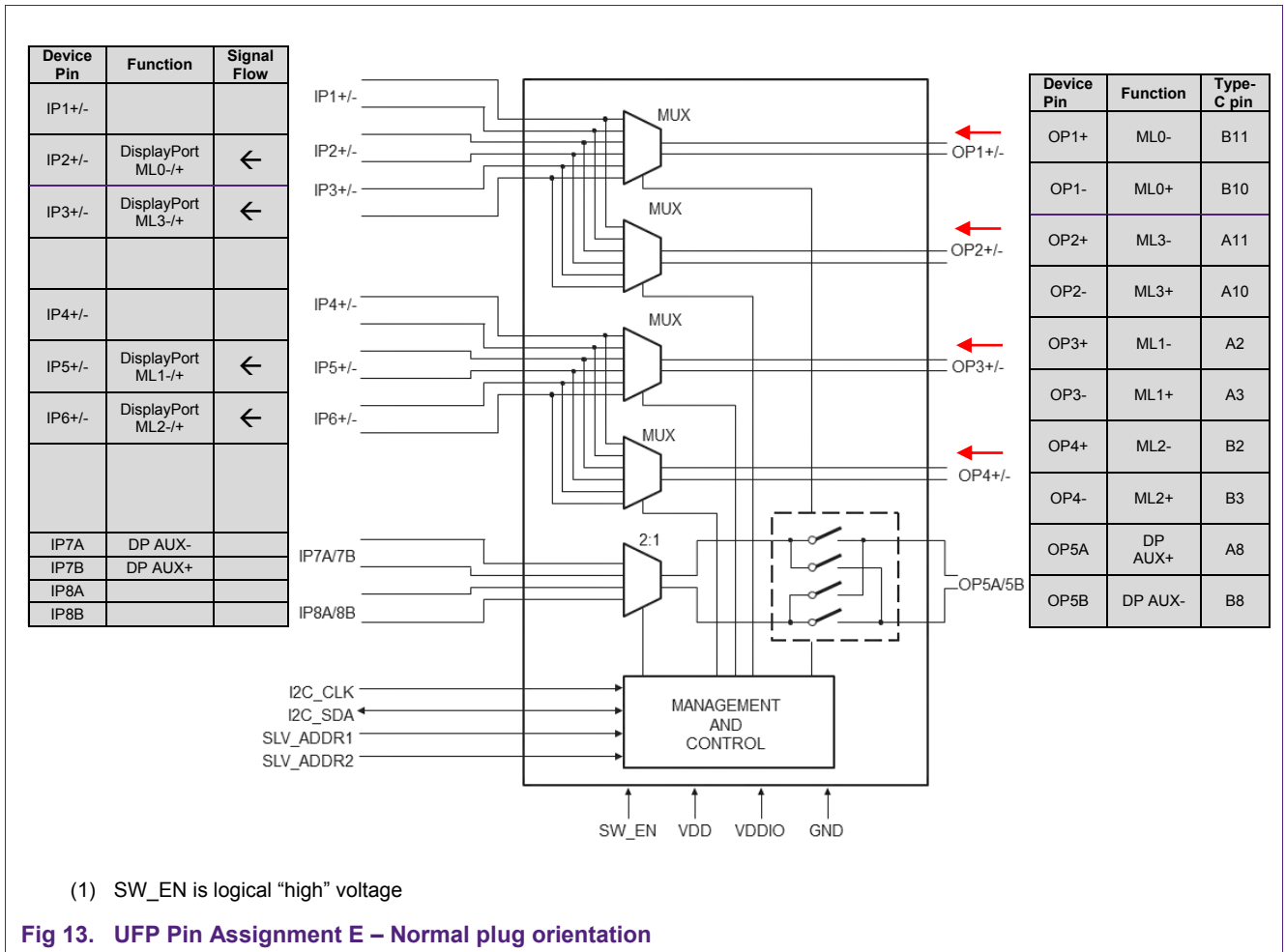**Fig 11. UFP Pin Assignment D – Normal plug orientation**

Table 10. Register Map: UFP Pin Assignment D – Normal plug orientation
Reserved bit fields are shaded. Reads will be zeros and writes do not have any effect

Address Offset	Register Name	Access	Hex Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x01	SYS_CTRL	RW	0x80	1							
0x02	OP1_CTRL	RW	0x01						0	0	1
0x03	OP2_CTRL	RW	0x04						1	0	0
0x04	OP3_CTRL	RW	0x08			0	0	1			
0x05	OP4_CTRL	RW	0x20			1	0	0			
0x06	OP5_CTRL	RW	0x40	0	1						
0x07	CROSS5_CTRL	RW	0x01							0	1
0x08	SW_CTRL	W	0x3F			1	1	1	1	1	1

(1) SW_EN is logical "high" voltage

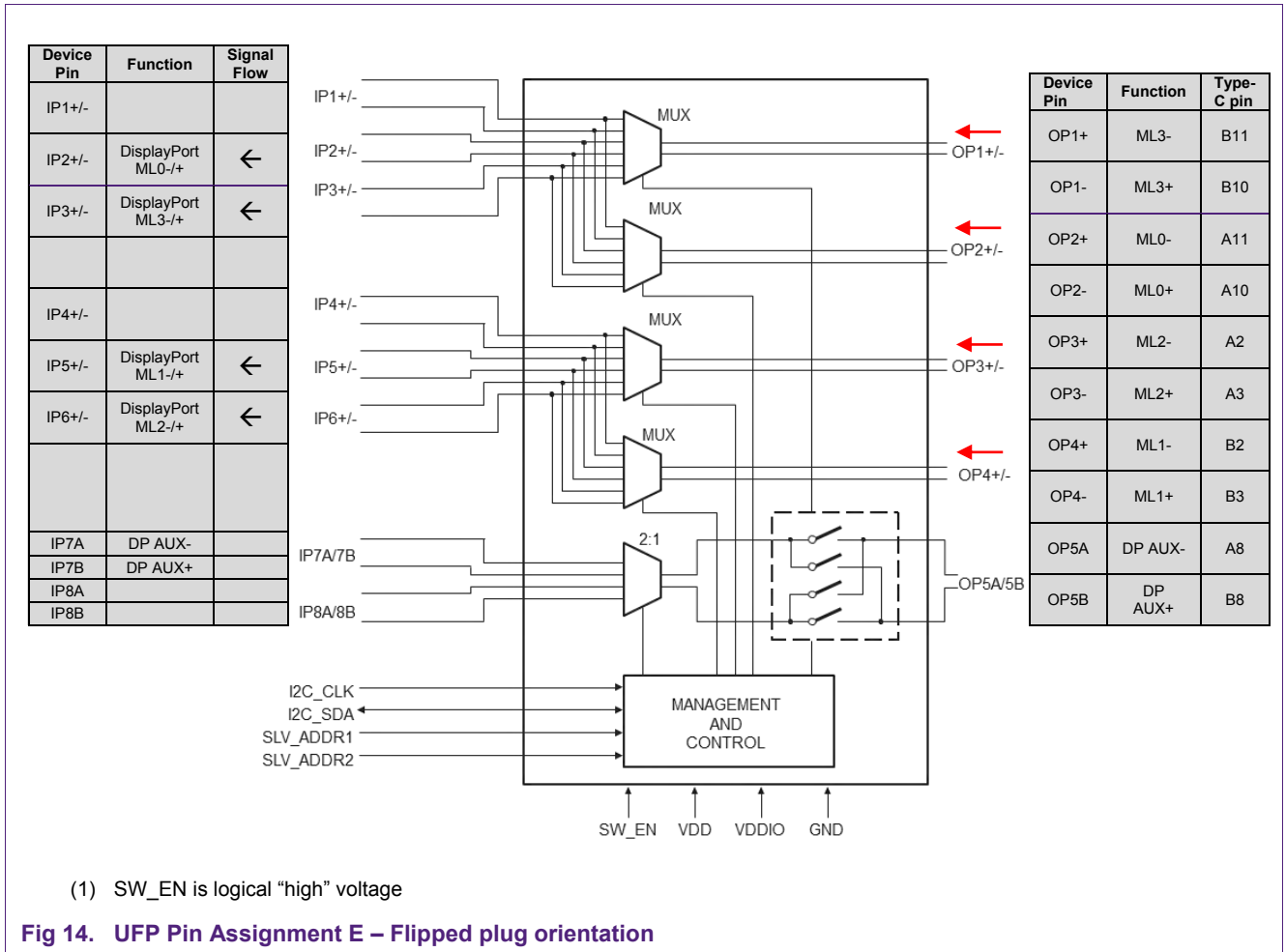**Fig 12.   UFP Pin Assignment D – Flipped plug orientation**

Table 11.   Register Map: UFP Pin Assignment D – Flipped plug orientation
Reserved bit fields are shaded. Reads will be zeros and writes do not have any effect

Address Offset	Register Name	Access	Hex Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x01	SYS_CTRL	RW	0x80	1							
0x02	OP1_CTRL	RW	0x04						1	0	0
0x03	OP2_CTRL	RW	0x01						0	0	1
0x04	OP3_CTRL	RW	0x20			1	0	0			
0x05	OP4_CTRL	RW	0x08			0	0	1			
0x06	OP5_CTRL	RW	0x40	0	1						
0x07	CROSS5_CTRL	RW	0x02							1	0
0x08	SW_CTRL	W	0x3F			1	1	1	1	1	1

3.5 UFP Pin Assignment E

UFP Pin Assignment E is for use cases where a UFP Type-C connector in a display monitor (sink) is connected to a DisplayPort-type source connector with a passive or active cable. Such cable assemblies have unique features as defined in the DP Alt Mode specification. For example note the signal inversion of the high-speed lines when compared to other UFP pin assignments. In addition these cables will contain AC-coupling capacitors on 2 of the 4 high-speed lanes. The required pinout and signal mappings are shown in Fig 13 and Fig 14. Table 12 and Table 13 show the relevant register maps for the CBTL08GP053 respectively.

Device Pin table (left):

Device Pin	Function	Signal Flow
IP1+/-		
IP2+/-	DisplayPort ML0-/+	←
IP3+/-	DisplayPort ML3-/+	←
IP4+/-		
IP5+/-	DisplayPort ML1-/+	←
IP6+/-	DisplayPort ML2-/+	←
IP7A	DP AUX-	
IP7B	DP AUX+	
IP8A		
IP8B		

Device Pin table (right):

Device Pin	Function	Type-C pin
OP1+	ML0-	B11
OP1-	ML0+	B10
OP2+	ML3-	A11
OP2-	ML3+	A10
OP3+	ML1-	A2
OP3-	ML1+	A3
OP4+	ML2-	B2
OP4-	ML2+	B3
OP5A	DP AUX+	A8
OP5B	DP AUX-	B8

(1) SW_EN is logical "high" voltage

Fig 13. UFP Pin Assignment E – Normal plug orientation

Table 12. Register Map: UFP Pin Assignment E – Normal plug orientation
Reserved bit fields are shaded. Reads will be zeros and writes do not have any effect

Address Offset	Register Name	Access	Hex Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x01	SYS_CTRL	RW	0x80	1							
0x02	OP1_CTRL	RW	0x02						0	1	0
0x03	OP2_CTRL	RW	0x04						1	0	0
0x04	OP3_CTRL	RW	0x10			0	1	0			
0x05	OP4_CTRL	RW	0x20			1	0	0			
0x06	OP5_CTRL	RW	0x40	0	1						
0x07	CROSS5_CTRL	RW	0x02							1	0
0x08	SW_CTRL	W	0x3F			1	1	1	1	1	1

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(1) SW_EN is logical "high" voltage

Fig 14. UFP Pin Assignment E – Flipped plug orientation

Table 13. Register Map: UFP Pin Assignment E – Flipped plug orientation
Reserved bit fields are shaded. Reads will be zeros and writes do not have any effect

Address Offset	Register Name	Access	Hex Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x01	SYS_CTRL	RW	0x80	1							
0x02	OP1_CTRL	RW	0x04						1	0	0
0x03	OP2_CTRL	RW	0x02						0	1	0
0x04	OP3_CTRL	RW	0x20			1	0	0			
0x05	OP4_CTRL	RW	0x10			0	1	0			
0x06	OP5_CTRL	RW	0x40	0	1						
0x07	CROSS5_CTRL	RW	0x01							0	1
0x08	SW_CTRL	W	0x3F			1	1	1	1	1	1

3.6 DP Alt Mode Standby Modes

Various usage cases have been presented in the previous sections to support DP Alt Mode functionality over Type-C connectors with the CBTL08GP053. There are also other configurations for the CBTL08GP053 that can be used as "safe" transition states between different DP Alt Mode pin assignments. Some possible options for DP standby modes for both DFP and UFP are presented in the following Tables. Please contact NXP for further specific implementation details.

Table 14. Safe Mode – Any plug orientation (DFP or UFP)
Reserved bit fields are shaded. Reads will be zeros and writes do not have any effect

Address Offset	Register Name	Access	Hex Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x01	SYS_CTRL	RW	0x80	1							
0x02	OP1_CTRL	RW	0x00						0	0	0
0x03	OP2_CTRL	RW	0x00						0	0	0
0x04	OP3_CTRL	RW	0x00			0	0	0			
0x05	OP4_CTRL	RW	0x00			0	0	0			
0x06	OP5_CTRL	RW	0x00	0	0						
0x07	CROSS5_CTRL	RW	0x00							0	0
0x08	SW_CTRL	W	0x3F			1	1	1	1	1	1

Table 15. USB 3x Mode – Normal plug orientation (DFP or UFP)
Reserved bit fields are shaded. Reads will be zeros and writes do not have any effect

Address Offset	Register Name	Access	Hex Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x01	SYS_CTRL	RW	0x80	1							
0x02	OP1_CTRL	RW	0x01						0	0	1
0x03	OP2_CTRL	RW	0x00						0	0	0
0x04	OP3_CTRL	RW	0x08			0	0	1			
0x05	OP4_CTRL	RW	0x00			0	0	0			
0x06	OP5_CTRL	RW	0x00	0	0						
0x07	CROSS5_CTRL	RW	0x00							0	0
0x08	SW_CTRL	W	0x3F			1	1	1	1	1	1

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Table 16. USB 3x Mode – Flipped plug orientation (DFP or UFP)

Reserved bit fields are shaded. Reads will be zeros and writes do not have any effect

Address Offset	Register Name	Access	Hex Value	Bit[7]	Bit[6]	Bit[5]	Bit[4]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
0x01	SYS_CTRL	RW	0x80	1							
0x02	OP1_CTRL	RW	0x00						0	0	0
0x03	OP2_CTRL	RW	0x01						0	0	1
0x04	OP3_CTRL	RW	0x00			0	0	0			
0x05	OP4_CTRL	RW	0x08			0	0	1			
0x06	OP5_CTRL	RW	0x00	0	0						
0x07	CROSS5_CTRL	RW	0x00							0	0
0x08	SW_CTRL	W	0x3F			1	1	1	1	1	1

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4. References

[1]   *CBTL08GP053 data sheet,* NXP Semiconductors, San Jose, CA, 2015

[2]   *VESA DisplayPort Alt Mode on USB Type-C Standard version 1.0*, Video Electronics Standards Association, Newark, CA 2014

[3]   *Universal Serial Bus Power Delivery Specification, Rev 2.0, V1.0,* 11 August 2014

[4]   *Universal Serial Bus Type-C Cable and Connector Specification Revision 1.1,* April 3, 2015

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