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NTAG I²C *plus* memory configuration options

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Application note
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Document information

Info	Content
Keywords	NTAG I²C *plus*, memory configuration, NDEF, read-only, EEPROM
Abstract	Describe how to configure the NTAG I²C *plus* in the different use case for read/write, read-only and protected access from RF and I²C side

Revision history

Rev	Date	Description
1.1	20180502	Editorial update and clarification on I²C address added
1.0	20160201	Initial revision

Contact information

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1. Introduction

The NTAG I²C *plus* ([2]) extends the NTAG I²C with several options to protect the access to the memory. The memory by default is read/write accessible and can be flexible protected to read-only, password protected write and password protected read/write.

The following use-cases should be described:

- Read only protection
- Partially password protect the memory:
  - split first part in unprotected/protected (keep in mind lock bit granularity)
  - use Sector 1 as password protected Memory (protect the write or read/write with a 32-bit password)
- Use a part of the memory as configuration EEPROM (only accessible from I²C) for e.g. MCUs
- Partial RF only access to Memory using the I²C lock bits

Additionally, it is important to know how to calculate the available NDEF size and put this information in the Capability Container, this is described first and then the different use cases are described.

2. Memory Layout of the NTAG I²C *plus*

If NDEF should be used on the tag, then the NDEF message always has to start at begin of the memory in user memory page 04 unless there are additional memory or lock control TLVs in front of the NFC message. Page 03 contains the NFC Forum capability container and contains the maximum available user memory size for storing a NDEF message.

How to define the NDEF message area in a NFC Forum Type 2 Tag is specified in [1]. Here a short practical introduction in calculating the capability container content should be given.

The Capability container in page 03 consists of four bytes. An example is given in the table below.

Table 1. Capability Container of a NFC Forum Type 2 Tag

Byte	Byte 0	Byte 1	Byte 2	Byte 3
Data/Content	0xE1	0x10	0x6D	0x00
Meaning	Magic Number for NDEF	NDEF mapping version 1.0	NDEF memory size in units of 8 bytes	NDEF access indicator, 0 means free access

Byte 2 contains the size of the memory map which can be used for NDEF storage. As long as there are no holes in this area (needed for the NTAG I²C *plus* 2k) the maximum size available for storing NDEF TLVs (T2T_Area) is given by:

T2T_Area = (Byte 2 of CC) * 8

The T2T_Area starts at page 04 and extends as many bytes as given by the NDEF memory size byte in the capability container.

To know the actual space for storing NDEF TLVs possible holes defined in Memory Control TLV and Lock Control TLVs have to be deducted from that space.

A memory initialization of a NTAG I²C *plus* with NDEF for a user memory size like the NTAG 216(F) is given in the below table. This initialization is recommended to be used on NTAG I²C *plus* 1k/2k unless there are special needs. When NDEF messages need more space, following changes need to be applied according to NFC Forum Type 2 Tag specification:

- CC, Byte2 (size of T2T_Area)
- Lock Control TLV needs to be added to address location of Dynamic Lock bits and their granularity
- Memory Control TLV needs to be added to exclude Configuration memory area and SRAM area at the end of Sector 0

Table 2. Memory initialization example for NTAG I²C *plus* for NDEF message size like on NTAG216

Page Address	Byte number within page			
	0	**1**	**2**	**3**
03h	E1h	10h	6Dh	00h
04h	03h	00h	FEh	00h

More details about how the memory can be configured to maximize the compatibility and locked to read only in a compatibility optimized way is described in [3].

NOTE: When configuring Block 0 of NTAG I²C plus from I²C perspective, also I²C write address gets updated, because I²C write address is stored in the first byte of user memory. Reading out this first byte of NTAG I²C plus, it always returns 04h (UID0). Therefore, for convenience reasons, it is recommended to change default I²C device address 55h to 02h. As this first byte codes I²C write address, 04h (02h shifted left by one bit) value needs to be written to Byte 0.

3. Use Cases.

3.1 Read Only Protection

The memory can be configured to be read only from the NFC side using the static and dynamic lock bits. The static lock bits can set the pages from 03h to 0Fh with a one-page granularity to read only. The dynamic lock bits lock the rest of the user memory with a granularity depending on the NTAG I²C *plus* memory size (1k or 2k).

If the lock bits are set, then RF cannot write to the corresponding pages anymore. The NFC side cannot unset the lock bits but the I²C side still can write to the memory even if the lock bits are set. I²C also can also reset the lock bits if write access from the NFC side to the corresponding pages is needed again.

So, if the content of read-only pages should be updated, either I²C needs to unset the lock bits and the NFC side can write again into the memory, or the data to be written is transferred using e.g. the pass-through mode to the MCU and the MCU writes the data into the memory over I²C.

The read only protection is independent from the other use cases shown below and can be freely combined with them. Only the recommendation for setting the size of the protected area below should be considered.

When protecting a tag to read only also the configuration lock bits (REG_LOCK_I2C and REG_LOCK_RF) should be considered and set if the configuration should be frozen. This two configuration lock bits once set remain set forever, they cannot be cleared.

3.2 Password Protection

The NTAG I²C *plus* features a password protection like the NTAG 21x(F). In the Sector 0 the password protection of the NTAG I²C *plus* works exactly like known from the NTAG 21x(F) where the relevant configuration parameters are:

- Protection pointer (AUTH0), which defines where the protected memory starts. If AUTH0 is set greater than EBh then password protection is disabled
- Protection mode (bit “NFC_PROT” in the configuration area), which defines if the protected area needs the password only for writing, or also for reading the memory
- Bit SRAM_PROT which enables/disables the password protection of read and write accesses to SRAM that includes pass-through mode
- Bit 2K_PROT which enables or disables password protection for the whole Sector 1 of the NTAG I²C *plus* 2K

For selecting the size of the protected area, these points should be considered as well:

- If either the protected area should be at the same time locked to read-only or a read-only area is directly before the protected area, it is necessary to align the protected area with the given granularity of the dynamic lock bits which is:
  - 16 pages per lock bit for the NTAG I²C *plus* 1k
  - 32 pages per lock bit for the NTAG I²C *plus* 2k
- If the T2T_Area (defined by the capability container) overlaps with the protected area, the start of the protected area should be aligned with lock bit granularity. In addition, a Memory Control TLV is needed to exclude the protected area from the T2T_Area.
- Dynamic Lock Bits are always on the same memory location. To be compliant to NFC Forum Type 2 Tag, in addition a Lock Control TLV is needed.

3.3 I²C only access

On the NTAG I²C *plus* 2k the Sector 1 can be switched unavailable for NFC access using the bit NFC_DIS_SEC1. When this bit is set to 1b, then NFC has no access to the whole Sector 1 anymore and this memory can then be used as I²C only accessible EEPROM starting from Block 64/40h to Block 127/7Fh.

This EEPROM area can be accessed with the normal NTAG I²C *plus* I²C read and write commands which read/write data in units of 16 bytes.

3.4 RF only access / I²C access protection

With the setting I2C_PROT the protected area defined by:

- All Memory above AUTH0 (page address in Sector 0) up to Block 58/3Ah (dynamic lock bits are excluded)
- If 2K_PROT is set the corresponding I²C blocks from NFC Sector 1 (Block 64/40h up to Block 127/7Fh)

Can be set to these modes:

- 00b: I²C has full read/write access to this area
- 01b: I²C can only read the protected area and read/write the remaining memory
- 1xb: I²C cannot access the protected area at all (only NFC can access the protected area)

With this mechanism a part of the memory can be specified which is only accessible via NFC.

4. References

[1] Type 2 Tag Operation, Technical Specification, Version 1.2, 2014-03-27, [T2TOP]

[2] NT3H2111/NT3H2211, NTAG I²C *plus*, NFC Forum Type 2 Tag compliant IC with I²C interface
http://www.nxp.com/documents/data_sheet/NT3H2111_2211.pdf

[3] AN11456, NTAG Using the dynamic lock bits to lock the tag

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