

# The Clock Monitor Unit (CMU)

## Initializing the CMU on MPC56xx & MPC57xx Devices

by: NXP Semiconductors

### 1 Introduction

A part's clocks are critical to its safe operation. They need to be accurate and correctly programmed and if there is any variation in their frequency then the application should be notified. Because of this, most NXP safety critical parts contain several Clock Monitor Units (CMU).

The main CMU of each device serves three purposes:

- Measures the frequency of the internal oscillator (IRCOSC)
- Monitors the external oscillator (XOSC) clock
- Monitors a selected clock

### 2 Overview

Main features of a CMU:

- Frequency meter: measure the IRCOSC frequency using the XOSC as a reference.
- XOSC clock monitoring: monitor the existence of the XOSC by comparing it to the IRCOSC clock.
- Selected clock monitoring: monitor the frequency of a selected clock against a user programmed upper and lower frequency boundary using IRCOSC clock ÷ 4 as a reference.
- Event generation for various failures detected.

The majority of the MPC56xx and MPC57xx parts have more than one CMU unit. The device has a CMU\_0 that is capable of measuring the IRCOSC, XOSC monitoring, and monitoring one of the other system clocks. The device then contains other CMU\_n blocks that are capable of monitoring other important system clocks. See the following table for examples of the CMU use for the MPC5643L and MPC5744P devices:

Table 1. CMU Use

Device	Module	Monitored clocks
MPC5643L	CMU_0	<ul style="list-style-type: none"><li>• System clock</li><li>• XOSC</li><li>• IRCOSC</li></ul>
	CMU_1	<ul style="list-style-type: none"><li>• Motor control clock</li></ul>
	CMU_2	<ul style="list-style-type: none"><li>• FlexRay Clock</li></ul>

Table continues on the next page...

#### Contents

- 1 Introduction..... 1
- 2 Overview..... 1
- 3 Procedure..... 4
- 4 Code Example..... 7



Table 1. CMU Use (continued)

Device	Module	Monitored clocks
MPC5744P	CMU0	<ul style="list-style-type: none"> <li>• MOTC_CLK</li> <li>• XOSC</li> <li>• IRCOSC</li> </ul>
	CMU1	<ul style="list-style-type: none"> <li>• SYS_CLK</li> </ul>
	CMU2	<ul style="list-style-type: none"> <li>• PBRIDGE<sub>n</sub>_CLK</li> </ul>
	CMU3	<ul style="list-style-type: none"> <li>• ADC_CLK</li> </ul>
	CMU4	<ul style="list-style-type: none"> <li>• SENT_CLK</li> </ul>

The user can use the CMU\_0 to verify the exact frequency of the IRCOSC clock. Since this clock can be used as the reference for other system clocks or protocol clocks it could be critical to know the exact frequency to ensure proper protocol timing.

The CMU\_0 can also be used to monitor the XOSC. This feature only checks that the  $XOSC > (IRCOSC \text{ clock}) \div 2^{RCDIV}$  where the RCDIV is a user selectable value of 0, 1, 2, or 3 in the CMU's Control Status Register (CMU\_CSR). This feature does not measure the frequency of the XOSC. Assuming an IRCOSC clock of 16 MHz, the CMU only checks that the XOSC is greater than either 16 MHz, 8 MHz, 4 MHz, or 2 MHz.

The user can closely monitor any of the selected system clocks that are hooked up to one of the part's many CMU's. With this feature the user can set an upper and lower limit for the CMU to compare the selected clock's frequency.

When a failure is detected in a CMU, by either the selected clock monitor or the XOSC monitor, the CMU can notify different modules in the system depending on the device's configuration. For some devices, this could be the Reset Generation Module (MC\_RGM), the Mode Entry (MC\_ME) module, and the Fault Control and Collection Unit (FCCU) module. The user has the option to program the system's reaction to a CMU fault through the modules that get notified. Some of the options available depending on what modules are available in the device are generating a reset, entering SAFE mode, or generating an interrupt.

In the [Figure 1. CMU\\_0 Block Diagram](#) on page 3 below, the clock selection signal, controlled by the clock selection (CKSEL1) bits of the CMU\_CSR, allows the user to select from several different reference sources. In truth the only option that is ever implemented is the IRCOSC. In some devices, it is hooked up to one of the inputs making the other ones invalid and in others it is hooked up to all of them.

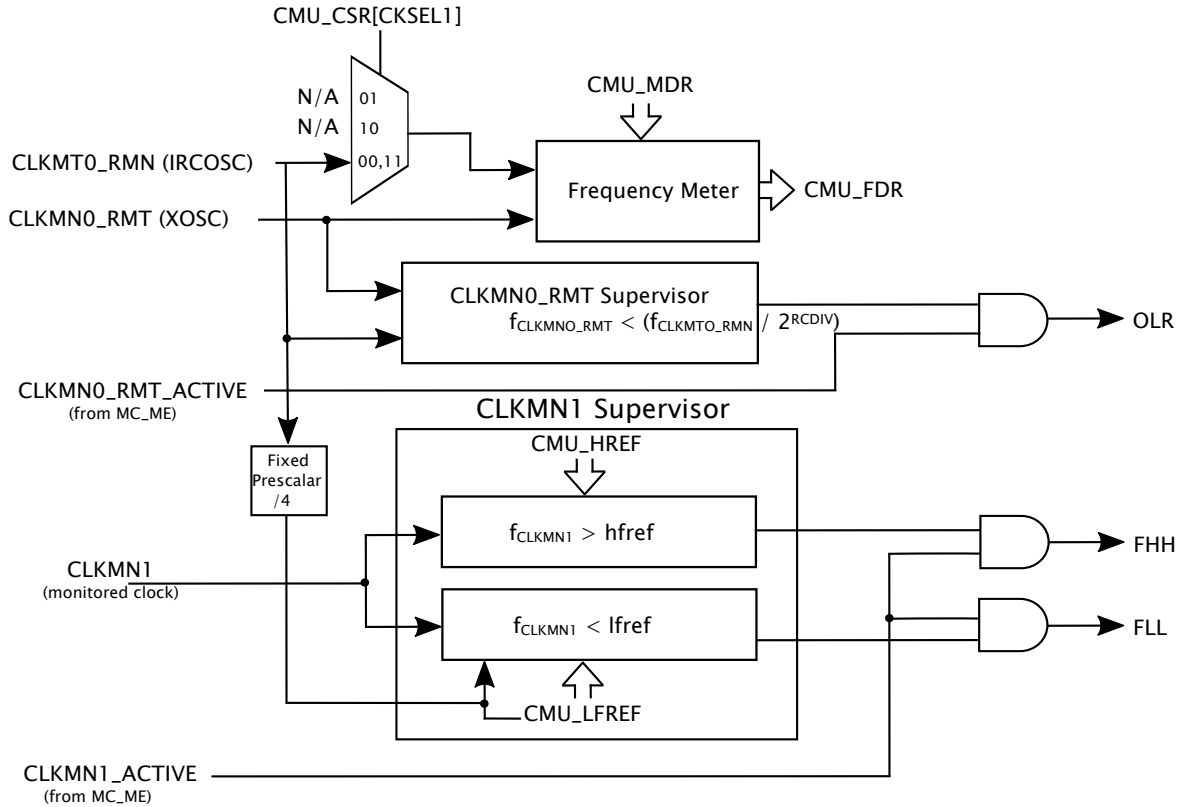


Figure 1. CMU\_0 Block Diagram

In the [Figure 2. CMU\\_n Block Diagram](#) on page 3 below, the blocks for the frequency meter and the blocks for monitoring the XOSC are absent. The CMU\_n modules do not support these functions.

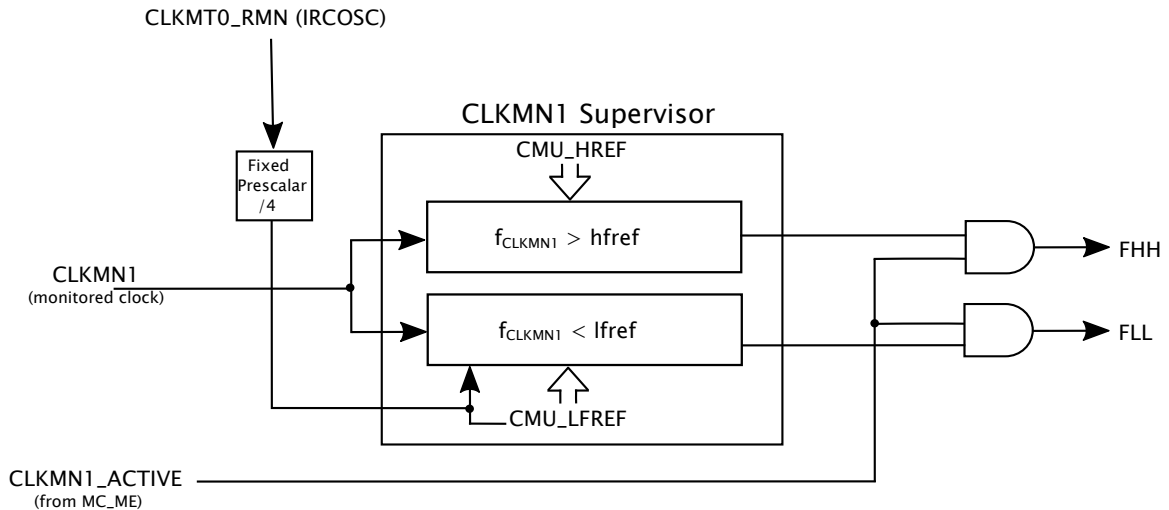


Figure 2. CMU\_n Block Diagram

Different device manuals might refer to the CMU signals differently. MPC56xx manuals usually reference the IRCOSC and the XOSC signals directly while it is more common in the MPC57xx devices to use the more formal signal names such as CLKMN0\_RMT and CLKMNMT0\_RMN. The [Table 2. Signal Description](#) on page 4 table below describes which clock sources are connected to which CMU signals.

Table 2. Signal Description

Signal	I/O	Description
CLKMN0_RMT (Always XOSC)	I	Monitored Clock Signal 0/Metered Clock Signal Reference — Receives a clock signal that the CMU compares to a specified low-limit frequency to determine whether the frequency of the clock signal is greater than the specified limit. Also provides a reference clock signal for all metered clock signals.
CLKMN1	I	Monitored Clock Signal 1 — Receives a clock signal that the CMU compares to specified low limit and high limit frequencies to determine whether the frequency of the clock signal is between the specified limits.
CLKMT0_RMN (Always IRCOSC)	I	Metered Clock Signal 0/Monitored Clock Signal Reference — Receives a clock signal that the CMU measures against a reference clock frequency. Also provides a reference clock signal for all monitored clock signals.

## 3 Procedure

### 3.1 Measuring the IRCOSC, also called frequency metering

The frequency meter, which is part of CMU\_0, measures the IRCOSC (CLKMT0\_RMN) using a known frequency, the XOSC (CLKMN0\_RMT). Knowing the exact frequency of the IRCOSC allows the user to make other timing corrections if necessary. The measurement starts when the start frequency measurement (SFM) bit of the Control Status Register (CMU\_CSR) is set. The measurement duration is given by the measurement duration (MD) bits of the Measurement Duration Register (CMU\_MDR) in terms of IRCOSC clock cycles with a width of 20 bits. The SFM bit is cleared by the hardware after the frequency measurement is done and the count is loaded in the measured frequency (FD) bits of the Frequency Display Register (CMU\_FDR). The IRCOSC measurement can be derived as follows:

$$f_{sel} = f_{CLKMN0\_RMT} \times \frac{CMU\_MDR[MD]}{CMU\_FDR[FD]}$$

Steps:

1. Program the CMU\_MDR[MD] value.
2. Program the CMU\_CSR[CKSEL1] bit to the CLKMT0\_RMN you wish to measure.
3. Enable the monitor by setting the CMU\_CSR[SMF] bit.
4. When the CMU\_CSR[SMF] bit is clear read the CMU\_FDR[FD] value and calculate the IRCOSC frequency.

### 3.2 Monitoring the XOSC clock

The XOSC (CLKMN0\_RMT) clock is automatically monitored by CMU\_0. If the XOSC is determined on and stable, signaled by CLKMN0\_RMT\_ACTIVE signal, and the frequency of the XOSC meets the following condition:

$$f_{XOSC\_CLK} < f_{IRCOSC\_CLK} \div 2^{CSR[RCDIV]}$$

then an oscillator less than (OLR) error event has occurred and the CMU\_0 takes the following steps:

1. The oscillator less than interrupt bit (OLRI) gets set in the CMU Interrupt Status Register (CMU\_ISR[OLRI]).
2. A failure event is signaled to the system which can react as programmed by the user. In many devices the MC\_RGM, MC\_ME, and FCCU are notified, which in turn can generate a 'functional' reset, a SAFE mode request, or an interrupt.

**NOTE**

For the MPC56xx devices the XOSC monitor may produce a false event when  $f_{\text{XOSC\_CLK}} < 2 \times f_{\text{IRCOSC\_CLK}} \div 2^{\text{CSR[RCDIV]}}$  due to an accuracy limitation of the compare circuitry.

**NOTE**

For the MPC57xx devices the  $f_{\text{XOSC\_CLK}}$  (CLKMN0\_RMT) must be greater than  $f_{\text{IRCOSC\_CLK}} \div 2^{\text{CSR[RCDIV]}}$  (CLKMT0\_RMN) by at least 0.5 MHz in order to guarantee correct XOSC (CLKMN0\_RMT) monitoring.

### 3.3 Monitoring the system clock or any other CMU\_n clock

This section applies to the device's main system clock, usually monitored by CMU\_0, and all monitored clocks (CLKMN1) monitored by the other CMU\_ns on the device.

The monitored clock (CLKMN1) frequency can be monitored by setting the Clock Monitor Enable (CME) bit in the CMU\_CSR. The clock monitoring starts as soon as  $\text{CMU\_CSR}[CME] = 1$ . This monitor can be disabled at any time by writing  $\text{CMU\_SCR}[CME] = 0$ .

If the monitored clock is greater than the High Frequency Reference (HFREF) value programmed into the High Frequency Reference Register (CMU\_HFREFR) and the monitored clock is enabled, then:

- A frequency higher than high reference (FHH) event is detected and  $\text{CMU\_ISR}[FHHI]$  is set
- A failure event is signaled to the system which can react as programmed by the user. In many devices the MC\_RGM, MC\_ME, and FCCU are notified, which in turn can generate a 'functional' reset, a SAFE mode request, or an interrupt.

If the monitored clock is less than the Low Frequency Reference (LFREF) value programmed into the Low Frequency Reference Register (CMU\_LFREFR) and the monitored clock is enabled, then:

- A frequency lower than low reference (FLL) event is detected and  $\text{CMU\_ISR}[FLLI]$  is set
- A failure event is signaled to the system which can react as programmed by the user. In many devices the MC\_RGM, MC\_ME, and FCCU are notified, which in turn can generate a 'functional' reset, a SAFE mode request, or an interrupt.

On the MPC56xx devices only, if the monitored clock is less than the reference clock frequency ( $f_{\text{IRCOSC\_CLK}} \div 4$ ) and the monitored clock is enabled, then:

- a frequency lower than reference clock (FLC) event is detected and  $\text{CMU\_ISR}[FLCI]$  is set
- A failure event is signaled to the system which can react as programmed by the user. In many devices the MC\_RGM, MC\_ME, and FCCU are notified, which in turn can generate a 'functional' reset, a SAFE mode request, or an interrupt.

**NOTE**

For the MPC56xx devices the system clock monitor may produce a false event when the monitored clock is less than  $2 \times f_{\text{IRCOSC\_CLK}} \div 2^{\text{CSR[RCDIV]}}$  due to an accuracy limitation of the compare circuitry.

The following equations are used to calculate HFREF and LFREF:

$$\text{HFREF} = \frac{f_{\text{CLKMN1}}}{(f_{\text{IRCOSC}} \div 4)} \times 16$$

$$\text{LFREF} = \frac{f_{\text{CLKMN1}}}{(f_{\text{IRCOSC}} \div 4)} \times 16$$

Procedure

Steps:

1. Program the CMU\_HFREFR[HFREF] and CMU\_LFREFR[LFREF] values.
2. Enable the monitor by setting the CMU\_CSR[CME] bit.

### 3.4 Requirements

A key point that always needs to be considered is that the user should check a device's data sheet for its IRCOSC variation. For any device, there are specifications for IRCOSC variation. It is necessary to take this into account when calculating the HFREF and LFREF values. Failure to adhere to the allowable variation detailed in a device's data sheet could result in false failures. The two tables below have excerpts from the MPC5643L and the MPC5744P data sheet.

**Table 3. MPC5643L 16 MHz RC oscillator electrical characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta_{RCMVAR}$	Fast internal RC oscillator variation over temperature and supply with respect to $f_{RC}$ at $T_A = 25\text{ }^\circ\text{C}$ in high-frequency configuration	-	-6	-	6	%

**Table 4. MPC5744P Internal RC Oscillator electrical specifications**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\delta F_{var\_noT}$	IRC frequency variation without temperature compensation	$T_J < 150\text{ }^\circ\text{C}$	-8	-	8	%
		$T_J < 165\text{ }^\circ\text{C}$	-10	-	10	

An example of determining the  $HFREF_{Actual}$  and  $LFREF_{Actual}$  for the MPC5744P device is as follows. The  $f_{IRCOSC\_CLK} = 16$  MHz with an accuracy of +/- 8%. In order to monitor a  $f_{CLKMN1} = 200$  MHz the ideal reference value is:

$$HFREF_{Ideal} = ( 200 / ( 16 / 4 ) ) * 16$$

$$HFREF_{Ideal} = ( 200 / 4 ) * 16$$

$$HFREF_{Ideal} = 50 * 16$$

$$HFREF_{Ideal} = 800.$$

The  $HFREF_{Ideal}$  and  $LFREF_{Ideal}$  are the same. The  $HFREF_{Actual}$  and  $LFREF_{Actual}$  are:

$$HFREF_{Actual} = HFREF_{Ideal} + (HFREF_{Ideal} * 0.08)$$

$$HFREF_{Actual} = 800 + (800 * 0.08)$$

$$HFREF_{Actual} = 800 + 64$$

$$HFREF_{Actual} = 864$$

$$LFREF_{Actual} = LFREF_{Ideal} - (LFREF_{Ideal} * 0.08)$$

$$LFREF_{Actual} = 800 - (800 * 0.08)$$

$$LFREF_{Actual} = 800 - 64$$

$$LFREF_{Actual} = 736$$

## 4 Code Example

See the attached Green Hills project for MPC5744P example code.

**How To Reach Us**

**Home Page:**

[nxp.com](http://nxp.com)

**Web Support:**

[nxp.com/support](http://nxp.com/support)

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [nxp.com/SalesTermsandConditions](http://nxp.com/SalesTermsandConditions).

NXP, the NXP logo, NXP SECURE CONNECTIONS FOR A SMARTER WORLD, COOLFLUX, EMBRACE, GREENCHIP, HITAG, I2C BUS, ICODE, JCOP, LIFE VIBES, MIFARE, MIFARE CLASSIC, MIFARE DESFire, MIFARE PLUS, MIFARE FLEX, MANTIS, MIFARE ULTRALIGHT, MIFARE4MOBILE, MIGLO, NTAG, ROADLINK, SMARTLX, SMARTMX, STARPLUG, TOPFET, TRENCHMOS, UCODE, Freescale, the Freescale logo, Altivec, C-5, CodeTEST, CodeWarrior, ColdFire, ColdFire+, C-Ware, the Energy Efficient Solutions logo, Kinetis, Layerscape, MagniV, mobileGT, PEG, PowerQUICC, Processor Expert, QorIQ, QorIQ Qonverge, Ready Play, SafeAssure, the SafeAssure logo, StarCore, Symphony, VortiQa, Vybrid, Airfast, BeeKit, BeeStack, CoreNet, Flexis, MXC, Platform in a Package, QUICC Engine, SMARTMOS, Tower, TurboLink, and UMEMS are trademarks of NXP B.V. All other product or service names are the property of their respective owners. Arm, AMBA, Arm Powered, Artisan, Cortex, Jazelle, Keil, SecurCore, Thumb, TrustZone, and  $\mu$ Vision are registered trademarks of Arm Limited (or its subsidiaries) in the EU and/or elsewhere. Arm7, Arm9, Arm11, big.LITTLE, CoreLink, CoreSight, DesignStart, Mali, Mbed, NEON, POP, Sensinode, Socrates, ULINK and Versatile are trademarks of Arm Limited (or its subsidiaries) in the EU and/or elsewhere. All rights reserved. Oracle and Java are registered trademarks of Oracle and/or its affiliates. The Power Architecture and Power.org word marks and the Power and Power.org logos and related marks are trademarks and service marks licensed by Power.org.