

AN12137

PTN5110N PD PHY application programming guide

Rev. 1.0 — 10 July 2018

Application note

Document information

Information	Content
Keywords	PTN5110N, TCPC, Type-C Port Controller, TCPM, USB PD PHY, Fast Role Swap
Abstract	PTN5110N is a 1-port TCPC (Type-C Port controller) compliant USB Power Delivery (PD) PHY IC that implements Type-C configuration channel interface and USB PD physical layer functions to a Type-C Port Manager (TCPM) that handles PD Policy management. The device can be used in the following applications: PC platforms (Notebook PCs, Desktop PCs, Ultra-books, Chromebooks), Tablets, 2:1 Convertibles, Smartphones and Portable devices, and PC accessories/peripherals (Docking, Mobile Monitors, Multi-Function Monitors, Portable/External hard drives, Cable adapters, Dongles and accessories, etc.)



Revision history

Rev	Date	Description
v.1.0	20180710	Initial version

1 Introduction

PTN5110N is a 1-port TCPC (Type-C Port controller) compliant USB Power Delivery (PD) PHY IC that implements Type-C configuration channel interface and USB PD physical layer functions to a Type-C Port Manager (TCPM) that handles PD Policy management. It complies with USB PD [1], Type-C [2] and TCPC [3] specifications and relevant ECNs/ECRs. This IC is targeted primarily for use in system platforms (e.g. Notebook PCs, Desktop PCs, Chromebooks, Tablets, Convertibles, etc.). Other use cases may be feasible depending on the application architecture - e.g. Docks, Monitors, Accessories, Cable adapters, Smartphones etc.

It can support Type-C roles – sink, source, sink with accessory support or DRP. It implements Type-C CC analog portion (i.e Rd/Rp/Ra detection, Rd/Rp indication) and PD Tx/Rx PHY and protocol state machines as per [3]. PTN5110N supports TCPM in system realization of the following PD roles: (i) Provider (P), (ii) Provider/Consumer (P/C) (iii) Consumer (C) (iv) Consumer/Provider (C/P).

PTN5110N can be programmed to operate with or without (autonomous, factory programmed) a policy controller. In autonomous mode, PTN5110N does the following:

- Cable plug/unplug handling
- Determine plug orientation
- CC detection/indication scheme based on preprogrammed DRP, DFP or UFP role
- Handling (applying) of Rd or Rp depending on preprogrammed port role
- Automatically closes the external power FETs

In non-autonomous mode, PTN5110N works under the control of a policy controller and a System Management Controller (SMC). Under the guidance of the policy controller and the SMC through the I²C-bus interface and hardware interrupt based, PTN5110N can be programmed to accomplish tasks such as power contract negotiations, swap power roles, swap data roles, request higher or lower power levels, and initiate and acknowledge DP Alternate mode. PTN5110N also supports Vendor Defined Message.

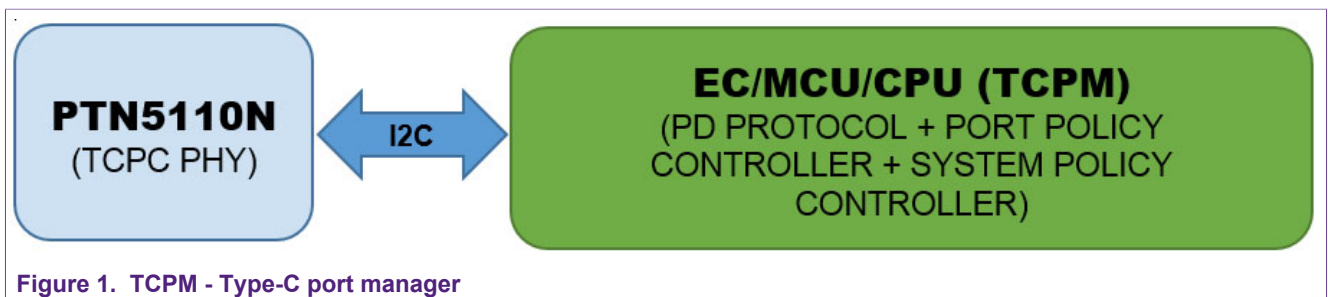


Figure 1. TCPM - Type-C port manager

The port policy and protocol controller (TCPM - Type-C port manager) are implemented in the EC as shown in the above figure. The PTN5110N PD PHY functionality can be programmed by the EC through a set of standardized registers that have been defined by USB IF called TCPC interface. The common interface between TCPM and TCPC defined by USB IF is shown below:

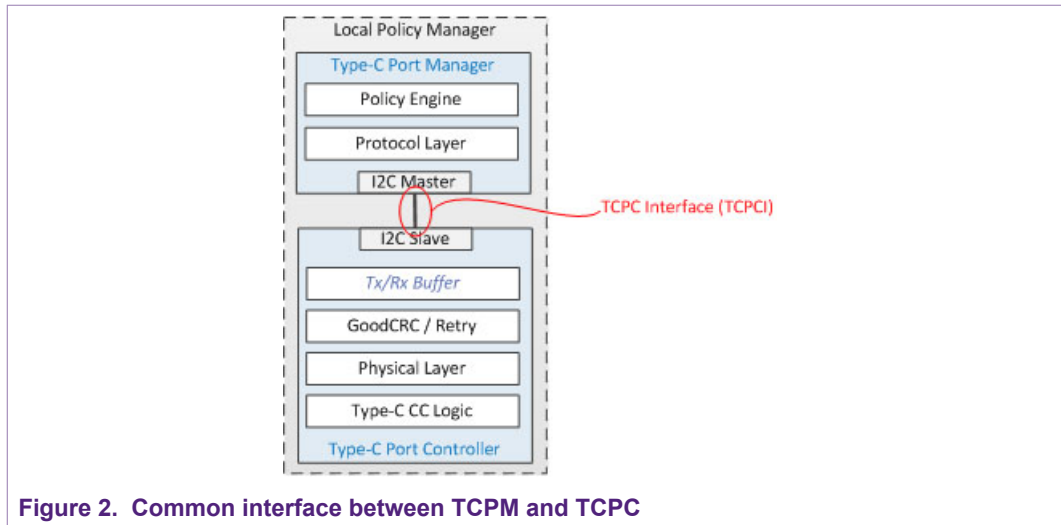


Figure 2. Common interface between TCPM and TCPC

2 I²C-bus interface

PTN5110N acts as an I²C slave to an I²C master and its slave address can be selected by the SLV_ADDR pin. The table below lists the four I²C addresses supported by PTN5110N.

Table 1. Supported I²C addresses

SLV_ADDR pin	Device address (Write/read) 7:0
GND	1010000x
10K pullup to BYPASS pin	1010001x
Unconnected	1010010x
100K pullup to BYPASS pin	1010011x

The I²C-bus interface is based on the standard I²C specification. The read and write operation specified by the I²C standard should be followed. Each I²C transaction requires a slave address, a register address (Reg Offset), followed by data bytes.

2.1 I²C write

The following figure shows an example of an I²C write operation.

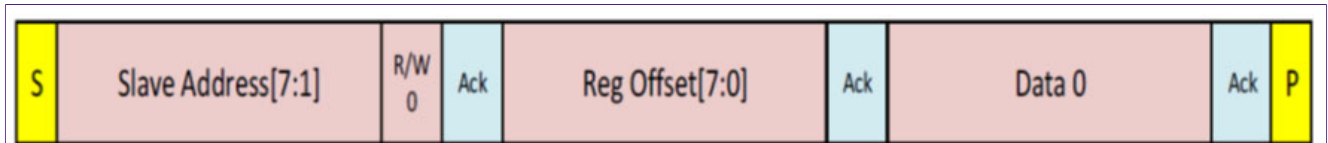


Figure 3. I²C write operation

2.2 I²C read

The following figure shows a repeat start I²C read operation.

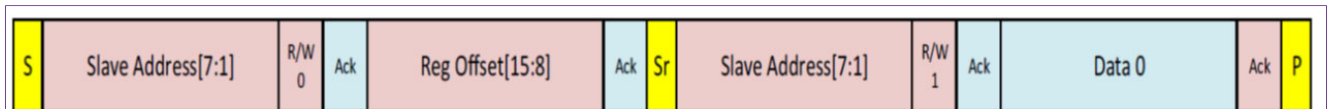


Figure 4. Repeat start I²C read operation

3 Register interface

PTN5110N implements the full register set defined by USB IF in the Type-C Port Controller specification. The register interface consists of several 8-bit registers. The list of these registers and the register bit(s) descriptions are listed in [Section 8](#). The functionality and behavior of the PTN5110N are dependent on how these registers are programmed. The power-on or default register settings are programmed at the factory into the non-volatile flash memory Multi-Time Programmable (MTP) inside the PTN5110N. These preprogrammed parameters determine the initial behavior of the PTN5110N, e.g., the PTN5110N can behave as Type-C DFP, UFP, or DRP upon power up. The PTN5110N can also be programmed to operate autonomously without a host intervention, e.g., during dead battery condition. Once the PTN5110N is up and running, the EC/SMC (system management controller) can always reprogram the PTN5110N through the register interface to change its behavior, such as to request higher power or lower power from the remote provider, to request role swap if needed, or to do Alternate modes. PTN5110N internal registers are listed in [Table 3](#).

Below are some sample flow charts to initialize PTN5110N, to set up the PTN5110N to handle interrupts, and to setup PTN5110N to send a USB PD message as well as to receive a PD message.

Type-C state machines and various timings related to the state machines are not described or specified in this application note. Please refer to Type-C and TCPC specifications.

4 PTN5110N initialization and connection

4.1 DPR initialization and connection

The flow chart below shows how TCPC can be configured to DRP role, and how to handle a valid connection. For standardization and simplification purposes, this flow chart is copied from the TCPC specification [3], figure 4-20. Please check USB.org for the latest spec update.

- After power on, PTN5110N generates a fault interrupt per TCPC spec. TCPM must clear this fault interrupt to deassert the alert pin.
- ROLE_CONTROL register is used to program the data role.
- ROLE_CONTROL bit 6 is used to select DRP role.
- ROLE_CONTROL bit3:0 can be used to select DFP or UFP role. Select Rp for DFP role and select Rd for UFP role.
- Once the role is configured, command 0x99 (Look4Connection) must be issued to TCPC to start DRP toggling.
- After a connection is established, the DRP actual role (DFP or UFP) can be determined by reading CC_STATUS register. The ConnectionResult bit (B4) of this register indicates whether TCPC presents Rp or Rd after the connection. Base on the ConnectionResult state, CC line state can be determined by reading CC1 state bits (B1:0), and CC2 state bits (b3:2).
- TCPC_CONTROL PlugOrientation bit (B0) state then can be written to indicate to TCPC what CC pin to apply VCONN, and what CC pin is used for BMC communication.
- Command SourceVbusDefaultVoltage or SinkVbus then can be issued to TCPC. TCPC power role (source/sink) must be determined by TCPM prior to issue this command based on the CC_STATUS.ConnectionResult.

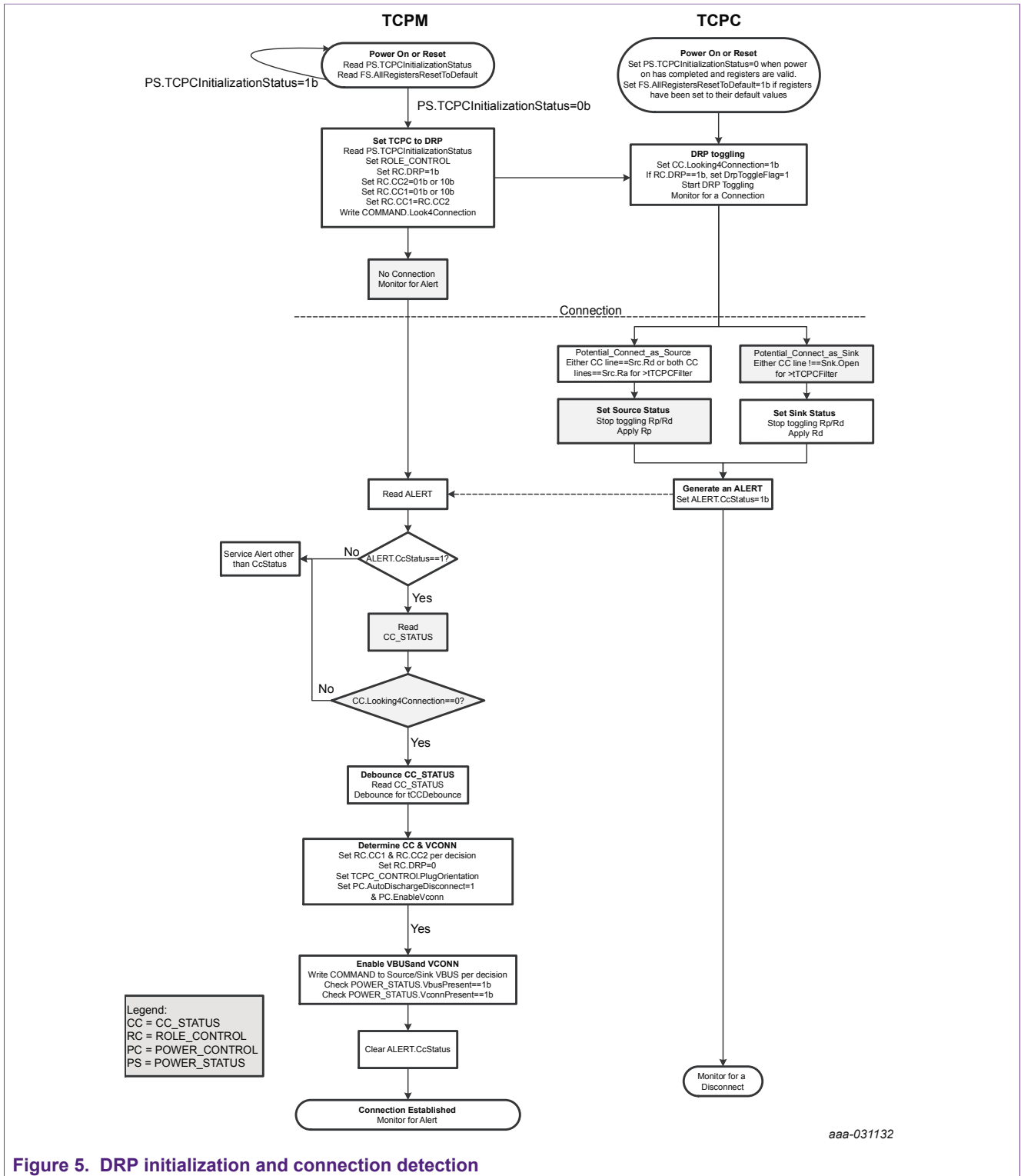


Figure 5. DRP initialization and connection detection

4.2 DFP initialization

To configure TCPC for DFP role, ROLE_CONTROL.DRP must be set to 0, ROLE_CONTROL.CC1State and ROLE_CONTROL.CC2State set to Rp. TCPC

initialization, connection handling, disconnection handling can be the same as specified in the DRP flow chart.

4.3 UFP initialization

To configure TCPC for DFP role, `ROLE_CONTROL.DRP` must be set to 0, `ROLE_CONTROL.CC1State` and `ROLE_CONTROL.CC2State` set to Rd. TCPC initialization, connection handling, disconnection handling can be the same as specify in the DRP flow chart, or source/sink disconnect flow charts.

4.4 Source disconnect

For standardization and simplification purposes, this flow chart is copied from the TCPC specification [3], figure 4-21. Please check USB.org for the latest spec update.

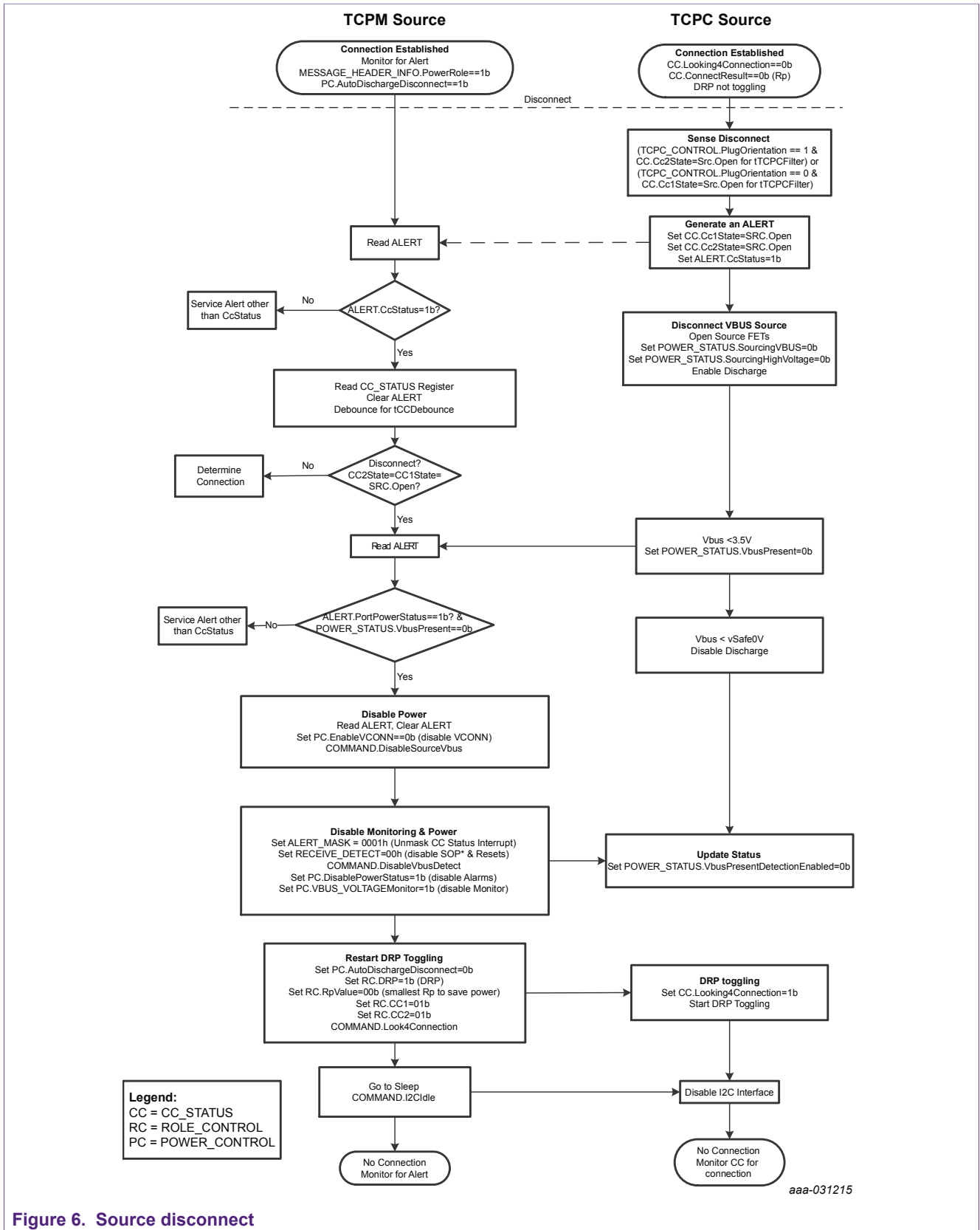


Figure 6. Source disconnect

4.5 Sink disconnect

For standardization and simplification purposes, this flow chart is copied from the TCPC specification [\[3\]](#), figure 4-21. Please check USB.org for the latest spec update.

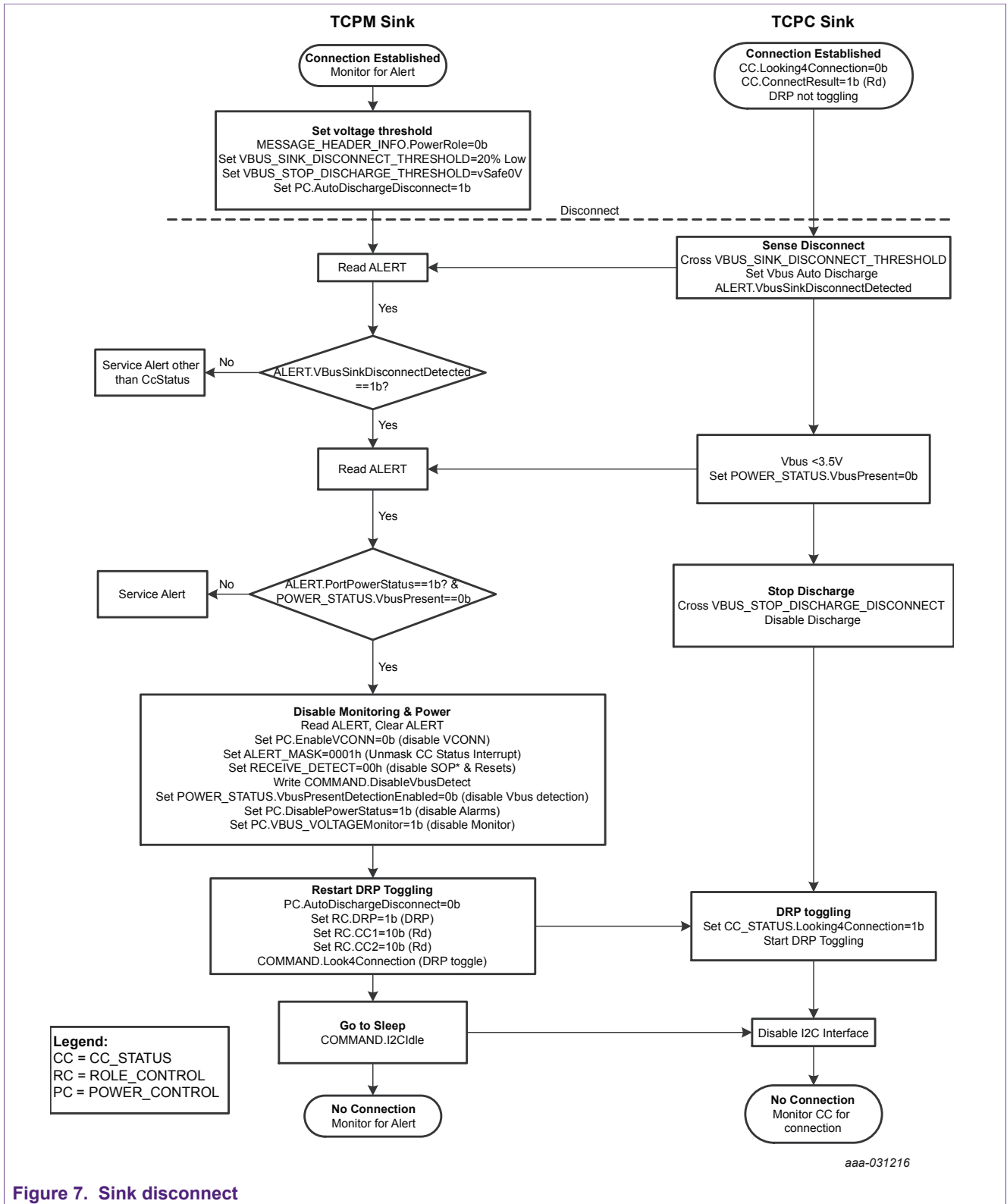


Figure 7. Sink disconnect

5 Sending a USB PD message

The general steps of transmitting a SOP* message are listed below. Please consult sections 4.7.1, 4.7.2, and 4.7.3 of the TCPC specification[3] for more detailed implementation and examples.

- Step 0: TCPM writes the content of the message to be transmitted into the TRANSMIT_BUFFER
- Step 1: TCPM writes to TRANSMIT requesting SOP* transmission
- Step 2: The outcome reported by the TCPC may be one of three indications after asserting the Alert# pin:
 - If the TCPC PHY layer successfully transmits the message, the TCPC sets the Transmission Successful bit in the ALERT register.
 - If the TCPC PHY layer did not get any response after retries, the TCPC sets the Transmission Failed bit in the ALERT register.
 - If the transmission was discarded due to an incoming message, the TCPC sets the Transmission Discarded bit in the ALERT register.
- Step 3: Before requesting another transmission, the TCPM shall clear the alert by writing a 1 to the asserted bit in the ALERT register.

When transitioning through the steps of transmitting SOP* message, TCPC may assert ALERT.ReceiveStatus or ALERT.ReceivedHardReset bit at any time to notify that a message was received.

6 Receiving a USB PD message

The steps of receiving SOP* message is listed below. Please consult section 4.7.4, 4.7.5, 4.7.6, 4.7.7 and 4.7.8 of TCPC specification[3] for more detailed implementation and examples.

- Step0: The TCPC asserts Alert# pin to request attention when it receives a Hard Reset, a Cable Reset, or has sent the GoodCRC in response to an SOP* message from a Port Partner.
- Step1: The TCPM reads the ALERT register to get notification that a message was received.
- Step2: The TCPM reads the RECEIVE_BUFFER.RECEIVE_BYTE_COUNT and RECEIVE_BUFFER.ReceiveSOP*Message. If the TCPC received an SOP* message, the TCPM reads as many bytes as defined in the RECEIVE_BUFFER.RECEIVE_BYTE_COUNT.
- Step3: The TCPM writes to the ALERT.ReceiveSOP*MessageStatus register to clear the message, the SOP* message buffer registers, and the ALERT.RxBufferOverflow. After the alert has been cleared, the TCPC shall put the next received message (if any) into the SOP* message buffer registers. The TCPC shall then update RECEIVE_BYTE_COUNT, RECEIVE_STATUS and ALERT registers.
- Step4: If Alert# pin is still asserted, go to Step 1.

7 USB PD 3.0 Support

7.1 Extended Message

PTN5110N allows TCPM to send and receive extended messages through TCPC standard transmit and receive buffer registers. Both chunked and unchunked messages are supported. Please consult section 6.2.1.2 (Extended Message Header) of USB PD specification[1] and 4.4.14, 4.4.15, 4.4.16 of TCPC specification[3] for more detailed implementation and examples.

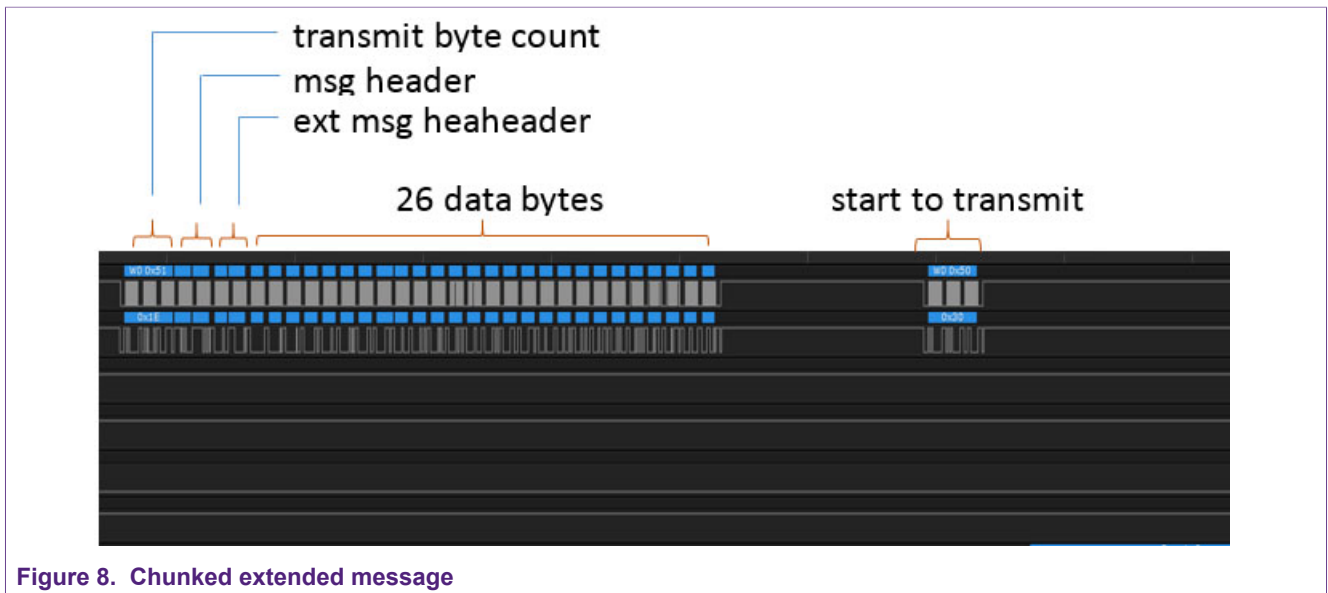
Chunked messages are supported using the standard USB PD mechanism to send a normal PD message with a minor modification – the first two bytes of the 28-byte data objects are used for extended message header. Therefore, the maximum data length in each message is 26 bytes. Up to 260 bytes of data can be sent and received as defined by USB PD specification[1].

Unchunked messages are supported using burst write and burst read the transmit and the receive buffers. TCPM can write up to 132 bytes to the transmit buffer in one burst. If the number of data to be sent is larger than 128 bytes, then TCPM must write the data into the transmit buffer in two burst writes.

7.1.1 Sending a chunked extended message

Below is an example of sending a chunk of 26 bytes. The complete message starts at transmit byte count register (address 0x51), and follows with the two-byte message header, two-byte extended message header and the rest of the data. TCPM then writes to the transmit register (0x50) to start sending the message.

If there are more chunks to be sent, then TCPM can use the same procedure described above to send the next chunk.



7.1.2 Sending an unchunked extended message

Below is an example of sending an unchunked message of 260 bytes. The complete message starts at transmit byte count register (address 0x51), followed by the two-byte message header, two-byte extended message header and the rest of the data. Since TCPM can only do a burst write of 132 bytes to the transmit buffer, the data must be separated into two separate writes of 132 bytes each. TCPM then writes to the transmit register (0x50) to start sending the message.

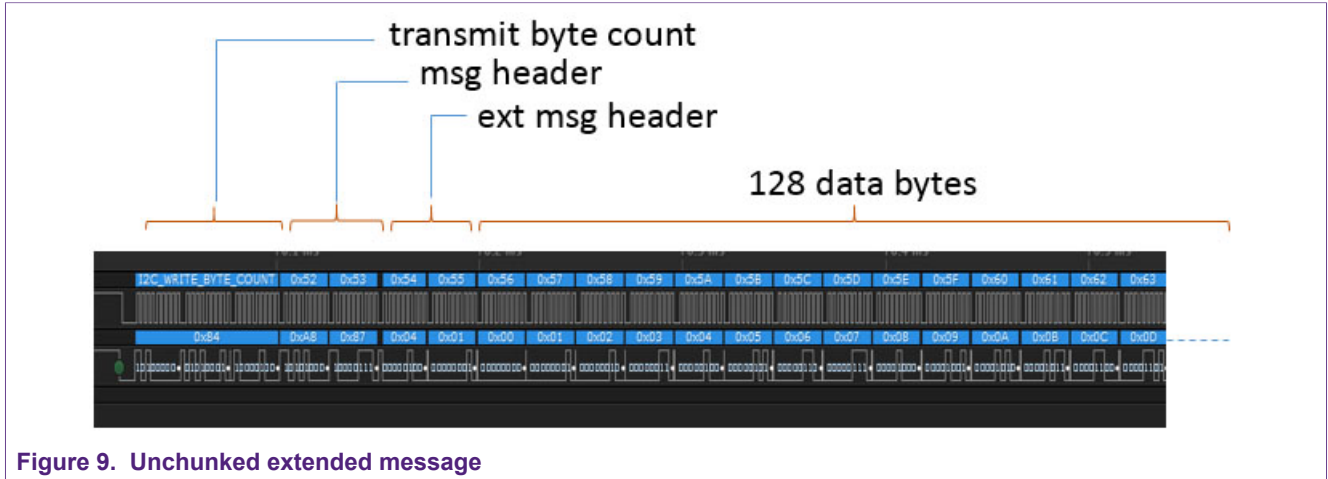


Figure 9. Unchunked extended message

7.1.3 Receiving an unchunked extended message

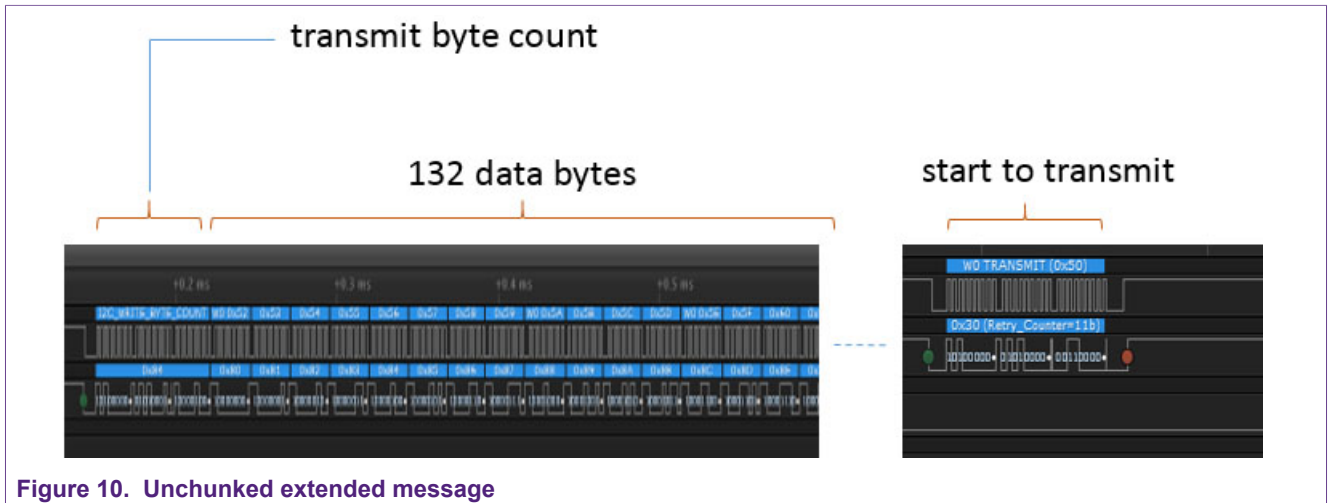


Figure 10. Unchunked extended message

7.2 Fast Role Swap (FRS)

PTN5110N supports FRS generation as well as FRS detection. PTN5110N has an output pin called FRS_EN that can be used to arm a power switching device such as the NX5P3290 to get it ready to source 5V quickly.

FRS is automated by the PTN5110N. Once the initial source TCPM sends a command to start FRS, PTN5110N automatically takes the active CC line low for approximately 100µS. The PTN5110N on the initial sink automatically asserts FRS_EN, disables

the EN_SNK1 signal and asserts EN_SRC signal. An FRS received interrupt is also generated and the interrupt status is reported in the EXT_ALERT register.

7.2.1 Original source initiates an FRS

1. Writes command 0x66 to TCPC COMMAND register (0x23) to disable sourcing VBUS
2. Writes command 0xCC to TCPC COMMAND register (0x23) to start FRS (to tell PTN5110N to start FRS process)
3. Writes command 0x55 to TCPC COMMAND register to enable the sink FET
4. WAIT FOR FRS REQUEST from the initial sink (Laptop, etc.)
5.
6. Receives FRS request message
7. Sends Accept
8. Sends PSRdy
9. After that, normal PD communication will occur

7.2.2 Original sink response to an FRS

1. Enables FRS detection using POWER_CONTROL register 'Fast Role Swap Enable' bit.
2. Receives FRS interrupt (EXTEND_STATUS register)
3. Clears FRS received interrupt (EXTEND_STATUS register)
4. Sends FRS REQUEST message through PD communication
5. WAIT FOR ACCEPT from the initial source
6. Receives accept
7. Waits for PSRdy
8. Receives PSRdy
9. Sends PSRdy
10. Sends Source Cap to start normal PD communication for an attachment

7.3 AMS (Auto Message Sequence)

AMS is supported by the PTN5110N based on the methodology of using Rp as described in USB PD 3.0 specification[1]. The source shall set an Rp value corresponding to a current of 3A to indicate to the sink that it may initiate AMS. The source shall set an Rp value corresponding to a current of 1.5A to indicate to the sink that it shall not initiate an AMS, and shall respond to messages as part of an AMS.

Table 2. Rp values used to initiate AMS

Source Rp	Parameter	Description	Sink operation	Source operation
1.5A@5V	<i>SinkTxNG</i>	Sink Transmit "No Go",	Sink cannot initiate an AMS. Sink can only respond to messages as part of an AMS	Source can initiate an AMS <i>tSinkTx</i> after setting Rp to this value
3A@5V	<i>SinkTxOk</i>	Sink Transmit "Ok"	Sink can initiate an AMS	Source cannot initiate an AMS while it has this value set

8 Register listing and description

Table 3. Register listing and description

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
00h	VENDOR_ID	Read Only Word	0x1FC9	15:0	Vendor ID A unique 16-bit unsigned integer. Assigned by the USB-IF to the Vendor.	Required	
02h	PRODUCT_ID	Read Only Word	0x5110	15:0	USB Product ID A unique 16-bit unsigned integer. Assigned uniquely by the Vendor to identify the TCPC.		
04h	DEVICE_ID	Read Only Word	0x0004	15:0	bcdDevice A unique 16-bit unsigned integer. Assigned by the Vendor to identify the version of the TCPC.		
06h	USBTYPEC_REV	Read Only Word	0x0012	15:8	Reserved		
				7:0	USB Type-C Revision Version number assigned by USB-IF 0001 0001b : Type-C Revision 1.1 0001 0010b : Type-C Revision 1.2		
08h	USBPD_REV_VER	Read Only Word	0x3011	15:8	bcdUSBPD Revision 0010 0000b : USBPD Revision 2.0 0011 0000b : USBPD Revision 3.0		Supported
				7:0	bcdUSBPD Version 0001 0000b : USBPD Version 1.0 0001 0001b : USBPD Version 1.1 Etc.		
0Ah	PD_INTERFACE_REV	Read Only Word	0x2010	15:8	bcd USB-PD Inter-Block Specification Revision 0001 0000 : TCPC Revision 1.0 0010 0000 : TCPC Revision 2.0 (this release)		
				7:0	bcd USB-PD Inter-Block Specification Version 0001 0000 : TCPC Version 1.0 0001 0001 : TCPC Version 1.1 0001 0010 : TCPC Version 1.2 Etc.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
0Ch-0Fh	Reserved	N/A	0x0000	N/A	Reserved		
10h	ALERT	Read / Write Word	0x0000	15	Vendor Defined Extended 0b: No vendor defined alert occurred 1b: Read EXT_ALERT to determine the source of the vendor defined alert. Writing 1 to this bit will clear only this bit, EXT_ALERT must also be cleared to de-assert ALERT_N.	Required	Supported
				14	Alert Extended 0b: Cleared 1b: An extended interrupt event has occurred. Read the ALERT_EXTENDED register.		
				13	Extended Status 0b: Cleared, 1b: Extended Status changed		
				12	Beginning SOP* Message Status READABLE_BYTE_COUNT is 133; this is just the beginning of an extended USB PD message with more than 128 data bytes. This bit is not set if READABLE_BYTE_COUNT is less than 133. 0b: Cleared, 1b: RECEIVE_BUFFER register changed. READABLE_BYTE_COUNT being set to 0 does not set this bit.		
				11	VBUS Sink Disconnect Detected 0b: Cleared 1b: Detected This bit shall only be asserted when POWER_CONTROL.AutoDischargeDisconnect is set		
				10	Rx Buffer Overflow 0b: TCPC Rx buffer is functioning properly 1b: TCPC Rx buffer has overflowed Writing 1 to this register acknowledges the overflow. The overflow is cleared by writing to ALERT.ReceiveSOP*MessageStatus		

Offset	Name	Type	Default Value	Bit field	Description	TCP/PC Required/Optional	Datasheet Requirement
				9	Fault 0b: No Fault 1b: Fault Occurred. Read the FAULT_STATUS register		
				8	VBUS Voltage Alarm Lo 0b: Cleared 1b: Occured. A low-voltage alarm has occurred		
				7	VBUS Voltage Alarm Hi 0b: Cleared 1b: Occured. A high-voltage alarm has occurred		
				6	Transmit SOP* Message successful 0b: Cleared, 1b: Successful. Reset or message transmitted. Transmission successful. GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers are empty.		
				5	Transmit SOP* Message discarded 0b: Cleared, 1b: Discarded. Reset or SOP* message transmission not sent due to incoming receive message. Transmit SOP* message buffer registers is not full.		
				4	Transmit SOP* Message failed 0b: Cleared, 1b: Message transmission failed. no GoodCRC response received on SOP* message transmission. Transmit SOP* message buffer registers is not full.		
				3	Received Hard Reset 0b: Cleared, 1b: Received Hard Reset message		
				2	Received SOP* Message Status 0b: Cleared, 1b: Receive status register changed READABLE_BYTE_COUNT being set to 0 does not set this bit.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				1	Port Power Status 0b: Cleared 1b: Port status changed		
				0	CC Status Alert 0b: Cleared 1b: CC status changed Note: _Alert suffix added to differentiate from CC_Status register clearly in code generation TCPC shall not assert this bit when CC_STATUS.Looking4Connection changes state if TCPC_CONTROL.EnableLooking4ConnectionAlert is set to 0.		
12h	ALERT_MASK	Read / Write Word	0x7FFF	15	Vendor Defined Extended Masked 0b: Interrupt masked (EXT_ALERT_MASK must also be 0 to completely unmask all vendor defined alerts) 1b: Interrupt unmasked	Required	Supported
				14	Alert Extended Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				13	Extended Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				12	Beginning SOP* Message Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				11	VBUS Sink Disconnect Detected Masked 0b: Interrupt masked 1b: Interrupt unmasked		
				10	Rx Buffer Overflow Masked 0b: Interrupt masked 1b: Interrupt unmasked		

Offset	Name	Type	Default Value	Bit field	Description	TCP/PC Required/Optional	Datasheet Requirement
				9	Fault Masked 0b: Interrupt masked 1b: Interrupt unmasked		
				8	VBUS Voltage Alarm Lo Masked 0b: Interrupt masked 1b: Interrupt unmasked		
				7	VBUS Voltage Alarm Hi Masked 0b: Interrupt masked 1b: Interrupt unmasked		
				6	Transmit SOP* Message successful Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				5	Transmit SOP* Message discarded Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				4	Transmit SOP* Message failed Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				3	Received Hard Reset Message Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked (The Hard Reset should generally not be masked)		
				2	Receive SOP* Message Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				1	Port Power Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		

Offset	Name	Type	Default Value	Bit field	Description	TCP/PC Required/Optional	Datasheet Requirement
				0	Cc Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
14h	POWER_STATUS_MASK	Read / Write Byte	0xFF	7	Debug Accessory Connected Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked	Required	Supported
				6	TCP/PC Initialization Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				5	Source High Voltage Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				4	Source VBUS Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				3	VBUS Present Detection Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				2	VBUS Present Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				1	VCONN Present Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				0	Sink VBUS Connected Status Interrupt Mask 0b: Interrupt masked 1b: Interrupt unmasked		

Offset	Name	Type	Default Value	Bit field	Description	TCP/PC Required/Optional	Datasheet Requirement
15h	FAULT_STATUS_MASK	Read / Write Byte	0xFF	7	All Registers Reset To Default Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked The condition that generates a FAULT_STATUS.AllRegistersResetToDefault Interrupt also resets this bit; therefore, writing a 0b to this bit will not mask FAULT_STATUS.AllRegistersResetToDefault Interrupt	Required	Supported
				6	Force Off VBUS Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				5	Auto Discharge Failed Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				4	Force Discharge Failed Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				3	VBUS Over Current Protection Fault Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				2	VBUS Over Voltage Protection Fault Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				1	VCONN Over Current Fault Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				0	I2C Interface Error Interrupt Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		
				7:1	Reserved Shall be set to zero by sender and ignored by receiver		
16h	EXTENDED_STATUS_MASK	Read / Write Byte	0xFF	7:1	Reserved Shall be set to zero by sender and ignored by receiver	Register Required	

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				0	vSafe0V Status Mask 0b: Interrupt masked 1b: Interrupt unmasked		Supported
17h	ALERT_EXTENDED_MASK	Read/Write Byte	0xFF	7:3	Reserved Shall be set to zero by sender and ignored by receiver	Register Required	
				2	Timer Expired Mask 0b: Interrupt masked 1b: Interrupt unmasked		Supported
				1	Source Fast Role Swap Mask 0b: Interrupt masked 1b: Interrupt unmasked		Supported
				0	Sink Fast Role Swap Mask 0b: Interrupt masked 1b: Interrupt unmasked		Supported
18h	CONFIGURE_STANDARD_OUTPUT	Read/Write Byte	0x60	7	High Impedance outputs 0b: Standard output control 1b: Force all outputs to High Impedance May be used to save power in Sleep Controlled by the TCPM.	Optional Normative	Supported
				6	Debug Accessory Connected# 0b: Debug Accessory Connected# output is driven low 1b: Debug Accessory Connected# output is driven high If TCPC_CONTROL.DebugAccessoryControl = 0, the TCPC shall write to this register and ignore inputs from TCPM If TCPC_CONTROL.DebugAccessoryControl = 1, the TCPC shall take input from the TCPM		Supported
				5	Audio Accessory Connected 0b: Audio Accessory connected 1b: No Audio Accessory connected (default) Controlled by the TCPM		Not supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				4	Active Cable Connected 0b: No Active Cable connected 1b: Active Cable connected Controlled by the TCPM		
				3:2	MUX Control 00b: No connection. 01b: USB3.1 Connected 10b: DP Alternate Mode : 4 lanes 11b: USB3.1 + Display Port Lanes 0 & 1 Controlled by the TCPM		
				1	Connection Present 0b: No Connection 1b: Connection Controlled by the TCPM		
				0	Connector Orientation GPIO0 0b: Normal (CC1=A5, CC2=B5, TX1=A2/A3, RX1=B10/B11) default 1b: Flipped (CC2=A5, CC1=B5, TX1=B2/B3, RX1=A10/A11) If TCPC_CONTROL.DebugAccessoryControl = 0, the TCPC shall write to this register and ignore inputs from TCPM If TCPC_CONTROL.DebugAccessoryControl = 1, the TCPC shall take input from the TCPM		Supported
19h	TCPC_CONTROL	Read / Write Byte	0x00	7	Enable SMBus PEC 0b: SMBus PEC is disabled (default) 1b: SMBus PEC is enabled Enables SMBus PEC according to TCPC Spec.		Not supported
				6	Enable Looking4Connection Alert 0b: Disable ALERT.CcStatus assertion when CC_STATUS.Looking4Connection changes (default) 1b: Enable ALERT.CcStatus assertion when CC_STATUS.Looking4Connection changes	Register Required	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				5	Enable Watchdog Timer 0b: Watchdog Monitoring is disabled (default) 1b: Watchdog Monitoring is enabled Enables Watchdog Timer Monitoring according to TCPC Spec Required if DEVICE_CAPABILITIES_2.Watch Dog Timer = 1b		Supported
				4	Debug Accessory Control 0b: Controlled by TCPC (power on default) 1b: Controlled by TPCM. The TPCM writes 1b to this register to take over control of asserting the DebugAccessoryConnected#. Required (Register is required but output is not required)		Supported
				3:2	I2C Clock Stretching Control Clock Stretching Control 00b: Disable clock stretching. TCPC shall not perform any clock stretching during I2C transfers. 01b: Reserved 10b: Enable clock stretching. TCPC is allowed limited clock stretching during each I2C Transfer. 11b: Enable clock stretching only if the Alert pin is not asserted. As soon as Alert is asserted, clock stretching is disabled by the TCPC. The TCPC datasheet should contain details as to the power consequences of clock stretching as well as the max duration of clock stretching per I2C transaction. This is only necessary if clock stretching is implemented. The TCPC shall limit total clock stretching as detailed in TCPC Spec I2C Physical Interface Specifications. This feature is optional. The TCPC is allowed to ignore updates to this bit field if it has not implemented clock stretching. The power on default value is such to disable clock stretching.		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				1	<p>BIST Test Mode</p> <p>Setting this bit to 1 is intended to be used only when a USB compliance tester is using USB BIST Test Data to test the PHY layer of the TCPC. The TCPM should clear this bit when a detach is detected.</p> <p>0: Normal Operation. Incoming messages enabled by RECEIVE_DETECT passed to TCPM via Alert.</p> <p>1: BIST Test Mode. Incoming messages enabled by RECEIVE_DETECT result in GoodCRC response but may not be passed to the TCPM via Alert. TCPC may temporarily store incoming messages in the Receive Message Buffer, but this may or may not result in a Receive SOP* Message Status or a Rx Buffer Overflow alert.</p> <p>The TCPM can mask or ignore received message alerts when this bit is set to 1 since the TCPC may or may not assert the alert. The TCPM may also treat received messages in this mode in the same way as received messages during normal operation.</p>		Supported
				0	<p>Plug Orientation</p> <p>0b: When Vconn is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled.</p> <p>1b: When Vconn is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled.</p> <p>Required</p>		Supported
1Ah	ROLE_CONTROL	Read / Write Byte	Set according to MTP	7	<p>Reserved</p> <p>Shall be set to zero by sender, shall be ignored by receiver.</p>		
				6	<p>DRP</p> <p>0b: No DRP. Bits B3..0 determine Rp/Rd/Ra or open settings</p> <p>1b: DRP</p> <p>The TCPC shall use the Rp value defined in B5..4 when a connection is resolved, ie. Upon entry to Potential_Connect_as_Src in TCPC Spec Figure "TCPC State Machine before a Connection".</p> <p>The TCPC toggles CC1 & CC2 after receiving COMMAND.Look4Connection and until a connection is detected. Upon connection, the TCPC shall resolve to either an Rp or Rd and report the CC1/CC2 State in the CC_STATUS register.</p> <p>The CC pins shall stay in Potential_start_as_SRC or Potential_start_as_Sink until directed otherwise.</p>	Required	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCP/PC Required/Optional	Datasheet Requirement
				5:4	Rp Value 00b: Rp default 01b: Rp 1.5A 10b: Rp 3.0A 11b: Reserved		
				3:2	CC2 00b: Ra 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don't care) Set to 11b if enabling DRP in B7..6		
				1:0	CC1 00b: Ra 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (Disconnect or don't care) Set to 11b if enabling DRP in B7..6		
1Bh	FAULT_CONTROL	Read / Write Byte	0x00	7:5	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				4	Force Off VBUS Enable 0b: Force Off VBUS circuit enabled 1b: Force Off VBUS circuit disabled Note that the STANDARD INPUT SIGNAL Force Off Vbus (4.5.1) has the same behavior as writing to this bit. Optional Normative	Partial Required	Supported
				3	VBUS Discharge Timer 0b: VBUS Discharge Timer enabled 1b: VBUS Discharge Timer disabled Optional Normative		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				2	VBUS Over Current Protection Fault Enable 0b: Internal and External OCP circuit enabled 1b: Internal and External OCP circuit disabled The TCPC shall not disconnect VBUS due to internal OCP.		Not supported
				1	VBUS Over Voltage Protection Fault Enable 0b: Internal and External OVP circuit enabled 1b: Internal and External OVP circuit disabled The TCPC shall not disconnect VBUS due to internal OVP.		Supported
				0	VCONN Over Current Fault Enable 0b: Fault detection circuit enabled 1b: Fault detection circuit disabled Required if DEVICE_CAPABILITIES_2.VCONNOvercurrentFaultCapable = 1b		Not supported
1Ch	POWER_CONTROL	Read / Write Byte	0x60	7	Fast Role Swap Enable 0b: Disable Fast Role Swap function 1b: Enable Fast Role Swap function Sink TCPC shall support this bit if DEVICE_CAPABILITIES_2.SinkFRSwap = 1b. Source TCPC shall support this bit if DEVICE_CAPABILITIES_2.SourceFRSwap = 1b. The detailed functional requirements for Source and Sink TCPCs supporting Fast Role Swap are provided in TCPC Spec. <i>Additional PTN5110 Specific Behaviour:</i> - Assert the FRS_EN pin while this bit is set - Enable detection of the FRS signal on CC by the PHY - Once FRS is detected, monitor the vbus voltage, and control the EN_SNK* and EN_SRC pins according to the USBPD3.0 spec <i>While enabled</i> - The FRO clock will always be enabled - The ADC will be enabled to monitor VBUS When 0b EXT_GPIO_CONFIG.FRS_EN can be used to control the FRS_EN pin independent of the Fast Role Swap feature.	Partial Required	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				6	<p>VBUS_VOLTAGE Monitor</p> <p>0b: VBUS_VOLTAGE Monitoring is enabled</p> <p>1b: VBUS_VOLTAGE Monitoring is disabled (default)</p> <p>Controls only VBUS_VOLTAGE Monitoring. VBUS_VOLTAGE shall report all zeros if disabled.</p> <p>Optional Normative</p>		
				5	<p>Disable Voltage Alarms</p> <p>0b: Voltage Alarms Power status reporting is enabled</p> <p>1b: Voltage Alarms Power status reporting is disabled (default)</p> <p>Controls VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG.</p> <p>Required if DEVICE_CAPABILITIES_1.VBUSMeasuremen andAlarmCapable = 1b</p>		
				4	<p>AutoDischargeDisconnect</p> <p>0b: The TCPC shall not automatically discharge VBUS based on VBUS voltage (default)</p> <p>1b: The TCPC shall automatically discharge</p> <p>Setting this bit in a Source TCPC triggers the following actions upon disconnection detection:</p> <ol style="list-style-type: none"> 1. Disable sourcing power over VBUS 2. VBUS discharge <p>Sourcing power over VBUS shall be disabled before or at the same time as starting VBUS discharge.</p> <p>Setting this bit in a Sink TCPC triggers the following action upon disconnection detection:</p> <ol style="list-style-type: none"> 1. VBUS discharge <p>The TCPC shall automatically disable discharge (without clearing this bit) once the voltage on VBUS is below vSafe0V (max) or VBUS_STOP_DISCHARGE_THRESHOLD.VBUS_STOP_DISCHARGE_THRESHOLD, if enabled, takes priority over vSafe0V. TCPC shall not re-apply discharge circuit if VBUS rises above VBUS_STOP_DISCHARGE_THRESHOLD or vSafe0V.</p> <p>Required</p>		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				3	Enable Bleed Discharge 0b: Disable bleed discharge (default) 1b: Enable bleed discharge of VBUS Bleed Discharge is a low current discharge to provide a minimum load current if needed 10K Ohms maximum or 2mA minimum Optional Normative		
				2	Force Discharge 0b: Disable forced discharge (default) 1b: Enable forced discharge of VBUS. Optional Normative		
				1	VCONN Power Supported 0b: TCPC delivers at least 1W on VCONN 1b: TCPC delivers at least the power indicated in DEVICE_CAPABILITIES.VCONNPowerSupported Refer to TCPC datasheet for actual power limit implemented Optional Normative		
				0	Enable VCONN 0b: Disable VCONN Source (default) 1b: Enable VCONN Source to CC Required		
1Dh	CC_STATUS	Read Only Byte	0x00	7:6	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				5	Looking4Connection 0b: the TCPC has stopped toggling or (ROLE_CONTROL.DRP=00) 1b: the TCPC is toggling		
				4	ConnectResult 0b: the TCPC is presenting Rp 1b: the TCPC is presenting Rd This bit is only valid if the TCPC was a DRP and has stopped DRP toggling.	Required	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				3:2	<p>CC2 State</p> <p>If (ROLE_CONTROL.CC2=Rp) or (ConnectResult=0)</p> <p>00b: SRC_Open (Open, Rp)</p> <p>01b: SRC_Ra (below maximum vRa)</p> <p>10b: SRC_Rd (within the vRd range)</p> <p>11b: reserved</p> <p>If (ROLE_CONTROL.CC2=Rd) or (ConnectResult=1)</p> <p>00b: SNK_Open (Below maximum vRa)</p> <p>01b: SNK_Default (Above minimum vRd-Connect)</p> <p>10b: SNK_Power1_5 (Above minimum vRd-Connect) Detects Rp 1.5A</p> <p>11b: SNK_Power3_0 (Above minimum vRd-Connect) Detects Rp 3.0A</p> <p>If ROLE_CONTROL.CC2=Ra, this field is set to 00b</p> <p>If ROLE_CONTROL.CC2=Open, this field is set to 00b</p> <p>This field always returns 00b if (Look4Connection=1) or (POWER_CONTROL.EnableVconn=1 and TCPC_CONTROL.PlugOrientation=1). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.</p>		
				1:0	<p>CC1 State</p> <p>If (ROLE_CONTROL.CC1 = Rp) or (ConnectResult=0)</p> <p>00b: SRC_Open (Open, Rp)</p> <p>01b: SRC_Ra (below maximum vRa)</p> <p>10b: SRC_Rd (within the vRd range)</p> <p>11b: reserved</p> <p>If (ROLE_CONTROL.CC1 = Rd) or ConnectResult=1)</p> <p>00b: SNK_Open (Below maximum vRa)</p> <p>01b: SNK_Default (Above minimum vRd-Connect)</p> <p>10b: SNK_Power1_5 (Above minimum vRd-Connect) Detects Rp-1.5A</p> <p>11b: SNK_Power3_0 (Above minimum vRd-Connect) Detects Rp-3.0A</p> <p>If ROLE_CONTROL.CC1=Ra, this field is set to 00b</p> <p>If ROLE_CONTROL.CC1=Open, this field is set to 00b</p> <p>This field always returns 00b if (Look4Connection=1) or (POWER_CONTROL.EnableVconn=1 and TCPC_CONTROL.PlugOrientation=0). Otherwise, the returned value depends upon ROLE_CONTROL.CC1.</p>		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
1Eh	POWER_STATUS	Read Only Byte	0x48				
				7	Debug Accessory Connected 0b: No Debug Accessory connected (default) 1b: Debug Accessory connected Autonomously controlled by the TCPC or controlled by the TCPM. Decision if controlled by the TCPC or TCPM is set in the TCPC_CONTROL register. Optional Normative		
				6	TCPC Initialization Status 0b: The TCPC has completed initialization and all registers are valid 1b: The TCPC is still performing internal initialization and the only registers that are guaranteed to return the correct values are 00h..-0Fh Required		
				5	Sourcing High Voltage 0b: vSafe5V 1b: High Voltage This bit does not control the path, just provides a monitor of the status. Assert as long as supplying voltage greater than vSafe5V. Required if voltage higher than vSafe5V can be sourced This bit is not valid if POWER_STATUS.SourcingVbus = 0b.	Required	Supported
				4	Sourcing VBUS 0b: Sourcing VBUS is disabled 1b: Sourcing VBUS is enabled This does not control the path, just provides a monitor of the status. Required		
				3	VBUS Detection Enabled 0b: VBUS Detection Disabled 1b: VBUS Detection Enabled (default) Indicates whether the TCPC is monitoring for VBUS Present and vSafe0V level, or the detection circuits have been powered off Required		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				2	<p>VBUS Present 0b: VBUS Disconnected 1b: VBUS Connected</p> <p>The TCPC shall report VBUS present when TCPC detects VBUS rises above 4V. The TCPC shall report VBUS is not present when TCPC detects VBUS falls below 3.5V. The TCPC may report VBUS is not present if VBUS is between 3.5V and 4V. This bit is not valid when POWER_STATUS.VbusDetectionEnabled = 0b. Required</p>		
				1	<p>VCONN Present 0b: VCONN is not present 1b: This bit is asserted when VCONN present CC1 or CC2. Threshold is fixed at 2.4V Required</p>		
				0	<p>Sinking VBUS 0b: Sink is Disconnected (Default and if not supported) 1b: TCPC is sinking VBUS to the system load Required</p>		
1Fh	FAULT_STATUS	Read / Write Byte	0x80	7	<p>All Registers Reset To Default 0b: No Fault detected 1b: All Registers Reset To Default fault latched This bit is asserted when the TCPC resets all registers to their default value. This happens at initial power up or if an unexpected power reset occurs.</p>	Required	Supported
				6	<p>Force Off VBUS Status 0b: No Fault Detected, no action (default and not supported) 1b: VBUS Source/Sink has been forced off due to external fault The TCPC has disconnected VBUS due to STANDARD_INPUT.ForceOffVbus. Required if STANDARD_INPUT_CAPABILITIES_1.ForceOffVbus = 1b</p>		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				5	Auto Discharge Failed 0b: No discharge failure 1b: Discharge commanded by the TCPM failed If POWER_CONTROL.AutoDischargeDisconnect is set, the TCPC shall report discharge fails if Vbus is not below vSafe0V within tSafe0V. Required		
				4	Force Discharge Failed 0b: No discharge failure 1b: Discharge commanded by the TCPM failed If POWER_CONTROL.ForceDischarge is set, the TCPC shall report a discharge fails if Vbus is not below vSafe0V within tSafe0V. Required if DEVICE_CAPABILITIES_1.ForceDischarge =1b		
				3	Internal or External VBUS Over Current Protection Fault 0b: Not in an over-current protection state 1b: Over-current fault latched Required if DEVICE_CAPABILITIES_1.VBUSOCPReporting = 1b		
				2	Internal or External VBUS Over Voltage Protection Fault 0b: Not in an over-voltage protection state 1b: Over-voltage fault latched. Required if DEVICE_CAPABILITIES_1.VBUSOVPRreporting = 1b		
				1	VCONN Over Current Fault 0b: No Fault detected 1b: Over current VCONN fault latched Required if DEVICE_CAPABILITIES_2.VCONNOvercurrentFaultCapable = 1b		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				0	I2C Interface Error 0b: No Error 1b: I2C error has occurred. Some of the conditions for asserting this bit: • TPCM writes to the TRANSMIT register when the TRANSMIT_BUFFER is empty • The watchdog timer has expired • TPCM writes an invalid COMMAND • TPCM writes a non-zero value to a reserved bit in a register • TPCM writes to the TRANSMIT_BUFFER when TCPC is transmitting the Fast Role Swap signal as triggered by the STANDARD INPUT signal Source Fast Role Swap • TPCM writes to CONFIG_EXTENDED1.FRSwapBidirectionalPin and STANDARD_INPUT_CAPABILITIES.SourceFastRoleSwap is not 10b Required		
20h	EXTENDED_STATUS	Read Only Byte	0x00	7:1	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				0	vSafe0V 0b: VBUS is not at vSafe0V 1b: VBUS is at vSafe0V The TCPC shall report VBUS is at vSafe0V when TCPC detects VBUS is below 0.8V. This bit is not valid when POWER_STATUS.VbusDetectionEnabled = 0b. Required <i>PTN5110 Specific:</i> <i>Latency for rising edge and falling edge will be different. Rising edge (VBUS enters vSafe0V region) will meet tSetReg, falling edge will have a larger latency and may not update until vbus rises to vbus present region.</i>	Required	Supported
21h	ALERT_EXTENDED	Read / Write Byte	0x00	7:3	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Required	

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				2	Timer Expired 0b: Generic timer is not expired 1b: Generic timer has expired		Supported
				1	Source Fast Role Swap 0b: No Fast Role Swap signal sent 1b: Fast Role Swap signal sent due to STANDARD INPUT Source Fast Role Swap is set low		Not supported
				0	Sink Fast Role Swap 0b: No Fast Role Swap signal received 1b: Fast Role Swap signal received		Supported
22h	Reserved	N/A	0x00	N/A	Reserved		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
23h	COMMAND	Write Only Byte	0x00	7:0	<p>Command</p> <p>0001 0001b : Wakel2C (no action is taken other than to wake the I2C interface).</p> <p>0010 0010b : DisableVbusDetect. Disable Vbus present detection. The TCPC shall ignore this command and assert the FAULT_STATUS.I2CInterfaceError if it has sourcing or sinking power over Vbus enabled.</p> <p>0011 0011b : EnableVbusDetect. Enable Vbus present detection.</p> <p>0100 0100b : DisableSinkVbus. Disable sinking power over Vbus. This COMMAND does not disable POWER_STATUS.VBUSPresent detection.</p> <p>0101 0101b : SinkVbus. Enable sinking power over Vbus and enable Vbus present detection. The TCPC shall ignore this command and assert the FAULT_STATUS.I2CInterfaceError if it has sourcing power over Vbus enabled.</p> <p>0110 0110b : DisableSourceVbus. Disable sourcing power over Vbus. The TCPC shall stop reporting FAULT_STATUS. Internal or External OCP or OVP Faults. This COMMAND does not disable POWER_STATUS.VBUSPresent detection.</p> <p>0111 0111b : SourceVbusDefaultVoltage. Enable sourcing vSafe5V over Vbus and enable Vbus present detection. Source shall transition to vSafe5V if at a high voltage. The TCPC shall ignore this command and assert the FAULT_STATUS.I2CInterfaceError if it has sinking power over Vbus enabled.</p> <p>1000 1000b : SourceVbusHighVoltage. Execute sourcing high voltage over Vbus. The TCPC shall ignore this command and assert the FAULT_STATUS.I2CInterfaceError if it is either does not have ability to source voltages higher than vSafe5V or is already sourcing vSafe5V. The actual voltage to be sourced may be set in a vendor defined manner. The TCPM may need to send vendor defined commands before sending this COMMAND.</p>	Required	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
					<p>1001 1001b : Look4Connection. Start DRP Toggling if ROLE_CONTROL.DRP=1b. If ROLE_CONTROL.CC1/CC2 = 01b start with Rp, if ROLE_CONTROL.CC1/CC2 =10b start with Rd. If ROLE_CONTROL.CC1/CC2 are not both 01b or 10b, then do not start toggling.</p> <p>1010 1010b : RxOneMore. Configure the receiver to automatically clear the RECEIVE_DETECT register after sending the next GoodCRC. This is used to shutdown reception of packets at a known point regardless of packet separation or the depth of the receive FIFO in the TCPC.</p> <p>1100 1100b : SendFRSwapSignal. Source TCPC sends Fast Role Swap signal within tTCPCSendFRSwap after receiving this command if POWER_CONTROL.FastRoleSwapEnable = 1b. TCPC shall ignore this command and assert the FAULT_STATUS.I2CinterfaceError if POWER_CONTROL.FastRoleSwapEnable = 0b.</p> <p>1101 1101b : ResetTransmitBuffer. The TCPC resets the pointer of the TRANSMIT_BUFFER register and the contents of TRANSMIT_BUFFER becomes invalid when this command is issued by the TPCM. This command shall be supported by TCPC compliant with USB Port Controller Specification Revision 2.0,</p> <p>1110 1110b : ResetReceiveBuffer. The TCPC resets the pointer of RX_BUFFER when this command is issued by the TPCM. TCPC does not clear the content of the buffer upon receiving this command. The TPCM issues this command in order to re-read the RECEIVE_BUFFER.RX_BUF_BYTE_x. This command shall be supported by TCPC compliant with USB Port Controller Specification Revision 2.0,</p> <p>1111 1111b : I2C Idle</p>		
24h	DEVICE_CAPABILITIES_1	Read Only Word	0x7EDF	15	<p>VBUS High Voltage Target</p> <p>0b: VBUS_HV_TARGET register not implemented (default)</p> <p>1b: VBUS_HV_TARGET register implemented</p>		Not supported
				14	<p>VBUS OCP Reporting</p> <p>0b: VBUS OCP is not reported by the TCPC</p> <p>1b: VBUS OCP is reported by the TCPC</p> <p>Support for both FAULT_STATUS.InternalorExternalOCP and FAULT_CONTROL. InternalorExternalOCP implemented</p>	Required	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				13	VBUS OVP Reporting 0b: VBUS OVP is not reported by the TCPC 1b: VBUS OVP is reported by the TCPC Support for both FAULT_STATUS.InternalorExternalOVP and FAULT_CONTROL. InternalorExternalOVP implemented		Supported
				12	BleedDischarge 0b: No Bleed Discharge implemented in TCPC 1b: Bleed Discharge is implemented in the TCPC Support for POWER_CONTROL.EnableBleedDischarge implemented		Supported
				11	ForceDischarge 0b: No Force Discharge implemented in TCPC 1b: Force Discharge is implemented in the TCPC Support for POWER_CONTROL.ForceDischarge, FAULT_STATUS.ForceDischargeFailed, and VBUS_STOP_DISCHARGE_THRESHOLD implemented Support for VBUS_STOP_DISCHARGE_THRESHOLD register implemented when act as Source		Supported
				10	VBUS Measurement and Alarm Capable 0b: No VBUS voltage measurement nor VBUS Alarms 1b: VBUS voltage measurement and VBUS Alarms Reported in VBUS_VOLTAGE, VBUS_VOLTAGE_ALARM_HI_CFG, and VBUS_VOLTAGE_ALARM_LO_CFG Registers		Supported
				9:8	Source Resistor supported 00b: Rp default only 01b: Rp 1.5A and default 10b: Rp 3.0A, 1.5A, and default 11b: Reserved Rp values which may be configured by the TCPM via the ROLE_CONTROL register		Supported

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Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				7:5	Roles Supported 000b: Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001b: Source only 010b: Sink only 011b: Sink with accessory support 100b: DRP only 101b: Source, Sink, DRP, Adapter/Cable all supported 110b: Source, Sink, DRP 111b: Not valid		Source, Sink, DRP. Supported
				4	SOP'_DBG/SOP''_DBG Support 0b: All SOP* except SOP'_DBG/SOP''_DBG 1b: All SOP* messages are supported Configured in RECEIVE_DETECT and TRANSMIT		Supported
				3	Source VCONN 0b: TCPC is not capable of switching VCONN 1b: TCPC is capable of switching VCONN Support for POWER_CONTROL.EnableVCONN and POWER_STATUS.VCONNPresent implemented		Supported
				2	Sink VBUS 0b: TCPC is not capable controlling the sink path to the system load 1b: TCPC is capable of controlling the sink path to the system load Support for POWER_STATUS.SinkingVbus, COMMAND.SinkVbus, and COMMAND.DisableSinkVbus implemented		Supported
				1	Source High Voltage VBUS 0b: TCPC is not capable of controlling the source high voltage path to VBUS 1b: TCPC is capable of controlling the source high voltage path to VBUS Support for VBUS_VOLTAGE, POWER_STATUS.SourcingHighVoltage, and COMMAND.SourceVbusHighVoltage implemented NOTE: DEVICE_CAPABILITIES_1.VBUS Measurement and Alarm Capable shall be set to 1b if Source High Voltage VBUS is enabled		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				0	Source VBUS 0b: TCPC is not capable of controlling the source path to VBUS 1b: TCPC is capable of controlling the source path to VBUS Support for POWER_STATUS.SourcingVbus, COMMAND.SourceVbusDefaultVoltage, COMMAND.DisableSourceVbus, COMMAND.EnableVbusDetect and COMMAND.DisableVbusDetect implemented		Supported
26h	DEVICE_CAPABILITIES_2	Read Only Word	0x37C7	15:14	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Required	
				13	Generic Timer 0b: GENERIC_TIMER register is not supported 1b: GENERIC_TIMER register is supported		Supported
				12	Long Message 0b: TCPC is only capable of passing 30 bytes content of the SOP* message 1b: TCPC is capable of passing 264 bytes content of the SOP* message. TRANSMIT_BUFFER is capable to hold 264 bytes content of the SOP* message. The TCPM can write up to 132 bytes to the TX_BUF_BYTE_x in one burst. RECEIVE_BUFFER is sized to hold a 264 bytes content SOP* message plus a 30 bytes content SOP* message.		Supported
				11	SMBus PEC 0b: TCPC_CONTROL.EnableSMBusPEC not implemented 1b: TCPC_CONTROL.EnableSMBusPEC implemented		Not supported
				10	Source FR Swap 0b: Not capable of sending Fast Role Swap signal as Source TCPC when receiving COMMAND.SendFRSwapSignal or when STANDARD INPUT Source Fast Role Swap is set low. 1b: Capable of sending Fast Role Swap signal as Source TCPC when receiving COMMAND.SendFRSwapSignal. If STANDARD_INPUT_CAPABILITIES.SourceFRSwap = 1b, capable of sending Fast Role Swap signal as Source TCPC when STANDARD INPUT Source Fast Role Swap is set low.		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				9	Sink FR Swap 0b: POWER_CONTROL.FastRoleSwapEnable not supported as Sink TCPC 1b: POWER_CONTROL.FastRoleSwapEnable supported as Sink TCPC		Supported
				8	Watchdog Timer 0b: TCPC_CONTROL.Enable Watchdog Timer not implemented 1b: TCPC_CONTROL.Enable Watchdog Timer implemented		Supported
				7	Sink Disconnect Detection 0b: VBUS_SINK_DISCONNECT_THRESHOLD not implemented (default: Use POWER_STATUS.VbusPresent=0b to indicate a Sink disconnect) 1b: VBUS_SINK_DISCONNECT_THRESHOLD implemented		Supported
				6	Stop Discharge Threshold 0b: VBUS_STOP_DISCHARGE_THRESHOLD not implemented (default) 1b: VBUS_STOP_DISCHARGE_THRESHOLD implemented		Supported
				5:4	VBUS Voltage Alarm LSB 00b: TCPC has 25mV LSB for its voltage alarm and uses all 10 bits in VBUS_VOLTAGE_ALARM_HI_CFG and VBUS_VOLTAGE_ALARM_LO_CFG. 01b: TCPC has 50mV LSB for its voltage alarm and uses only 9 bits. VBUS_VOLTAGE_ALARM_HI_CFG[0] and VBUS_VOLTAGE_ALARM_LO_CFG[0] are ignored by TCPC. 10: TCPC has 100mV LSB for its voltage alarm and uses only 8 bits. VBUS_VOLTAGE_ALARM_HI_CFG[1:0] and VBUS_VOLTAGE_ALARM_LO_CFG[1:0] are ignored by TCPC. 11: reserved Support for VBUS_VOLTAGE_ALARM_LO_CFG and VBUS_VOLTAGE_ALARM_HI implemented		Default supported.

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				3:1	VCONN Power Supported 000b: 1.0W 001b: 1.5W 010b: 2.0W 011b: 3W 100b: 4W 101b: 5W 110b: 6W 111b: External		External Supported.
				0	VCONN Overcurrent Fault Capable 0b: TCPC is not capable of detecting a Vconn fault 1b: TCPC is capable of detecting a Vconn fault Support for FAULT_STATUS.VCONNOverCurrentFault and FAULT_CONTROL.VCONNOverCurrentFault implemented		Supported
28h	STANDARD_INPUT_CAPABILITIES	Read Only Byte	0x06	7:5	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				4:3	Source Fast Role Swap 00b: Not present in TCPC 01b: Present in TCPC as an input only pin 10b: Present in TCPC as a bidirectional pin, sharing with the STANDARD_OUTPUT signal Vbus Sink Disconnect Detect Indicator. The "Vbus Sink Disconnect Detect Indicator" bit in STANDARD_OUTPUT_CAPABILITIES register shall also be set to 1. 11b: Reserved	Required	Not supported
				2	Vbus External Over Voltage Fault Capable 0b: Not present in TCPC 1b: Present in TCPC		Supported
				1	Vbus External Over Current Fault Capable 0b: Not present in TCPC 1b: Present in TCPC		Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				0	Force Off VBUS Capable (Source or Sink) 0b: Not present in TCPC 1b: Present in TCPC		Supported
29h	STANDARD_OUTPUT_CAPABILITIES	Read Only Byte	0x40	7	Vbus Sink Disconnect Detect Indicator 0b: Not present in TCPC 1b: Present in TCPC Shall present in TCPC if “Source Fast Role Swap” in STANDARD_INPUT_CAPABILITIES is set to 10b ((present as a bidirectional pin)).	Required	Not supported
				6	Debug Accessory Indicator 0b: Not present in TCPC 1b: Present in TCPC		Supported
				5	Vbus Present Monitor 0b: Not present in TCPC 1b: Present in TCPC		Not supported
				4	Audio Adapter Accessory Indicator 0b: Not present in TCPC 1b: Present in TCPC		Not supported
				3	Active Cable Indicator 0b: Not present in TCPC 1b: Present in TCPC		Not supported
				2	MUX Configuration Control 0b: Not present in TCPC 1b: Present in TCPC		Not supported
				1	Connection Present Indicator 0b: Not present in TCPC 1b: Present in TCPC		Not supported
				0	Connector Orientation 0b: Not present in TCPC 1b: Present in TCPC		Not supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
2Ah	CONFIGURE_EXTENDED1	Read / Write Byte	0x00	7:2	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Optional Normative	Not supported
				1	FR Swap Bidirectional Pin 0b: The bidirectional pin is configured as STANDARD INPUT signal Source Fast Role Swap (default) 1b: The bidirectional pin is configured as STANDARD OUTPUT signal Vbus Sink Disconnect Detect Indicator The TCPC shall ignore TCPM writing to this bit and assert FAULT_STATUS.I2CinterfaceError if STANDARD_INPUT_CAPABILITIES.SourceFastRoleSwap is not set to 10b (present as a bidirectional pin), and STANDARD_OUTPUT_CAPABILITIES.VbusSinkDisconnectDetectIndicator is not set to 1.		
				0	Standard Input Source FR Swap 0b: Allow STANDARD INPUT signal Source Fast Role Swap to trigger sending Fast Role Swap signal (default) 1b: Block STANDARD INPUT signal Source Fast Role Swap to trigger sending Fast Role Swap signal This bit enables or disables STANDARD INPUT signal Source Fast Role Swap functionality. Required if STANDARD_INPUT_CAPABILITIES.SourceFastRoleSwap is set to either 01b or 10b (present).		
2Bh	Reserved	N/A		N/A	Reserved		
2Ch	GENERIC_TIMER	Write Only Word	0x0000	15:0	Timer Value 16-bit timer value with 0.1ms LSB. A non-zero value starts the timer. A value of zero stops the timer. The timer does not restart after it has expired. Required if DEVICE_CAPABILITIES_2.GenericTimer = 1b.	Optional Normative	Supported
2Eh	MESSAGE_HEADER_INFO	Read / Write Byte	0x02	7:5	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Required	Supported
				4	Cable Plug 0b: Message originated from Source, Sink, or DRP 1b: Message originated from a Cable Plug		

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Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				3	Data Role 0b: UFP 1b: DFP		
				2:1	USB PD Specification Revision 00b: Revision 1.0 01b: Revision 2.0 (NOTE - As USBPD 2.0 requires this value, the TCPM should select this even when it has support for USBP3.0, unless the partner also supports USBPD3.0) 10b: Revision 3.0 (NOTE - USBPD 3.0 allows GoodCRC to use any value except 11b reserved) 11b: Reserved		
				0	Power Role 0b: Sink 1b: Source		
2Fh	RECEIVE_DETECT	Read / Write Byte	0x00	7	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				6	Enable Cable Reset 0b: TCPC does not detect Cable Reset signaling (default) 1b: TCPC detects Cable Reset signaling		
				5	Enable Hard Reset 0b: TCPC does not detect Hard Reset signaling (default) 1b: TCPC detects Hard Reset signaling		
				4	Enable SOP_DBG_PP message 0b: TCPC does not detect SOP_DBG" message (default) 1b: TCPC detects SOP_DBG" message	Required	Supported
				3	Enable SOP_DBG_P message 0b: TCPC does not detect SOP_DBG' message (default) 1b: TCPC detects SOP_DBG' message		
				2	Enable SOP_PP message 0b: TCPC does not detect SOP" message (default) 1b: TCPC detects SOP" message		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				1	Enable SOP_P message 0b: TCPC does not detect SOP' message (default) 1b: TCPC detects SOP' message		
				0	Enable SOP message 0b: TCPC does not detect SOP message (default) 1b: TCPC detects SOP message		
30h	READABLE_BYTE_COUNT	Read Only Byte	0x00	7:0	Indicates the number of bytes in the RX_BUF_BYTE_x registers plus one (for the RX_BUF_FRAME_TYPE). The content of this register is undefined when the RECEIVE_BUFFER is cleared		
	RX_BUF_FRAME_TYPE	Read Only Byte	0x00	7:3	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				2:0	Received SOP* Message 000b: Received SOP 001b: Received SOP' 010b: Received SOP" 011b: Received SOP_DBG' 100b: Received SOP_DBG" 110b: Received Cable Reset All others are reserved. Type of received frame. This register is "hidden" and can only be accessed by reading at address 30h.	Required	Supported
	RX_BUF_BYTE_x	Read Only Byte	0x00		Receive Buffer Bytes. These registers are "hidden" and can only be accessed by reading at address 30h.		
50h	TRANSMIT	Read/Write Byte	0x00	7:6	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				5:4	Retry Counter 00b: No message retry is required 01b: Automatically retry message transmission once 10b: Automatically retry message transmission twice 11b: Automatically retry message transmission three times	Required	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
				3	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				2:0	Transmit SOP* message 000b: Transmit SOP 001b: Transmit SOP' 010b: Transmit SOP'' 011b: Transmit SOP_DBG' 100b: Transmit SOP_DBG'' 101b: Transmit Hard Reset 110b: Transmit Cable Reset 111b: Transmit BIST Carrier Mode 2 (TCPC shall exit the BIST mode no later than tBISTContMode max)		
51h	I2C_WRITE_BYTE_COUNT	Write Only Byte	0x00	7:0	The number of bytes the TCPM intends to write to the TX_BUF_BYTE_x in the given I2C/SMBus transaction.	Required	Supported
	TX_BUF_BYTE_x	Write Only Byte	0x00		Transmit Buffer Bytes. These registers are "hidden" and can only be accessed by writing to address 51h.	Required	Supported
70h	VBUS_VOLTAGE	Read Only Word	0x0000	15:12	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				11:10	Vbus Scale Factor 00: VBUS measurement not scaled. 01: VBUS measurement divided by 2 10: VBUS measurement divided by 4 11: reserved	Optional Normative	Supported
				9:0	VBUS voltage measurement 10-bit measurement of (VBUS / Scale Factor) TCPM multiplies this value by the scale factor to obtain the voltage measurement. Voltages greater than or equal to 4V shall meet +/-2% absolute value or +/- 50mV, whichever is greater. The LSB is 25mV.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
72h	VBUS_SINK_DISCONNECT_THRESHOLD	Read / Write Word	0x008C	15:10	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Required	Supported
				9:0	Vbus Sink Disconnect trip point (Default 3.5V) 10-bit for voltage threshold with 25mV LSB. +/- 5% accuracy. The TCPC may ignore B0 or B1 & B0 depending upon DEVICE_CAPABILITIES_2.VbusVoltageAlarmLsb.		
74h	VBUS_STOP_DISCHARGE_THRESHOLD	Read / Write Word	0x0020	15:10	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Required	Supported
				9:0	Vbus Stop Discharge trip point (Default 0.8V) 10-bit for voltage threshold with 25mV LSB. +/- 5% accuracy. The TCPC may ignore B0 or B1 & B0 depending upon DEVICE_CAPABILITIES_2.VbusVoltageAlarmLsb.		
76h	VBUS_VOLTAGE_ALARM_HI_CFG	Read / Write Word	0x0000	15:10	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Optional	Supported
				9:0	Vbus Lo Voltage trip point 10-bit for voltage threshold with 25mV LSB. +/- 5% accuracy. The TCPC may ignore B0 or B1 & B0 depending upon DEVICE_CAPABILITIES_2.VbusVoltageAlarmLsb.		
78h	VBUS_VOLTAGE_ALARM_LO_CFG	Read / Write Word	0x0000	15:10	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Normative	Supported
				9:0	Vbus Hi Voltage trip point 10-bit for voltage threshold with 25mV LSB. +/- 5% accuracy. The TCPC may ignore B0 or B1 & B0 depending upon DEVICE_CAPABILITIES_2.VbusVoltageAlarmLsb.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
7Ah	VBUS_HV_TARGET	Read / Write Word	0x0000	15:0	VBUS voltage target 16-bit for the VBUS voltage target with 20mV LSB. +/- 5% accuracy. The TCPC shall ignore if the value is less than 5.5V (113h) or DEVICE_CAPABILITIES_1.VbusHighVoltageTarget is set to 0b.	Optional Normative	Not supported
7Ch-7 Fh	Reserved	N/A	0x0000	N/A	Reserved		
80h	EXT_CFG_ID	Read Only Word	NA	15:0	For NXP Internal Use Only	Vendor Defined	Supported
82h	EXT_ALERT	Read / Write Word	0x0000	15:8	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				7	GPIO Status Change 0b: Cleared 1b: An GPIO status change has occurred, read the EXT_GPIO_STATUS register. Only IILIM_5V_VBUS can be configured to raise an alert on change. See EXT_GPIO_CONFIG and EXT_GPIO_ALERT_CONFIG.		
				6:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
84h	EXT_ALERT_MASK	Read / Write Word	0x0000	15:8	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				7	GPIO Status Change 0b: Interrupt masked (default) 1b: Interrupt unmasked		
				6:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
86h	EXT_CONFIG	Read / Write Word	0x0000	15:7	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				6:4	Reserved Shall be set to zero by sender, shall be ignored by receiver.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				3:2	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				1:0	Automatic Discharge for Negative Transition (Controls the behaviour when executing the COMMAND.SourceVbusDefaultVoltage some time after executing COMMAND.SourceVbusHighVoltage, while still connected.) 00b : Set EN_SNK1=0, Discharge to 5V, Set EN_SRC=1 (default) 01b : Set EN_SNK1=0, Discharge to VBUS_STOP_DISCHARGE_THRESHOLD, Set EN_SRC=1 10b : Set EN_SNK1=0, Automatic discharge disabled, Allow TCPM to use force discharge, when ADC monitors 5V set EN_SRC=1 11b: Reserved		
88h	EXT_FAULT_CONFIG	Read / Write Byte	0x1F	7:4	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				4	Open Fets On ADC Alarm 0b: Do not open fets on ADC Alarm 1b: Open FETs (EN_SNK1, EN_SRC) on ADC Alarm (High or Low) (Default)		
				3	VCONN Over Current Limit Enable (OCL) 0b: OCL and SCL Fault detection circuit disabled 1b: OCL and SCL Fault detection circuit enabled (Default) when FAULT_CONTROL.VCONN Over Current Fault set to Enabled (0) (Default) This register should be left at the default value for normal operation. VCONN Short Circuit Protection (SCP) is also enabled/disabled by this bit. FAULT_CONTROL.VCONN Over Current Fault Must also be set to Enabled (0). this register must be set before enabling the vconn switch or while FAULT_CONTROL.VCONN Over Current Fault is disabled.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				2	VCONN Over Temperature Fault Enable (OTF) 0b: OTF Fault detection circuit disabled 1b: OTF Fault detection circuit enabled (Default) when FAULT_CONTROL.VCONN Over Current Fault set to Enabled (0) (Default) This register should be left at the default value for normal operation. FAULT_CONTROL.VCONN Over Current Fault Must also be set to Enabled (0), this register must be set before enabling the vconn switch or while FAULT_CONTROL.VCONN Over Current Fault is disabled.		
				1	Reserved Shall be set to 1 by sender, shall be ignored by receiver.		
				0	VCONN Reverse Current Fault Enable (RCP) 0b: RCP Fault detection circuit disabled 1b: RCP Fault detection circuit enabled (Default) when FAULT_CONTROL.VCONN Over Current Fault set to Enabled (0) (Default) This register should be left at the default value for normal operation. FAULT_CONTROL.VCONN Over Current Fault Must also be set to Enabled (0), this register must be set before enabling the vconn switch or while FAULT_CONTROL.VCONN Over Current Fault is disabled.		
89h	Reserved	Read / Write Byte	0x00	7:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Not Supported
8ah	Reserved	Read /Write Word	0x0000	15:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Not Supported
8ch	Reserved	Read /Write Word	0x0000	15:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Not Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/ Optional	Datasheet Requirement
8eh	EXT_CONTROL	Read /Write Byte	0x60	7:4	Bleed Discharge Strength (Only applied on write to POWER_CONTROL) 0001b : Select 3.2K Ohm typical (+/- 15%) pulldown resistor to ground on Vbus 0010b : Select 8K Ohm typical (+/- 15%) pulldown resistor to ground on Vbus 0100b : Select 20K Ohm typical (+/- 15%) pulldown resistor to ground on Vbus 1000b : Select 50 KOhm typical (+/- 15%) pulldown resistor to ground on Vbus Other values - resistors are applied in parallel: 0110b : 5.7K Ohm (+/- 15%) (Select 8K Ohm and 20K Ohm) pulldown resistor to ground on Vbus (Default) This register does not enable the bleed discharge. This value must be changed before writing to POWER_CONTROL.Enable Bleed Discharge.	Vendor Defined	Supported
				3	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				2:1	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				0	VCONN Force Discharge 0b: VCONN discharge path is disabled. 1b: VCONN switch is disabled and the discharge path is enabled. The VCONN discharge path will be automatically disabled when the VCONN Voltage completes discharge to vVCONNDISCHARGE, however the TCPM must clear this bit manually, after waiting tVCONNDISCHARGE. When using this bit to control a VCONN discharge, a read-modify-write should be used to ensure the other fields are not changed. This should always be cleared to 0 before writing POWER_CONTROL.Enable VCONN = 1.		
8fh	Reserved	Write Only Byte	0x00	7:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Not Supported
90h	EXT_STATUS	Read Only Word	0x0000	15:5	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				4	VCONN Over Current Limit Fault Status (OCL) 0b: No Fault detected 1b: Over current VCONN fault latched Only valid when FAULT_STATUS.VCONN Over Current Fault is 1		
				3	VCONN Over Temperature Fault Status (OTF) 0b: No Fault detected 1b: Over temperature VCONN fault latched Only valid when FAULT_STATUS.VCONN Over Current Fault is 1		
				2	VCONN Short Circuit Fault Status (SCF) 0b: No Fault detected 1b: Short circuit VCONN fault latched Only valid when FAULT_STATUS.VCONN Over Current Fault is 1		
				1	VCONN Reverse Current Fault Status (RCP) 0b: No Fault detected 1b: Reverse current VCONN fault latched Only valid when FAULT_STATUS.VCONN Over Current Fault is 1		
				0	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
92h	EXT_GPIO_CONFIG	Read / Write Byte	0x03	7	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				6	FRS_EN 0b : Input Pin, Output will be set according to POWER_CONTROL.Fast Role Swap Enable (default) 1b : Output Pin To change only 1 pin mode the TCPM must do a read-modify-write. POWER_CONTROL.Fast Role Swap Enable always has priority over this field.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				5	EN_SRC 0b : Controlled by COMMAND.SourceVbusDefaultVoltage (default) 1b : Output Pin To change only 1 pin mode the TCPM must do a read-modify-write. This register should be left at the default value for standard TCPC operation.		
				4	EN_SNK1 0b : Controlled by COMMAND.SinkVbus or COMMAND.SourceVbusHighVoltage (default) 1b : Output Pin To change only 1 pin mode the TCPM must do a read-modify-write. This register should be left at the default value for standard TCPC operation.		
				3	IILIM_5V_VBUS 0b : Input Pin 1b : Output Pin To change only 1 pin mode the TCPM must do a read-modify-write.		
				2:0	Reserved Shall be set to 0x3 by sender, shall be ignored by receiver.		
93h	EXT_GPIO_CONTROL	Read / Write Byte	0x00	7:2	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				6	FRS_EN 0b : Drive Low, Unless POWER_CONTROL.Fast Role Swap Enable is set. 1b : Drive High (Only when EXT_GPIO_CONFIG.FRS_EN = 1 and POWER_CONTROL.Fast Role Swap Enable = 0) POWER_CONTROL.Fast Role Swap Enable always has priority over this field. To change only 1 pin value the TCPM must do a read-modify-write.		

Offset	Name	Type	Default Value	Bit field	Description	TCPM Required/Optional	Datasheet Requirement
				5	EN_SRC 0b : Drive Low 1b : Drive High (Only when EXT_GPIO_CONFIG.EN_SRC = 1) To change only 1 pin value the TCPM must do a read-modify-write.		
				4	EN_SNK1 0b : Drive Low 1b : Drive High (Only when EXT_GPIO_CONFIG.EN_SNK1 = 1) To change only 1 pin value the TCPM must do a read-modify-write.		
				3	IILIM_5V_VBUS 0b : Drive Low 1b : Drive High (Only when EXT_GPIO_CONFIG.IILIM_5V_VBUS = 1) To change only 1 pin value the TCPM must do a read-modify-write.		
				2:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
94h	EXT_GPIO_ALERT_CONFIG			15:6	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
		Read /Write Word	0x0038	5:3	IILIM_5V_VBUS 000b: Active Low Level Sensitive 001b: Active High Level Sensitive 010b: Rising Edge Triggered 011b: Falling Edge Triggered 100b: Triggered on both edges 101b: Reserved 110b: Reserved 111b: Disable Interrupt (default)		
				2:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
96h	EXT_GPIO_STATUS	Read Only Byte	undefined	7	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				6	FRS_EN 0b : Pin is low (or input disabled) 1b : Pin is high		
				5:4	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				3	IILIM_5V_VBUS 0b : Pin is low (or input disabled) 1b : Pin is high		
				2:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
97h	SOURCE_HIGH_VOLTAGE_MB4B_TIME	Read / Write Byte	Device Specific PTN5110 HQ/PTN5110DHQ: 0x1E PTN5110THQ: 0x00	7:0	Source High Voltage Make Before Break Time (ms). Controls the behaviour when the TCPM issues the SourceVbusHighVoltage command: 0 : Break before make: Disable the EN_SRC and then enable EN_SNK1 immediately. 1-255 : Make before break: Time, in milliseconds(ms), EN_SRC and EN_SNK1 will both be enabled immediately, then after this time EN_SRC is disabled and EN_SNK1 only enabled.	Vendor Defined	Supported
98h	Reserved	Read Only Byte	0x00	7:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Not Supported
99h	Reserved	Read Only Byte	0x00	7:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Not Supported
9Ah	ADC_FILTER_CONTROL_1	Read / Write Byte	0x00	7:0	ADC Voltage Filter Control - Controls the amount of debounce/filtering performed on the ADC voltage threshold detects. This is used for the Vbus Over and Vbus Under Voltage Alarms. 0 : Disabled. No debouncing/filtering is performed 1 - 255 : The measured voltage must be beyond the threshold (above for high thresholds, below for low thresholds) for ADC_FILTER_CONTROL_1*256 us before the condition is considered true and an interrupt asserted.	Vendor Defined	Supported

Offset	Name	Type	Default Value	Bit field	Description	TCP/PC Required/Optional	Datasheet Requirement
9Bh	ADC_FILTER_CONTROL_2	Read / Write Byte	0x13	7:0	ADC Voltage Filter Control - Controls the amount of debounce/filtering performed on the ADC voltage threshold detects. This is used for the Vbus Sink Disconnect Alarm. 0 : Disabled. No debouncing/filtering is performed 1 - 255 : The measured voltage must be beyond the threshold for ADC_FILTER_CONTROL_2 * 256 us before the condition is considered true and an interrupt asserted. 0x13: 4.9ms (default)	Vendor Defined	Supported
9Ch	VCONN_CONFIG	Read / Write Byte	0x02	7	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				6	VCONN OCL Switch Open Enable 0b: Keep sourcing current on VCONN, with the current limited. (Default) 1b: Open the switch and alert the host that a fault has occurred.		
				5	VCONN_SelfClearCtrl_Temp Controls the behaviour when a VCONN switch over temperature fault occurs. 0b: Stop sourcing current on VCONN, raise a FAULT_STATUS.VCONN Over Current Fault. (Default) 1b: The device waits for VCONN_TempFault_FaultRecovery time before reclosing the Vconn switch. This is attempted VCONN_NumVconnAttempts_TempFault times. If the fault persists then raise FAULT_STATUS.VCONN Over Current Fault.		
				4	Reserved Shall be set to zero by sender, shall be ignored by receiver.		
				3	VCONN_SelfClearCtrl_RCP Controls the behaviour when a VCONN switch reverse current fault occurs. 0b: Stop sourcing current on VCONN, raise a FAULT_STATUS.VCONN Over Current Fault. (Default) 1b: The device waits for VCONN_RCP_FaultRecovery time before reclosing the Vconn switch. This is attempted VCONN_NumVconnAttempts_RCP times. If the fault persists then raise FAULT_STATUS.VCONN Over Current Fault.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
				2:0	VCONN_OCL_Threshold This specifies the Vconn current limiting threshold. 000b : 150 mA 001b : 300 mA 010b : 450 mA (Default) 011b : 600 mA 1xxb : Reserved (Typical values, see datasheet for Min/Max)		
9Dh	VCONN_FAULT_DEBOUNCE	Read / Write Byte	0x08	7:6	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Supported
				5:2	VCONN_RCP_FaultDebounce This controls how long a Vconn RCP must be present for it to be considered valid. 0001b : ~12 us 0010b : ~36 us (Default) 0011b : ~60 us 0100b : ~100 us 0101b : ~200 us 0110b : ~500 us 0111b : ~1000 us 1000b : ~2 ms 1001b : ~5 ms 1010b : ~10 ms 1011b : ~20 ms 11xxb : ~50 ms		
				1:0	Reserved Shall be set to zero by sender, shall be ignored by receiver.		

Offset	Name	Type	Default Value	Bit field	Description	TCPC Required/Optional	Datasheet Requirement
9Eh	VCONN_FAULT_RECOVERY	Read / Write Byte	0x11	7:4	VCONN_TempFault_FaultRecovery 0000b : 0ms 0001b: 500ms (Default) 0010b: 1000ms 0011b-1111b: Reserved This specifies the amount of time the switch is to be opened after an Temperature fault is detected before the switch can be reclosed. Each value represents 500 ms. The min value is 0. The max value is 1s.	Vendor Defined	Supported
				3:0	VCONN_RCP_FaultRecovery 0000b : 0ms 0001b: 500ms (Default) 0010b: 1000ms 0011b: 1500ms 0100b: 2000ms 0101b: 2500ms 0110b: 3000ms 0111b: 3500ms 1000b: 4000ms 1001b: 4500ms 1010b: 5000ms 1011b-1111b: Reserved This specifies the amount of time the switch is to be opened after an RCP fault is detected before the switch can be reclosed. Each value represents 500 ms. The min value is 0. The max value is 5s.		

Offset	Name	Type	Default Value	Bit field	Description	TCPM Required/Optional	Datasheet Requirement
9Fh	VCONN_FAULT_ATTEMPTS	Read / Write Byte	0x00	7:4	VCONN_NumVconnAttempts_TempFault 0 : Stop sourcing current on VCONN, raise a FAULT_STATUS.VCONN Over Current Fault. (Default) 1-16 : Number of times to attempt to recovery from the over temperature fault. This is the number of attempts the device will try to close the Vconn switch before giving up and alerting the TCPM. After each fault occurrence, the device will increment an internal counter and reclose the Vconn switch. If the counter exceeds VCONN_NumVconnAttempts then the switch will still be closed but the TCPM will be alerted with the FAULT_STATUS.VCONN Over Current Fault. The internal counter is cleared each time the TCPM request for the Vconn switch to be closed.	Vendor Defined	Supported
				3:0	VCONN_NumVconnAttempts_RCP 0 : Stop sourcing current on VCONN, raise a FAULT_STATUS.VCONN Over Current Fault. (Default) 1-16 : Number of times to attempt to recovery from the reverse current fault. This is the number of attempts the device will try to close the Vconn switch before giving up and alerting the TCPM. After each fault occurrence, the device will increment an internal counter and reclose the Vconn switch. If the counter exceeds VCONN_NumVconnAttempts then the switch will not be closed and the TCPM will be alerted with the FAULT_STATUS.VCONN Over Current Fault. The internal counter is cleared each time the TCPM request for the Vconn switch to be closed.		
A0h-F Fh	Reserved	N/A	0x0000	N/A	Reserved Shall be set to zero by sender, shall be ignored by receiver.	Vendor Defined	Not Supported

9 References

- | | | |
|---|---|--|
| 1 | USB Power Delivery Specification | Revision 3.0, Version 1.1 January 2017 |
| 2 | USB Type-C Cable and Connector Specification | Revision 1.2, March 25, 2016 |
| 3 | USB Type-C Port Controller Interface Specification | Revision 2.0, Version 1.0, Oct 2017 |

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