AN12204

Power consumption and measurement of i.MX RT1020

Rev. 1 — 11 February 2020 Application Note

Contents

1 Introduction

This document describes the power consumption of i.MX RT1020.

- i.MX RT1020 overview
- Run mode definition and configuration
- Low-power mode definition and configuration
- How to measure power consumption based on MIMXRT1020 EVK Board
- Power consumption under different power modes

The development environment in this application note is IAR Embedded Workbench. The software version is SDK 2.6.1. The hardware environment is MIMXRT1020 EVK Board (Rev A2).

2 Chip overview

2.1 i.MX RT1020 overview

The i.MX RT1020 is a Cortex-M7 based chip that operates at speed up to 500 MHz to provide high CPU performance and best real-time response.

- 256 KB on-chip RAM which can be flexibly configured as TCM or general-purpose on-chip RAM.
- Advanced power management module with DCDC and LDO to reduce complexity of external power supply and simplifies power sequencing.
- Rich memory interfaces, including SDRAM, Raw NAND FLASH, NOR FLASH, SD/eMMC, and FlexSPI.
- Various interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS.
- Audio features including SPDIF and I2S audio interface.
- Provide rich peripheral modules, such as SPI, I2C, Can, Ethernet, Flex-Timers, and ADC.
- Target at Industrial HMI, Motor Control, and Home Appliance areas.

3 Low power overview

3.1 Power supply

Table 1 below shows the power supply rails of i.MX RT1020.

Table 1. External power supply rails

Power Rail	Description	MIN(V)	TYP(V)	MAX(V)
DCDC_IN	Power for DCDC.	3	3.3	3.6
SOC_IN	Power for SOC.	0.925	-	1.3
VDD_HIGH_IN	Power for Analog.	3	3.3	3.6
VDD_SNVS_IN	Power for SNVS and RTC.	2.4	3.0	3.6
USB_OTG_VBUS	Power for USB VBUS.	4.4	5.0	5.5
VDDA_ADC_3P3	Power for 12-bit ADC.	3	3.3	3.6
NVCC_SD0	Power for GPIO in SDIO1 bank (3.3 V mode).	3	3.3	3.6
	Power for GPIO in SDIO1 bank (1.8 V mode).	1.65	1.8	1.95
NVCC_GPIO	IO Power for GPIO in GPIO bank.	3	3.3	3.6

3.2 Run mode

3.2.1 Run mode definition

Table 2. Run mode definition

Run Mode	Definition
Overdrive Run	• CPU runs at 500 MHz, overdrive voltage to 1.275 V • Bus frequency at 125 MHz • All the peripheral is enabled and runs at target frequency • All PLLs are enabled
Full Speed Run	• CPU runs at 396 MHz, full loading, lower voltage to 1.15 V • Bus frequency at 132 MHz • All the peripheral is enabled and runs at target frequency • All PLLs are enabled
Low Speed Run	• CPU runs at 132 MHz, lower voltage to 1.15 V • Internal bus frequency at 33 MHz • All PLL and PFDs are disabled except SYSPLL, SYSPLLPFD2, and SYSPLLPFD3 • 20 % peripheral are active, others are in low-power mode
Low-Power Run	• CPU runs at 24 MHz, lower voltage to 0.95 V

Table 2. Run mode definition (continued)

Run Mode	Definition
	• Internal bus frequency at 12 MHz • All PLLs are powered down, OSC24M powered down, RCOSC24 enabled • High-speed peripherals are power down

In general, Run mode can be divided in four modes as shown in above table. The Low-speed run mode uses the bus clock of Full-speed run mode as core clock. The Low-power run mode uses 24 MHz internal OSC as core clock source.

3.2.2 Run mode configuration

Table 3. Run mode configuration

	Overdrive Run	Full Speed Run	Low Speed Run	Low-Power Run
CPU Core	500 MHz	396 MHz	132 MHz	24 MHz
L1 Cache	ON	ON	ON	ON
IPG CLK	125 MHz	132 MHz	33 MHz	12 MHz
PEG CLK	62.5 MHz	66 MHz	33 MHz	12 MHz
FlexRAM	ON	ON	ON	ON
SOC Voltage	1.275 V	1.15 V	1.15 V	0.95 V
Analog LDO	ON	ON	ON	In Weak Mode
24 MHz XTAL OSC	ON	ON	ON	OFF
24 MHz RC OSC	OFF	OFF	OFF	ON
SYS PLL	ON	ON	ON	Power Down
SYS PFD0	ON	ON	Power Down	Power Down
SYS PFD1	ON	ON	Power Down	Power Down
SYS PFD2	ON	ON	ON	Power Down
SYS PFD3	ON	ON	ON	Power Down
USB1 PLL	ON	ON	Power Down	Power Down
USB1 PFD0	ON	ON	Power Down	Power Down
USB1 PFD1	ON	ON	Power Down	Power Down
USB1 PFD2	ON	ON	Power Down	Power Down

Table continues on the next page...

Table 3. Run mode configuration (continued)

	Overdrive Run	Full Speed Run	Low Speed Run	Low-Power Run
USB1 PFD3	ON	ON	Power Down	Power Down
Audio PLL	ON	ON	Power Down	Power Down
ENET PLL	ON	ON	Power Down	Power Down
Module Clock	ON	ON	On as needed	Peripheral clock off
RTC32K	ON	ON	ON	ON

3.3 Low power modes

3.3.1 Low power mode definition

Table 4. Low power mode definition

Low Power Mode	Definition
System Idle	• CPU can automatically enter this mode when no thread running • All the peripheral can remain active • CPU only enter WFI mode, it will have its state retained so the interrupt response can be very short
Low Power Idle	• Much lower power than System Idle mode, with longer exit time • All PLLs are shut off, analog modules running in low power mode • All high-speed peripherals are power gated, low speed peripherals can remain running at low frequency
Suspend	• The most power saving mode with longest exit time • All PLLs are shut off, XTAL are off, all clocks are shut off except 32K clock • All high-speed peripherals are power gated, low speed peripherals are clock gated
SNVS	• All SOC digital logic, analog modules are shut off only except SNVS domain • 32KHz RTC is alive • VDD_HIGH_IN and VDD_DCDC_IN can be powered off

3.3.2 Low power mode configuration

Table 5. Low power mode configuration

	System Idle	Low Power Idle	Suspend	SNVS
CCM LPM Mode	WAIT	WAIT	STOP	-
CPU Core	WFI	WFI	Power Down	OFF
L1 Cache	ON	ON	Power Down	OFF
FlexRAM	ON	ON	ON	OFF
SOC Voltage	1.15V	0.95V	0.925V	OFF
SYS PLL	ON	Power Down	Power Down	OFF
SYS PFD0	Power Down	Power Down	Power Down	OFF
SYS PFD1	Power Down	Power Down	Power Down	OFF
SYS PFD2	ON	Power Down	Power Down	OFF
SYS PFD3	ON	Power Down	Power Down	OFF
USB1 PLL	Power Down	Power Down	Power Down	OFF
USB1 PFD0	Power Down	Power Down	Power Down	OFF
USB1 PFD1	Power Down	Power Down	Power Down	OFF
USB1 PFD2	Power Down	Power Down	Power Down	OFF
USB1 PFD3	Power Down	Power Down	Power Down	OFF
Audio PLL	Power Down	Power Down	Power Down	OFF
ENET PLL	Power Down	Power Down	Power Down	OFF
24MHz XTAL OSC	ON	OFF	OFF	OFF
24MHz RC OSC	OFF	ON	OFF	OFF
LDO2P5	ON	OFF	OFF	OFF
LDO1P1	ON	OFF	OFF	OFF
WEAK2P5	OFF	ON	OFF	OFF
WEAK1P1	OFF	ON	OFF	OFF
Bandgap	ON	OFF	OFF	OFF
Low Power Bandgap	ON	ON	ON	OFF

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Table 5. Low power mode configuration (continued)

	System Idle	Low Power Idle	Suspend	SNVS
AHB clock	33MHz	12MHz	OFF	OFF
IPG clock	33MHz	12MHz	OFF	OFF
PER clock	33MHz	12MHz	OFF	OFF
Module Clocks	ON as needed	ON as needed	OFF	OFF
RTC32K	ON	ON	ON	ON

3.3.3 Wake up source

Table 6. Wake up source

	System Idle	Low Power Idle	Suspend	SNVS
GPIO wake-up	YES	YES	YES	YES (1 pin only)
RTC wake-up	YES	YES	YES	YES
USB remote wake-up	YES	YES	YES	NO
Other peripheral wake-up sources	YES	YES	YES	NO

NOTE

Irrespective of whether the system is in System Idle, Low-Power Idle or Suspend modes, the wake-up interrupt should be enabled in GPC module. The only pin that can wake up the system in SNVS is IOMUXC_SNVS_WAKEUP_GPIO5_IO00. Peripheral wake-up requires that the clock for the peripheral is available in the mode.

4 How to measure power consumption on MIMXRT1020 EVK

4.1 Current measurements on EVK

The POR_B pin has an internal pullup, R22 and R179 should be removed. Leaving these resistors populated causes higher SNVS current than what is shown in this application note.

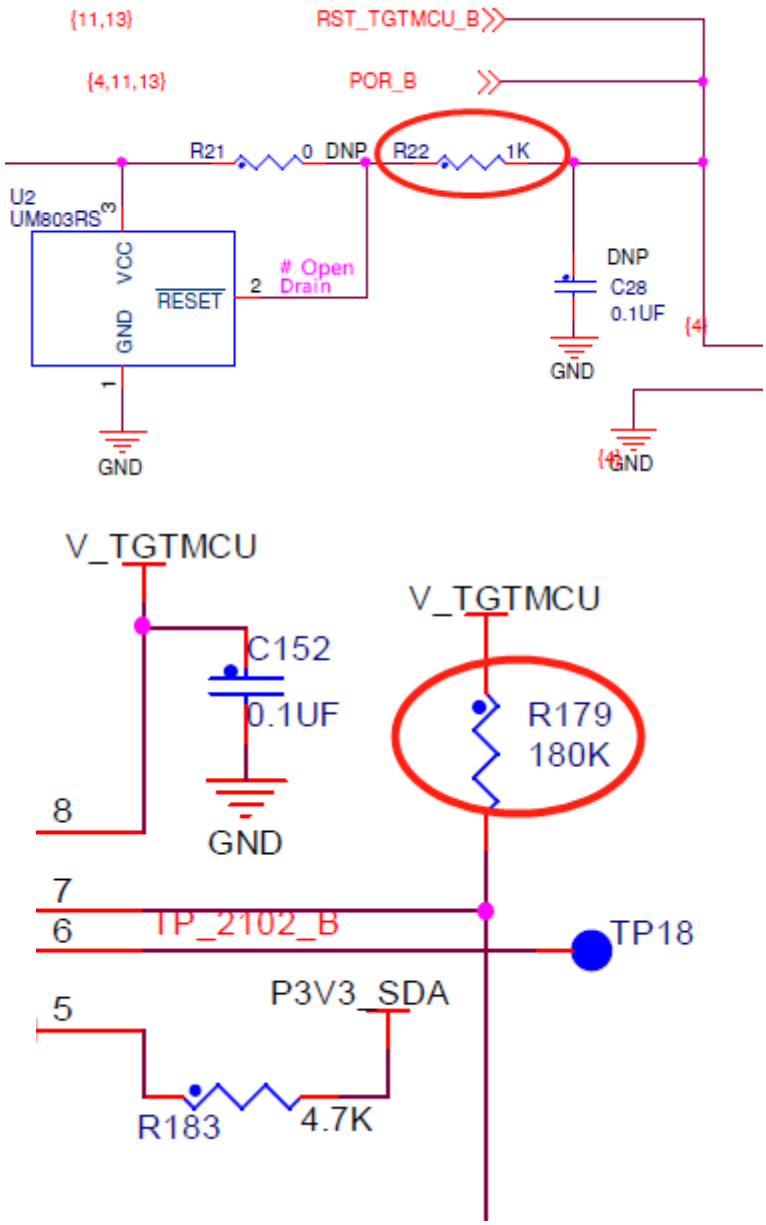

Figure 1. Remove resistors R22 and R179

Next we must measure the current value of DCDC_IN(J37), VDD_HIGH_IN (J5), and VDD_SNVS_IN (J6).

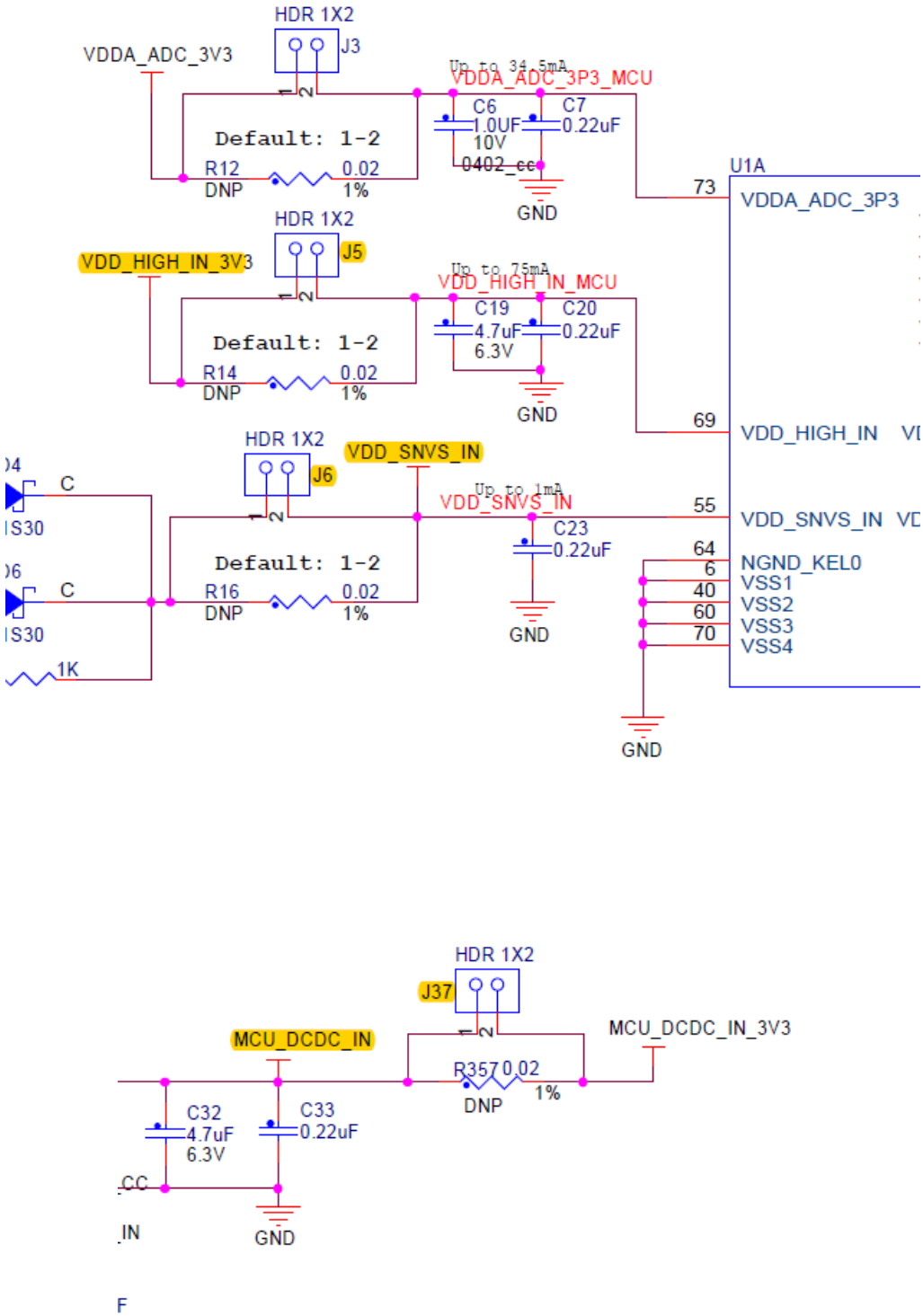

Figure 2. Test Points for DCDC_IN, VDD_HIGH_IN, and VDD_SNVS_IN

5 Power consumption results

The testing code is based on SDK 2.6.1 and the project files is at: boards\evkmimxrt1020\demo_apps\power_mode_switch_bm\iar\power_mode_switch_bm.eww.

CoreMark testing project is based on power_mode_switch_bm.

5.1 Run mode

NOTE

All power consumption values are typical silicon at 25 C.

The power consumption in Table 7 and Table 8 is measured with the default SDK low-power mode switch project.

Table 7. Run mode on RAM

Power Rail	Overdrive (500 MHz)			Full Speed Run (396 MHz)			Low Speed Run (132 MHz)			Low-Power Run (24 MHz)		
	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	3.30	27.855	91.92	3.30	21.26	70.158	3.30	9.63	31.779	3.30	1.745	5.7585
VDD_HIGH_IN	3.30	13.915	45.9195	3.30	13.92	45.936	3.30	5.615	18.5295	3.30	0.34	1.122
VDD_SNVS_IN	3.30	0.0115	0.0379	3.30	0.012	0.0396	3.30	0.007	0.0231	3.30	0.0095	0.03135

Table 8. Run mode XIP on Flash

Power Rail	Overdrive (500 MHz)			Full Speed Run (396 MHz)			Low Speed Run (132 MHz)			Low-Power Run (24 MHz)		
	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	3.30	28.01	92.433	3.30	21.375	70.5375	3.30	9.83	32.439	3.30	1.79	5.907
VDD_HIGH_IN	3.30	13.92	45.936	3.30	13.92	45.936	3.30	5.615	18.5295	3.30	0.34	1.122
VDD_SNVS_IN	3.30	0.0115	0.038	3.30	0.0115	0.038	3.30	0.007	0.0231	3.30	0.009	0.0297

The power consumption in Table 9 and Table 10 is measured with the **CoreMark** which based on low-power mode switch project.

Table 9. CoreMark on RAM

Power Rail	Overdrive (500 MHz)			Full Speed Run (396 MHz)			Low Speed Run (132 MHz)			Low-Power Run (24 MHz)		
	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	3.30	57.096	188.4216	3.30	39.2565	129.5465	3.30	14.6515	48.341	3.30	2.612	8.6196
VDD_HIGH_IN	3.30	13.974	46.1126	3.30	13.9745	46.1159	3.30	5.669	18.7077	3.30	0.399	1.3167
VDD_SNVS_IN	3.30	0.013	0.0429	3.30	0.0115	0.038	3.30	0.0065	0.0215	3.30	0.0095	0.0314

Table 10. CoreMark XIP on Flash

Power Rail	Overdrive (500 MHz)			Full Speed Run (396 MHz)			Low Speed Run (132 MHz)			Low-Power Run (24 MHz)		
	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	3.30	54.3915	179.492	3.30	37.1875	122.7188	3.30	14.583	48.1239	3.30	2.5505	8.4167
VDD_HIGH_IN	3.30	13.9735	46.1126	3.30	13.9745	45.936	3.30	5.6705	18.7127	3.30	0.398	1.3134
VDD_SNVS_IN	3.30	0.0105	0.0347	3.30	0.0125	0.038	3.30	0.006	0.0198	3.30	0.0095	0.0314

5.2 Low-power mode

The power consumption in Table 11and Table 12 is measured with the power mode switch project (The demo project in the attachment).

NOTE

Because discontinuous conduction mode(DCM) can increase the efficiency of DCDC, if low current loading, it is always recommended.

Table 11. Low-power mode on RAM

Power Rail	System Idle			Low Power Idle			Suspend[1]			SNVS[2]		
	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	3.30	4.5	14.85	3.30	1.045	3.4485	3.30	0.168	0.5544	0.00	0.00	0.00
VDD_HIGH_IN	3.30	5.62	18.546	3.30	0.34	1.122	3.30	0.1205	0.3977	0.00	0.00	0.00

Table continues on the next page...

Table 11. Low-power mode on RAM (continued)

Power Rail	System Idle			Low Power Idle			Suspend[1]			SNVS[2]		
	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
VDD_SNVS_IN	3.30	0.007	0.0231	3.30	0.0103	0.0340	3.30	0.0057	0.0188	3.30	0.0163	0.0536

Table 12. Low-power mode XIP on Flash

Power Rail	System Idle			Low Power Idle			Suspend[1]			SNVS[2]		
	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)	Voltage (V)	Current (mA)	Power (mW)
DCDC_IN	3.30	5.225	17.2425	3.30	1.155	3.8115	3.30	0.165	0.5445	0.00	0.00	0.00
VDD_HIGH_IN	3.30	5.61	18.513	3.30	0.335	1.1055	3.30	0.12	0.396	0.00	0.00	0.00
VDD_SNVS_IN	3.30	0.0069	0.0228	3.30	0.0103	0.0338	3.30	0.0054	0.0178	3.30	0.0161	0.0531

NOTE

1. **Suspend:** Suspend mode with RAM data in FlexRAM(bank0).
2. **SNVS:** SNVS mode with RTC working

NOTE

Discontinuous conduction mode (DCM) increases the efficiency of DCDC if low current loading and is always recommended.

To reduce power consumption, VDD_SNVS_IN is powered by VDD_HIGH_IN in all power modes except the SNVS mode.

NOTE

All power consumption values are typical silicon at 25 C

6 Conclusion

This document mainly describes how to measure power consumption on i.MX RT based on MIMXRT1020 EVK (Rev A2). For more design details in designing a low-power application, you can take the application note How to use iMXRT Low Power Feature for reference.

7 Reference

- i.MX RT 1020 reference manual
- Arm Cortex M7 reference manual

8 Revision history

Table 13. Revision history

Revision number	Date	Substantive changes
0	05/2018	Initial release
1	02/2020	Updated the power results based on Flash and RAM.

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Date of release: 11 February 2020

Document identifier: AN12204