NXP Semiconductors
Application Note

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Migration Guide from i.MX RT1060 to i.MX RT1064

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1. Introduction

The i.MX RT1064 processor contains 4 MB on-chip flash and 1 MB on-chip RAM. Different from the i.MX RT1060, i.MX RT1064 is embedded with one 4 MB QSPI flash, which helps customers to save the space and simply circuit design.

This document intends to introduce how to migrate from the i.MX RT1060 to i.MX RT1064.

2. Overview

The i.MX RT1064 combines the i.MXRT1060 and one 4 MB QSPI flash in chip. During the migration, be aware of the following items:

- The i.MX RT1064 chip can directly replace the i.MXRT1060 chip and no hardware upgrade is required.
- The i.MX RT1064 can boot by the internal QSPI flash while the i.MXRT1060 can boot by external flash.
- The modification on the linker file is required.

The i.MX RT1060 and i.MX RT1064 take different XIP boot options, which means they boot by different FlexSPI instances. The i.MX RT1060 uses FlexSPI and i.MXRT1064 uses FlexSPI2. Please see following tables for the differences on boot pins, memory map and pin mux.

Table 1 and *Table 2* describe the XIP boot pins for i.MXRT1060 and i.MXRT1064.

Table 1. i.MXRT1060 XIP boot options

Peripheral	Port (IO function)	PAD	Description
FlexSPI	FLEXSPI_B_DATA3	GPIO_SD_B1_00	Boot option to connect the external XIP flash, such as, QSPI flash, Octal flash and Hyper flash, and so on.
	FLEXSPI_B_DATA2	GPIO_SD_B1_01	
	FLEXSPI_B_DATA1	GPIO_SD_B1_02	
	FLEXSPI_B_DATA0	GPIO_SD_B1_03	
	FLEXSPI_B_SCLK	GPIO_SD_B1_04	
	FLEXSPI_B_DQS	GPIO_SD_B0_05	
	FLEXSPI_B_SS0_B	GPIO_SD_B0_04	
	FLEXSPI_B_SS1_B	GPIO_SD_B0_01	
	FLEXSPI_A_DQS	GPIO_SD_B1_05	
	FLEXSPI_A_SS0_B	GPIO_SD_B1_06	
	FLEXSPI_A_SS1_B	GPIO_SD_B0_00	
	FLEXSPI_A_SCLK	GPIO_SD_B1_07	
	FLEXSPI_A_DATA0	GPIO_SD_B1_08	
	FLEXSPI_A_DATA1	GPIO_SD_B1_09	
	FLEXSPI_A_DATA2	GPIO_SD_B1_10	
	FLEXSPI_A_DATA3	GPIO_SD_B1_11	
FlexSPI	FLEXSPI_A_DQS	GPIO_AD_B1_09	The other boot option, just available to connect QSPI flash.
	FLEXSPI_A_DATA3	GPIO_AD_B1_10	
	FLEXSPI_A_DATA2	GPIO_AD_B1_11	
	FLEXSPI_A_DATA1	GPIO_AD_B1_12	
	FLEXSPI_A_DATA0	GPIO_AD_B1_13	
	FLEXSPI_A_SCLK	GPIO_AD_B1_14	
	FLEXSPI_A_SS0_B	GPIO_AD_B1_15	

Table 2. i.MXRT1064 XIP boot options

Peripheral	Port (IO function)	PAD	Description
FlexSPI2	FLEXSPI2_A_ SS0_B	GPIO_SPI_B1_06	Connected to the embedded QSPI flash for booting.
	FLEXSPI2_A_ SCLK	GPIO_SPI_B0_08	
	FLEXSPI2_A_ DQS	GPIO_SPI_B0_09	
	FLEXSPI2_A_DATA0	GPIO_SPI_B0_02	
	FLEXSPI2_A_DATA1	GPIO_SPI_B1_03	
	FLEXSPI2_A_DATA2	GPIO_SPI_B1_02	
	FLEXSPI2_A_DATA3	GPIO_SPI_B0_10	
	FLEXSPI2_RESET_PIN	GPIO_SPI_B0_13	

Table 3 shows the memory map differences between FlexSPI and FlexSPI2.

Table 3. FlexSPI/FlexSPI2 memory map

Start address	End address	Size	Description
7000_0000	7EFF_FFFF	240 MB	FlexSPI2/FlexSPI2 ciphertext
6000_0000	6FFF_FFFF	256 MB	FlexSPI/FlexSPI ciphertext

During the migration from the i.MX RT1060 to i.MX RT1064, there are pin mux changes, as shown in *Table 4*.

Table 4. Pin mux changes

Peripheral	Function	Pin muxing	
		i.MX RT1060	i.MX RT1064
FlexSPI2	FLEXSPI2_A_DATA0	GPIO_EMC_26	GPIO_SPI_B0_02
		GPIO_SPI_B1_04	
		GPIO_SPI_B0_02	
	FLEXSPI2_A_DATA1	GPIO_SPI_B0_12	GPIO_SPI_B1_03
		GPIO_SPI_B1_03	
		GPIO_EMC_27	
	FLEXSPI2_A_DATA2	GPIO_SPI_B0_06	GPIO_SPI_B1_02
		GPIO_SPI_B1_02	
		GPIO_EMC_28	
	FLEXSPI2_A_DATA3	GPIO_SPI_B0_10	GPIO_SPI_B0_10
		GPIO_SPI_B1_01	
		GPIO_EMC_29	
	FLEXSPI2_A_DQS	GPIO_SPI_B0_09	GPIO_SPI_B0_09
		GPIO_SPI_B1_00	
		GPIO_EMC_23	
	FLEXSPI2_A_SCLK	GPIO_SPI_B0_08	GPIO_SPI_B0_08
		GPIO_SPI_B1_05	
		GPIO_EMC_25	
	FLEXSPI2_A_SS0_B	GPIO_SPI_B0_05	GPIO_SPI_B1_06
		GPIO_SPI_B1_06	
		GPIO_EMC_24	

Table 4. Pin mux changes

Peripheral	Function	Pin muxing	
		i.MX RT1060	i.MX RT1064
	FLEXSPI2_A_SS1_B	GPIO_EMC_22	N/A
	FLEXSPI2_B_DATA0	GPIO_SPI_B0_11	N/A
		GPIO_EMC_13	N/A
	FLEXSPI2_B_DATA1	GPIO_SPI_B0_07	N/A
		GPIO_EMC_14	N/A
	FLEXSPI2_B_DATA2	GPIO_SPI_B0_03	N/A
		GPIO_EMC_15	N/A
	FLEXSPI2_B_DATA3	GPIO_SPI_B0_04	N/A
		GPIO_EMC_16	N/A
	FLEXSPI2_B_DQS	GPIO_EMC_11	N/A
	FLEXSPI2_B_SCLK	GPIO_SPI_B0_01	N/A
		GPIO_EMC_12	N/A
	FLEXSPI2_B_SS0_B	GPIO_EMC_10	N/A
	FLEXSPI2_B_SS1_B	GPIO_EMC_09	N/A

3. How to migrate

As the i.MX RT1064 XIP boots through the FlexSPI2 interface, modifications are required on the linker file.

3.1. Linker file modification

As mentioned above, there are changes on the memory map during the migration from the i.MX RT1060 to i.MX RT1064.

As shown in *Figure 1* and *Figure 2*, you need to update the base address of text space from `0x60000000` to `0x70000000` during the code migration from the i.MX RT1060 to i.MX RT1064.

```
define symbol m_interrupts_start       = 0x60002000;
define symbol m_interrupts_end         = 0x600023FF;

define symbol m_text_start             = 0x60002400;
define symbol m_text_end               = 0x607FFFFF;

define symbol m_data_start             = 0x20000000;
define symbol m_data_end               = 0x2001FFFF;

define symbol m_data2_start            = 0x20200000;
define symbol m_data2_end              = 0x202BFFFF;

define exported symbol m_boot_hdr_conf_start = 0x60000000;
define symbol m_boot_hdr_ivt_start           = 0x60001000;
define symbol m_boot_hdr_boot_data_start     = 0x60001020;
define symbol m_boot_hdr_dcd_data_start      = 0x60001030;
```

Figure 1. Linker file in i.MXRT1060

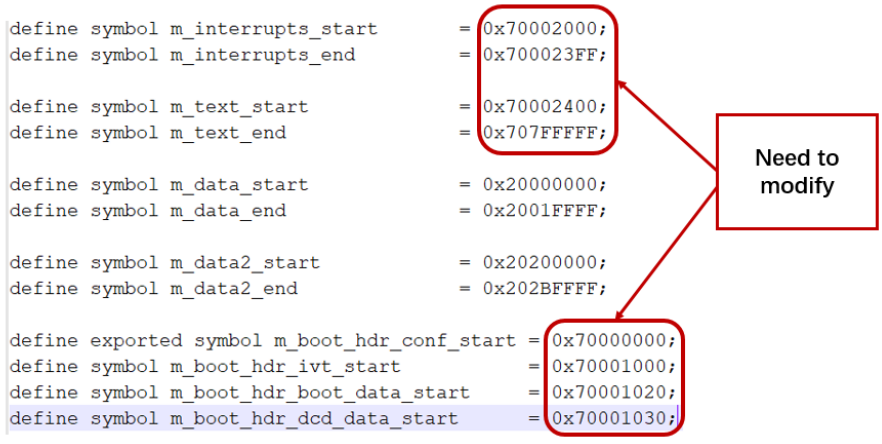

Figure 2. Linker file in i.MXRT1064

3.2. XIP flash boot option

Do not try the XIP boot by FlexSPI with external XIP flash, but you can still connect the external flash through the FlexSPI interface, which can be used to save data or other functions except boot.

3.3. FlexSPI2 pin mux changes

i.MX RT1060 can remap the FlexSPI2 to external pins (SEMC port) and internal pad, while i.MX RT1064 can only remap to the internal pad (SPI port).

NOTE

DO NOT remap the FlexSPI2 to other pins except the embedded flash connection when migrating from i.MX RT1060 to i.MX RT1064. Otherwise, the embedded QSPI flash malfunctions.

4. Conclusion

This document introduces how to migrate from the i.MXRT1060 to the i.MXRT1064, which helps customers to move the project to i.MXRT1064 easily.

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