AN12442

Theoretical Set Up Checks for Future MPC5510 Family XOSC Use

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by: NXP Semiconductors

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1 Introduction

Initially the NXP team must state that as we do not know the final use case and hence what the customer will see as the most critical parameter (eg. Idd, start up time, reliability, noise immunity, etc. etc.). The set up is not easy to optimize for all parameters at the same time. We do not supply or recommend crystals so it is impossible to put any type of “limits or controls” in this application note.

Traditionally the oscillator set up has been performed by crystal vendors and/or the customer having access to all system requirements having the ability to characterize the entire circuit.

The following is therefore general recommendations for consideration in future optimizations, if the NXP team was to be invited to participate in characterization of an oscillator circuit using a similar Micro and crystal we would advise the following :

1. Theoretical calculation of C0, C_load, gm, and mW drive level of the oscillator (using data sheet values of Micro, PCB design, Capacitor Specifications, and Oscillator Data Sheet).

   Example:

   f = 8 MHz

   C1,C2 = 16 pF (starting point 8.2 pF capacitors plus, pin capacity, PCB stray capacity, etc)

   C0 = 4 pF

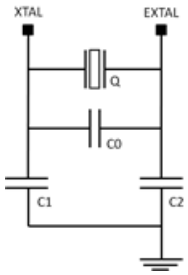

Figure 1. Pierce Oscillator including C0

C0 represents shunt capacitance . It is the sum of capacitance due to the electrodes on the crystal plate plus stray capacitances due to the crystal holder and enclosure. Also the microcontroller pin capacitance and the PCB add to this capacitance.

Values of C0 typically range from 3 to 10 pF.

C1 and C2 used for calculations below should be the sum of the capacitors used + stray pcb capacitance + stray capacitance from the microcontroller. Commonly the starting point for this will equal the recommended Cload value of the crystal. Note, two capacitors in series reduces the affective capacitance in ½ so if the recommended Cload for the crystal is 8 pF then you want C1=C2=16 pF as your theoretical starting point.

2 Oscillator GM

the following equation is used to calcuate Oscillator GM:

$gm_{opt\ osc}$ = 2 x π x f x(C1 + C2 + (C1xC2/C0))

$gm_{opt\ osc}$ = 4.82 mA/V

gm_{mcu} = ~16 mA/V

Center gm to expected gm_optimum (by using R_damp), center C_load to expected values (2x crystal manufacturer C_load – Cs – C_pcb) then test NRM and average startup time at theoretical centers.

3 Requirement

The following requirements needs to be fullfilled:

$gm_{opt\ osc} \approx gm_{mcu}$

In the example:

4.82 mA/V ≠ ~16 mA/V

$gm_{opt\ osc} \neq gm_{mcu}$

- Adapt oscillator gm

  $R_{out\ MPC551xx}$ = 2.2 kΩ

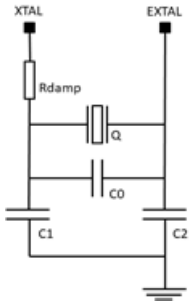

Figure 2. Pierce Oscillator including Rdamp

  $gm_{mcu'} = gm_{mcu}$ x 1/1 + Rdamp/Rout

  With Rdamp = 5 kΩ

  $gm_{mcu'}$ = ~4.9 mA/V

  $gm_{opt\ osc} = gm_{mcu'}$

  4.82 mA/V ~ 4.9 mA/V

- Another method to match gm could be to adapt C1 and C2, or use a different crystal. Note, changing C1 and C2 from crystal manufactures recommended value can affect drive level, startup time EMI performance, and ppm frequency accuracy.

Example: C1, C2 = 22pF (giving a total of ~ 30pF)(22 pF capacitors plus, pin capacity, PCB stray capacity, etc)

$gm_{opt\ osc}$ = 2 x π x f x (C1 + C2 + (C1 x C2/C0))

$gm_{opt\ osc}$ = ~14.32 mA/V

$gm_{opt\ osc} \sim gm_{mcu}$

Typical calculation and testing should now meet typical crystal manufactures NRM requirements.Further testing to insure your design has good margin. All of these tests are to confirm that your theoretical calculations are correct and centered on your expected results.

If you see an increase or decrease in the measured data that you did not suspect (or any sudden large shift in the data) then that is a sign that something in the calculations may not be correct. A properly designed oscillator will be centered on the data and calculations. If the NRM and startup time data just keeps increasing in one direction as you move up and down from optimum gm

and you do not see any drop then that is a sign you are not centered (or you need to push it further each way to confirm you are centered).

1. Test crystal frequency over C-loads above calculated ideal and below calculated ideal and confirm lowest ppm deviation matches targeted C_load. Measure crystal frequency over C-loads with minimum and maximum C-load (use Capacitor specification).Test a few parts with 2x more capacitor margin (up and down) to verify functionality.
    - If gm minimum and maximum gm parts are available, Using minimum gm part with maximum Cload and the maximum gm part with minimum Cload from the above desired configuration measure NRM (Negative Resistance Margin) and average startup time of the crystal in the circuit.
2. Test C0 corner, add C0 (by adding a capacitor across the crystal) to get C0 to slightly above maximum expected value and use minimum Cload values then measure NRM (Negative Resistance Margin) and average startup time.
    - If gm minimum and maximum gm parts are available, Using maximum gm part with minimum Cload and minimum gm part with the maximum Cload (and still have the additional C0), measure NRM (Negative Resistance Margin) and average startup time of the crystal in the circuit.
3. Measure peak to peak amplitude across crystal and ensure it is less than mW rating of the crystal. Observe waveforms; look for distortion especially with the XTAL pin. Notice start up of the wave form if it has very high amplitude before dropping to controlled level (waveform above and below Vddpll and Vsspll). These are signs point to a marginal design.
4. Test noise immunity of circuit.
5. The team would then repeat the standard configuration with 2x maximum crystal ESR at minimum and maximum capacitance expected with regards to temperature, minimum Voltage and maximum Voltage. Verify start-up and function under these conditions.

4 Conclusion

From the results above further testing may be recommended, or if the system had some special requirements those would be tested.Note all NRM tests done with non-standard configuration may not meet the crystal manufactures recommended margin, this is normally ok since the NRM margin is to accommodate for those variations that you are manually applying to the circuit. The data is mainly to insure you are centered and as an additional indicator to how much margin you will have if any of those adjusted parameters shift.

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