AN13022
LX2160A SerDes 1 Lane Reconfiguration from 11 to 31

Rev. 0 — 10/2020

1 Introduction

The device reference manual provides a list of all supported SerDes protocols. Only SerDes options that have been validated on silicon are documented in the reference manual. Custom SerDes configuration may be supported by reconfiguring the lanes for the desired settings if validated and approved by NXP. Any changes to configuration of default SerDes options require software reconfiguration.

This document describes the sequence to reconfigure SerDes lanes from SGMII to USXGMII/XFI and two PCIe x2 lanes at Gen 1 or Gen 2 speeds for the LX2160A device. Subsequent reconfiguration from SFI/XFI to 10GBase-KR or USXGMII shall follow the sequence described in the LX2160A Reference Manual.

2 SerDes configuration requirements

This document describes a use case requirement of four lanes of USXGMII/XFI and two PCIe x2 lanes at Gen 1 or Gen 2 speeds, shown as SerDes 1 protocol number 31 in Table 1. Protocol 31 is not one of the default SerDes options for the LX2160A, therefore, it is not documented in the LX2160A Reference Manual. However, standard MC firmware versions 10.24.1 and later add support for protocol 31.

This document describes the sequence that results in the target configuration which can be summarized as:

1. Start with SerDes protocol 11, which supports four lanes of SGMII on lanes F, E, B, and A, and two PCIe x2 lanes at Gen 3 speed on lanes H, G, D, and C.

2. Reconfigure the SGMII lanes to USXGMII/XFI and limit the PCIe lanes to Gen 2 speed.

3. Change the PLL assignment for USXGMII/XFI to PLLS since 10G Ethernet only runs on PLLS.

4. Change the PLL assignment for PCIe to PLLF since it runs on 5 GHz VCO frequency so it cannot run on the same PLL as USXGMII/XFI.

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Table 1. SerDes 1 reconfiguration

SRDS_PRTCL_S1 (decimal)	Lane								PLL mapping	PLL mapping after Gen3 speed switch
	H/0	G/1	F/2	E/3	D/4	C/5	B/6	A/7		
11 (starting)	PCIe.1 x2		SGMII.5	SGMII.6	PCIe.2 x2		SGMII.9	SGMII.10	SSSSSSSS	FFSSFFSS
31 (target)	PCIe.1 x2 (Gen 1, 2)		USXGMII/XFI.5	USXGMII/XFI.6	PCIe.2 x2 (Gen 1, 2)		USXGMII/XFI.9	USXGMII/XFI.10	FFSSFFSS	N/A

The reconfiguration sequence assumes the following starting RCW settings:

- SRDS_PRTCL_S1 = 5'b01011 to select protocol 11.

- SRDS_DIV_PEX_S1 = 2'b10 to configure PCIe to train up to a max rate of 5G (Gen 2).

- SRDS_PLL_REF_CLK_SEL_S1 = 2'b*mn*, where *m* selects the reference clock for the PCIe lanes on PLLS and *n* selects the reference clock for USXGMII/XFI lanes on PLLF. Example:

    — *m* = 0 for 100 MHz PCIe reference clock

    — *n* = 1 for 161.1328125 MHz USXGMII/XFI reference clock

- SRDS_PLL_PD_PLL1 = 0 and SRDS_PLL_PD_PLL2 = 0 so both PLLF and PLLS are powered up.

- SRDS_REFCLKF_DIS_S1 = 0 to keep SD1_PLLF_REF_CLK enabled.

- SRDS_INTRA_REF_CLK_S1 = 0 intra reference clock is not used.

3 Software sequence

The reconfiguration sequence must be implemented in PBI and is shown below.

1. Disable SGMII for lanes A, B, E, and F.

    - SD1: PCC8 (offset 0x10A0) = 0x0000_0000

        — SGMIIA_CFG = 0 disable SGMIIa

        — SGMIIB_CFG = 0 disable SGMIIb

        — SGMIIE_CFG = 0 disable SGMIIe

        — SGMIIF_CFG = 0 disable SGMIIf

2. Enable XFI mode for lanes A, B, E, and F

    - SD1: PCCC (offset 0x10B0) = 0x9900_9900

        — SXGMIIA_XFI = 1 PCS operates in XFI/SFI mode

        — SXGMIIA_CFG = 001b enable SXGMIIa

        — SXGMIIB_XFI = 1 PCS operates in XFI/SFI mode

        — SXGMIIB_CFG = 001b enable SXGMIIb

        — SXGMIIE_XFI = 1 PCS operates in XFI/SFI mode

        — SXGMIIE_CFG = 001b enable SXGMIIe

        — SXGMIIF_XFI = 1 PCS operates in XFI/SFI mode

        — SXGMIIF_CFG = 001b enable SXGMIIf

3. Assume 100 MHz reference clock for PLLF for the PCIe lanes

    - SD1: PLLFCR0 (offset 0x0404) = 0x0000_0000

        — REFCLK_SEL = 00000b for 100 MHz

4. Configure 5G clock net frequency for PLLF

    - SD1: PLLFCR1 (offset 0x0408) = 0x9030_0008

        — SLOW_VCO_EN = 1 to enable the slower VCO

        — FRATE_SEL = 10000b for PCIe on PLLF

        — HI_BW_SEL = 1 to select higher PLL bandwidth

        — CLKD_RCAL_SLW_EN = 1 to enable resistor calibration for clock driver

        — RTMR_BYP = 1 to bypass retimer to clock driver and SSC phase interpolator

        — EX_DLY_SEL = 00b

5. Set the recommended PLLF settings for PCIe 5G

- SD1: PLLFCR3 (offset 0x0410) = 0x0000_3000

  — SSC_SEL = 00b no PLL modulation

  — SSC_SLP_OFF = 0000000000b for no slope offset

  — Bit 13 = 1

  — Bit 12 = 1

6. Set the recommended PLLF settings for PCIe 5G

- SD1: PLLFCR4 (offset 0x0414) = 0x0000_0000

  — SSC_BIAS_BST = 000b SSC bias boost

  — SSC_SAW_MIN = 0000000000b SSC minimum sawtooth frequency offset

  — SSC_PI_BST = 00000b SSC phase interpolator Iqdiv2 boost

  — SSC_SAW_MAX = 0000000000b SSC maximum sawtooth frequency offset

7. Assume 161.1328125 MHz reference clock for PLLS for 10GE operation

- SD1: PLLSCR0 (offset 0x0504) = 0x0004_0000

  — REFCLK_SEL = 00100b for 161.1328125 MHz

8. Configure 10.3125G clock net frequency for PLLS

- SD1: PLLSCR1 (offset 0x0508) = 0x8610_0008

  — SLOW_VCO_EN = 1 to enable the slower VCO

  — FRATE_SEL = 00110b for XFI/SFI on PLLS

  — HI_BW_SEL = 0 to do not select higher PLL bandwidth

  — CLKD_RCAL_SLW_EN = 1 to enable resistor calibration for clock driver

  — RTMR_BYP = 1 to bypass retimer to clock driver and SSC phase interpolator

  — EX_DLY_SEL = 00b

9. Set the recommended PLLS settings for XFI

- SD1: PLLSCR3 (offset 0x0510) = 0x0000_3000

  — SSC_SEL = 00b no PLL modulation

  — SSC_SLP_OFF = 0000000000b for no slope offset

  — Bit 13 = 1

  — Bit 12 = 1

10. Set the recommended PLLS settings for XFI

- SD1: PLLSCR4 (offset 0x0514) = 0x0000_1000

  — SSC_BIAS_BST = 000b SSC bias boost

  — SSC_SAW_MIN = 0000000000b SSC minimum sawtooth frequency offset

  — SSC_PI_BST = 00010b SSC phase interpolator Iqdiv2 boost

  — SSC_SAW_MAX = 0000000000b SSC maximum sawtooth frequency offset

11. Change the PLL assignment for PCIe on the transmitter for lanes C, D, G, H from PLLS to PLLF

- SD1: LNmTGCR0 (offsets 0x0A24 for lane C, 0x0B24 for lane D, 0x0E24 for lane G, 0x0F24 for lane H) = 0x0100_0200

— USE_SLOW_PLL = 0 transmit uses PLLF

— BY_N_RATE_SEL = 001b PCIe is half rate

— CM_DLY_MATCH = 1 changes in LNmTRSTCTL[OUT_CM] are delay matched to changes in transmit data

12. Change the PLL assignment for PCIe on the receiver for lanes C, D, G, H from PLLS to PLLF

   • SD1: LNmRGCR0 (offsets 0x0A44 for lane C, 0x0B44 for lane D, 0x0E44 for lane G, 0x0F44 for lane H) = 0x0100_0001

   — USE_SLOW_PLL = 0 receive uses PLLF

   — BY_N_RATE_SEL = 001b PCIe is half rate

   — PTRM_VCM_SEL = 01b Common mode is HiZ if PLLnRST[EN] or LNmRRSTCTL[EN] is negated.

13. Change the protocol for lanes A, B, E, F from SGMII to XFI

   • SD1: LNmGCR0 (offsets 0x0800 for lane A, 0x0900 for lane B, 0x0C00 for lane E, 0x0D00 for lane F) = 0x0000_0052

   — Bit 28 = 0 Must be 0 for all protocols

   — PORT_LN0_B = 0 Single-lane protocol

   — PROTO_SEL = 01010b for XFI

   — IF_WIDTH = 010b 20-bit interface width

14. Set the PLL assignment for XFI on the transmitter for lanes A, B, E, F to PLLS

   • SD1: LNmTGCR0 (offsets 0x0824 for lane A, 0x0924 for lane B, 0x0C24 for lane E, 0x0D24 for lane F) = 0x1000_0000

   — USE_SLOW_PLL = 1 transmit uses PLLS

   — BY_N_RATE_SEL = 000b 10G is full rate

   — CM_DLY_MATCH = 0 changes in LNmTRSTCTL[OUT_CM] are not delay matched to changes in transmit data

15. Configure the transmit equalization for lanes A, B, E, F for XFI

   • SD1: LNmTECR0 (offsets 0x0830 for lane A, 0x0930 for lane B, 0x0C30 for lane E, 0x0D30 for lane F) = 0x1080_8307

   — EQ_TYPE = 001b for 2-tap equalization

   — EQ_SGN_PREQ = 1 for positive sign for pre-cursor

   — EQ_PREQ = 0000b for 1.0x drive strength of transmit full swing transition bit to pre-cursor

   — EQ_SGN_POST1Q = 1 for positive sign for first post-cursor

   — EQ_POST1Q = 00011b for 1.14x drive strength of transmit full swing transition bit to first post-cursor

   — EQ_AMP_RED = 000111b for 0.585x overall amplitude reduction

16. Set the PLL assignment for XFI on the receiver for lanes A, B, E, F to PLLS

   • SD1: LNmRGCR0 (offsets 0x0844 for lane A, 0x0944 for lane B, 0x0C44 for lane E, 0x0D44 for lane F) = 0x1000_0000

   — USE_SLOW_PLL = 1 receive uses PLLS

   — BY_N_RATE_SEL = 000b 10G is full rate

   — PTRM_VCM_SEL = 00b Common mode impedance is always calibrated to SD_GND

17. Set the recommended XFI settings for lanes A, B, E, F

- SD1: LNmRGCR1 (offsets 0x0848 for lane A, 0x0948 for lane B, 0x0C48 for lane E, 0x0D48 for lane F) = 0x1000_0000

  — RX_ORD_ELECIDLE = 0 Do not put into ordered idle state

  — Bit 28 = 1

  — ENTER_IDLE_FLT_SEL = 00b Bypass unexpected entrance into idle

  — EXIT_IDLE_FLT_SEL = 000b Force immediate exit from idle state AFTER order idle released and min time in idle

  — DATA_LOST_TH_SEL = 000b Disable loss of signal detection

18. Disable receive equalization gain overrides for lanes A, B, E, F

    - SD1: LNmRECR0 (offsets 0x0850 for lane A, 0x0950 for lane B, 0x0C50 for lane E, 0x0D50 for lane F) = 0x0000_0000

19. Set the recommended the receive equalization for XFI for lanes A, B, E, F

    - SD1: LNmRECR2 (offsets 0x0858 for lane A, 0x0958 for lane B, 0x0C58 for lane E, 0x0D58 for lane F) = 0x8100_0020

      — Bit 31 = 1

      — EQ_BLW_SEL = 01b baseline wander for 10G

      — Bits 5:4 = 10b

The PBI sequence is shown below:

```
.pbi
write 0x01EA10A0,0x00000000
write 0x01EA10B0,0x99009900

write 0x01EA0404,0x00000000
write 0x01EA0408,0x90300008
write 0x01EA0410,0x00003000
write 0x01EA0414,0x00000000

write 0x01EA0504,0x00040000
write 0x01EA0508,0x86100008
write 0x01EA0510,0x00003000
write 0x01EA0514,0x00001000

write 0x01EA0A24,0x01000200
write 0x01EA0A44,0x01000001
write 0x01EA0B24,0x01000200
write 0x01EA0B44,0x01000001

write 0x01EA0E24,0x01000200
write 0x01EA0E44,0x01000001
write 0x01EA0F24,0x01000200
write 0x01EA0F44,0x01000001

write 0x01EA0800,0x00000052
write 0x01EA0900,0x00000052
write 0x01EA0C00,0x00000052
write 0x01EA0D00,0x00000052

write 0x01EA0824,0x10000000
write 0x01EA0924,0x10000000
write 0x01EA0C24,0x10000000
```

```
write 0x01EA0D24,0x10000000

write 0x01EA0830,0x10808307
write 0x01EA0930,0x10808307
write 0x01EA0C30,0x10808307
write 0x01EA0D30,0x10808307

write 0x01EA0844,0x10000000
write 0x01EA0944,0x10000000
write 0x01EA0C44,0x10000000
write 0x01EA0D44,0x10000000

write 0x01EA0848,0x10000000
write 0x01EA0948,0x10000000
write 0x01EA0C48,0x10000000
write 0x01EA0D48,0x10000000

write 0x01EA0850,0x00000000
write 0x01EA0950,0x00000000
write 0x01EA0C50,0x00000000
write 0x01EA0D50,0x00000000

write 0x01EA0858,0x81000020
write 0x01EA0958,0x81000020
write 0x01EA0C58,0x81000020
write 0x01EA0D58,0x81000020
.end
```

4 RCWSR29 override

The Reset Configuration Word Status Registers (RCWSR1:RCWSR32) are written with the RCW information that are read from flash memory by the device at power-on-reset. The RCWSR register values are read-only after exiting reset.

Software (U-boot) reads the selected SerDes protocol from RCWSR29. It looks at the SerDes configuration table to find the entry for protocol 31 and its corresponding interfaces. In order for software (U-boot) to read the updated SerDes 1 protocol value of 31, the following steps must be performed:

1. Add an entry for SerDes 1 protocol 31 in the SerDes configuration table in U-boot

2. Override the RCWSR29 with the updated SerDes 1 protocol value of 31

   • Write to address 0x7_00100170 the new protocol SRDS_PRTCL_S1 = 31.

   • The SerDes 2 and SerDes 3 configuration fields should remain unchanged.

   • Note: The RCWSR29 cannot be updated from the PBI phase. The update must be done in the initial stages of the the board-specific U-boot code so that the correct SerDes protocol is read as U-boot continues execution.

Table 2. Address 0x7_00100170

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SRDS_ REFCL KF_DIS _S1	SRDS_PRTCL_S3					SRDS_PRTCL_S2					SRDS_PRTCL_S1				
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table continues on the next page...

Table 2. Address 0x7_00100170 (continued)

Reserved	SRDS_PLL_PD_PLL6	SRDS_PLL_PD_PLL5	SRDS_PLL_PD_PLL4	SRDS_PLL_PD_PLL3	SRDS_PLL_PD_PLL2	SRDS_PLL_PD_PLL1

NOTE

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5 Revision history

The table below summarizes the revisions to this document.

Table 3. Revision history

Revision	Date	Topic cross-reference	Description
Rev 0	10/2020	-	Initial release.