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Self-test procedure for FXLS896xAF and FXLS897xCF accelerometer family

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Document information

Information	Content
Keywords	FXLS8964AF, FXLS8967AF, FXLS8968AF, FXLS8974CF, FXLS8971CF, FXLS8961AF, 3-axis accelerometer, accelerometer self-test, SDCD validation
Abstract	This document describes the needed information to deploy a self-test routine for the FXLS896xAF and FXLS897xCF accelerometer family. This document also discusses an optional procedure to validate the embedded Sensor Data Change Detection (SDCD) function using self-test.

Table 1. Revision history

Rev	Date	Description
3	20230310	• Added "accelerometer family" to the title of the document. • Updated the keywords and abstract on the first page. • Section 1, revised the second paragraph. • Section 4, revised the second paragraph. • Section 8, revised the paragraph.
2.1	20211130	• Section 9.1, Table 27, revised "178" to "–178" in the "Min" column for "±16 *g* mode, Z axis".
2	20211019	• Section 4, revised "minimize" to "avoid" in the first sentence of the fifth paragraph. • Section 5, revised "If STOC > 'W' LSB, the device passed self-test. The value of 'W' is based on..." to "If LSL (Lower Spec Limit in LSB) ≤ STOC ≤ USL (Upper Spec Limit in LSB), the device passed self-test. The LSL and USL values are based on..." in the paragraph below the equation. • Section 6.3, revised as follows: – Step 6a: revised "If STOC > 'W' LSB, the device passed self-test. The value of 'W' is based on..." to "If LSL (Lower Spec Limit in LSB) ≤ STOC ≤ USL (Upper Spec Limit in LSB), the device passed self-test. LSL and USL values are based on...." – Step 6b: Added "Let W = min(abs(LSL), abs(USL))". – Moved the table titled "Self-test output change limits" to Section 9.1 and revised the table to reflect STOC values found in the product data sheet. • Section 6.4, revised as follows: – Step 8a: revised "If STOC > 'W' LSB, the device passed self-test. The value of 'W' is based on..." to "If LSL (Lower Spec Limit in LSB) <= STOC <= USL (Upper Spec Limit in LSB), the device passed self-test. LSL and USL values are based on…." – Step 8b: Added "Let W = min(abs(LSL), abs(USL))". • Section 7, added new section. • Section 9.1, revised as follows: – Revised "FXLS8962AF" to "FXLS8964AF" in the first paragraph. – Removed table titled "Self-test measurement results for DUT1". – Removed table titled "Self-test measurement results for DUT2". – Table 26, revised the table title, removed the last column titled "Data (*g*)" and revised the values in the table. – Revised the note "For all axes and for ST_POL = 0, the output data is positive only when compared to the self-test offset. The opposite holds true for the ST_POL = 1 case." to "Refer to the FXLS8964AF data sheet for valid self-test limits." • Section 9.2, revised as follows: – First paragraph: revised "reference output plots for FXLS8962AF..." to "example output X, Y, Z plots for FXLS8964AF...." – Removed the figure titled "Self-test response for X-axis". – Second and Third paragraphs: performed minor grammatical corrections. – Removed the figure titled "Self-test response for Y-axis". – Figure 6: revised the image. • Section 9.3, revised as follows: – Revised "FXLS8962AF" to "FXLS8964AF" in the second paragraph. – Table 28, revised the table values. – Revised the values in Step 2, Calculate Self-test Offset and Self-test output change. – Revised the values in Step 3, Set SDCD thresholds.
1	20210514	Initial release

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1 Introduction

The accelerometer self-test feature generates an artificial acceleration signal by deflecting the MEMS transducer proof mass with an electrostatic force. As a consequence, an artificially induced acceleration is measured at the device output indicating proper operation of both MEMS transducer and ASIC signal chain.

The main objective of this document is to provide the user with details on how to deploy a self-test routine for the FXLS896xAF and FXLS897xCF accelerometer family. Such a procedure can be readily implemented in the host MCU handling the sensor and executed when appropriate. An appropriate execution time might be at system power-up prior to sensor initialization.

2 Applicable devices

This document applies to FXLS896xAF and FXLS897xCF devices with PROD_REV register value equal to 13h or 14h.

The PROD_REV register contains the revision number, stored in BCD format, as MAJ.MIN with a range from 1.0 to 9.9. Refer to the respective device data sheet for more details on the PROD_REV product revision register.

3 Accelerometer and self-test principle

The FXLS896xAF/FXLS897xCF 3-axis inertial sensors measure acceleration through its inertial proof mass inside the MEMS transducer. When the device undergoes acceleration, the movement of the proof mass equates to a slight change in capacitance that is translated into a voltage and digitized inside the sensor mixed-signal chain.

In order to check the operation of the sensor (transducer and signal chain) without any applied acceleration, a self-test function is executed. The self-test function applies a voltage to the MEMS transducer electrodes, creating an electrostatic force that deflects the proof mass and causes an output response similar to a response seen during acceleration. The application of the self-test electrostatic force can be viewed as a step input, with the inertial proof mass following a first order response curve and settling to a final value after a finite amount of time (settling time).

The self-test procedure is performed in two steps for each axis. The two-step process moves the proof mass in a positive, then negative direction, which allows higher sensitivity and removes any constant acceleration or sensor offsets.

The device is not required to be at rest during the test sequence and may also be arbitrarily oriented. It is important to check that the output data registers do not become saturated at the maximum positive or negative value to ensure clipping is not occurring. Thus, during self-test, a higher full-scale range (±4 *g* or higher) is selected to ensure proper results.

4 Self-test procedure

The self-test procedure relies on a serial communication interface between the sensor and a host MCU. The serial bus can be I^2C or SPI, as FXLS896xAF and FXLS897xCF support both types. In addition to the serial interface, an interrupt line is required between the host MCU and the sensor.

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In order to activate the self-test feature, the SENS_CONFIG1 register is accessed and programmed (address 15h). The SENS_CONFIG1 full content description and bit fields details are shown in the data sheet.

A full-scale measurement range of ±4 *g* or higher is recommended for self-test. Note that in ±16 *g* mode, 1 *g* corresponds to 128 LSBs, or equivalently, 1 LSB ≈ 7.81 m*g*, in ±8 *g* mode, 1 *g* corresponds to 256 LSBs, or equivalently, 1 LSB ≈ 3.91 m*g* and in ±4 *g* mode, 1 *g* corresponds to 512 LSBs, or equivalently, 1 LSB ≈ 1.95 m*g*.

The default output data rate (ODR) for self-test is 3200 Hz (this *out-of-reset* value can be subsequently changed by use of the SELF_TEST_CONFIG2 register). For more details, see Section 4.1.4 "SELF_TEST_CONFIG2 - self-test configuration register 2 (address 38h)". The self-test procedure detailed in this document uses an ODR of 100 Hz, which is realized by programming the SELF_TEST_CONFIG2 register with a value of 05h.

NXP recommends users avoid communication traffic on the device serial interface during the measurement phase of the sensor in order to reduce the susceptibility of the self-test response signal to induced noise. The most effective way to prevent induced noise during self-test is to employ data ready interrupts to synchronize the collection of data over serial interface and ensure digital communications do not coincide with the measurement phase of the self-test sequence.

When the BT_MODE pin is connected to V_{DD}, the data ready interrupt is signaled for TPULSE-MOT seconds (5 ms typ) and then is automatically cleared. As a result, the maximum recommended self-test ODR when the BT_MODE pin is connected to V_{DD} is 100 Hz.

When BT_MODE pin is connected to GND, the data ready interrupt clears immediately after reading the data. Therefore, self-test ODR can be configured up to 3200 Hz.

Note: *Only one axis can be tested at a time during self-test mode, because the signal chain processes only the selected axis. This is an important difference from normal operation, where all three axes are processed sequentially during a measurement cycle.*

After reviewing Section 4 "Self-test procedure", see Section 9 for example results.

4.1 Register used in the self-test procedure

For self-test configuration, the user needs to program specific settings in the following registers. Note that after a POR, soft-reset, or exit from Hibernate mode, these settings will be overwritten by the default values as indicated by the register description table in the data sheet.

The following sections summarize the bit fields relevant to the self-test sequence. The data sheet contains the full descriptions of the registers.

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Table 2. Key register involved in sensor self-test

Name	Address	Access	Comment	Accessibility
SENS_CONFIG1	15h	R/W	Full-scale range, self-test control, soft reset, Active mode enable	Read: always Write: standby mode only
SENS_CONFIG4	18h	R/W	Pulse generation option for DRDY event, output pin logic polarity and driver type	Read: always Write: standby mode only
SELF_TEST_CONFIG1	37h	R/W	Self-test idle phase duration	Read: always Write: standby mode only
SELF_TEST_CONFIG2	38h	R/W	Self-test measurement phase decimation factor	Read: always Write: standby mode only
INT_EN	20h	R/W	Interrupt output enable register	Read: always Write: standby mode only

4.1.1 SENS_CONFIG1 - sensor configuration register 1 (address 15h)

Table 3. SENS_CONFIG1 - sensor configuration register 1 (address 15h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	RST	ST_AXIS_SEL[1:0]		ST_POL	SPI_M	FSR[1:0]		ACTIVE
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Register reset value provided above assumes that BT_MODE = GND.

As this register is thoroughly described in the sensor product data sheet, the following table mainly summarizes the bit fields relevant to the self-test sequence.

Table 4. SENS_CONFIG1 - sensor configuration register 1 (address 15h) bit description

Bit	Name	Description
6 to 5	ST_AXIS_SEL[1:0]	Self-test axis selection **00 —** self-test function is disabled (reset value) **01 —** self-test function is enabled for X-axis **10 —** self-test function is enabled for Y-axis **11 —** self-test function is enabled for Z-axis
4	ST_POL	Self-test displacement polarity **0 —** Proof mass displacement for the selected axis is in the positive direction (reset value) **1 —** Proof mass displacement for the selected axis is in the negative direction

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Table 4. SENS_CONFIG1 - sensor configuration register 1 (address 15h) bit description*...continued*

Bit	Name	Description
3	SPI_M	SPI interface mode selection; selects between 3- and 4-wire operating modes for the SPI interface: **0 —** 4-wire interface mode is selected (reset value) **1 —** 3-wire interface mode is selected ***Notes:*** • *The state of this bit is only relevant when the SPI interface mode is selected (INTF_SEL = V_{DD}).* • *When INTF_SEL = V_{DD} and SPI_M = 1, the SDA/SPI_MOSI pin becomes the bidirectional SPI_DATA pin; the SA0/MISO pin is unused and placed in a high-impedance state.* • *4-wire mode is selected by default after a POR/BOR event or when exiting Hibernate mode.* • *If INTF_SEL = V_{DD} and the SPI_MOSI and SPI_MISO lines are directly connected together on the PCB, 3-wire SPI mode is enabled regardless of the setting of this bit*
2 to 1	FSR[1:0]	Full-scale measurement range (FSR) selection **00 —** ±2 *g*; 0.98 m*g*/LSB (1024 LSB/*g*) nominal sensitivity (reset value) **01 —** ±4 *g*; 1.95 m*g*/LSB (512 LSB/*g*) nominal sensitivity **10 —** ±8 *g*; 3.91 m*g*/LSB (256 LSB/*g*) nominal sensitivity **11 —** ±16 *g*; 7.81 m*g*/LSB (128 LSB/*g*) nominal sensitivity
0	ACTIVE	Standby/Active mode selection

4.1.2 SENS_CONFIG4 - sensor configuration register 4 (address 18h)

Table 5. SENS_CONFIG4 - sensor configuration register 4 (address 18h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	EXT_ TRIG_M	WAKE_ SDCD_WT	WAKE_ SDCD_OT	WAKE_ ORIENT	DRDY_PUL	INT2_FUNC	INT_ PP_OD	INT_POL
Reset	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 6. SENS_CONFIG4 field descriptions

Bit	Name	Description
3	DRDY_PUL	Pulse generation option for DRDY event **0 —** A SRC_DRDY event is output on the INTx pin as an active high or active low signal depending on the polarity setting made in INT_POL. The INTx pin will remain asserted until the host reads any of the OUT_X/Y/Z registers. (reset value) **1 —** A 32 µs (nominal) duration pulse is output on the configured INTx pin once per ODR cycle. The output pulse is either positive or negative, depending on the INT_POL setting. Note: The pulsed output signal is OR’d with all of the other interrupt events assigned to the INTx pin. Note: In Motion Detection mode (BT_MODE = V_{DD}), the state of this bit is ignored and has no effect on device operation.

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Table 6. SENS_CONFIG4 field descriptions*...continued*

Bit	Name	Description
1	INT_PP_OD	INT1 and INT2 pins output driver selection **0 —** INTx output pin driver is push-pull type. (reset value) **1 —** INTx output pin driver is open-drain/open-source type. An external pull-up/ pull-down resistor is required. ***Notes:*** • *If a user operation sets INT_PP_OD before issuing a soft reset command, the setting is maintained through the reset sequence (only lost when V_{DD} supply is removed or Hibernate mode is enabled).* • *The INT_PP_OD bit setting is ignored when BT_MODE = V_{DD} as the INT1/ MOT_DET and INT2/BOOT_OUT output driver type is fixed to open-drain.*
0	INT_POL	Interrupt logic polarity on INT1 and INT2 pins Selects the polarity of the interrupt output signal on the INT1 and INT2 pins. **0 —** Active low: interrupt events are signaled with a logical ‘0’ level. If DRDY_ PUL=1, a SRC_DRDY event pulse is negative going. The inactive state of the INTx pins is logic ‘1’ (V_{DD}). **1 —** Active high: interrupt events are signaled with a logical ‘1’ level. If DRDY_ PUL=1, a SRC_DRDY event pulse is positive going. The inactive state of the INTx pins is logic ‘0’ (GND). (reset value) ***Notes:*** • *If a user operation sets INT_POL before issuing a soft reset command the setting is maintained through the reset sequence (only lost if V_{DD} supply is removed or Hibernate mode is enabled).* • *The INT_POL bit setting is ignored when BT_MODE = V_{DD} as the INT1/ MOT_DET and INT2/BOOT_OUT interrupt logic polarity is fixed at active low (external pull-up resistor(s) is/are required).*

4.1.3 SELF_TEST_CONFIG1 - self-test configuration register 1 (address 37h)

Table 7. SELF_TEST_CONFIG1 - self-test configuration register1 (address 37h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	ST_IDLE[4:0]				
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 8. SELF_TEST_CONFIG1 (address 37h) bit description

Bit	Name	Description
4 to 0	ST_IDLE[4:0]	Self-test Idle phase duration: The value contained in ST_IDLE determines the Self-test Idle phase duration per the following equation: ST_ IDLE = 312.5 μs + (ST_IDLE[4:0] * 31.25) μs

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4.1.4 SELF_TEST_CONFIG2 - self-test configuration register 2 (address 38h)

Table 9. SELF_TEST_CONFIG2 - self-test configuration register1 (address 38h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	ST_DEC[3:0]			
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 10. SELF_TEST_CONFIG2 - self-test configuration register1 (address 38h) bit description

Bit	Name	Description
3 to 0	ST_DEC[3:0]	Self-test measurement phase decimation factor This bit field selects the self-test measurement phase decimation factor. The decimation selection ranges from 1 to 4096. The default ST_DEC setting (00h), configures ODR for self-test to be 3200 Hz.

Table 11. Self-test measurement phase decimation settings

ST_DEC[3]	ST_DEC[2]	ST_DEC[1]	ST_DEC[0]	Decimation selection (number of samples)	Self-test measurement period (ms)	Self-test ODR[1] (Hz)
0	0	0	0	1	0.3125	3200
0	0	0	1	2	0.625	1600
0	0	1	0	4	1.25	800
0	0	1	1	8	2.5	400
0	1	0	0	16	5	200
0	1	0	1	32	10	100
0	1	1	0	64	20	50
0	1	1	1	128	40	25
1	0	0	0	256	80	12.5
1	0	0	1	512	160	6.25
1	0	1	0	1024	320	3.125
1	0	1	1	2048	640	1.56125
1	1	0	0	4096	1280	0.78125
1	1	0	1	4096	1280	0.78125
1	1	1	0	4096	1280	0.78125
1	1	1	1	4096	1280	0.78125

[1] The ST recurrence and period shown in this table correspond to ST_IDLE = 0. Otherwise, the formula provided in note 1 shall be used.

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Notes:

1. *During the self-test sequence, the accelerometer measurement period in µs (for each axis and each direction) is given by the following equation:*
   ST_PERIOD (µs) = 2 $^{ST_DEC[3:0]}$ ** [312.5 + (ST_IDLE[4:0] * 31.25)] µs*
2. *The user-selected ODR in SENS_CONFIG3 register and power mode settings are ignored during self-test operation. The user-selected settings for ODR and power mode are applied after self-test is disengaged, for example, ST_AXIS_SEL[1:0] = 0b00.*

4.1.5 INT_EN - interrupt output enable register (address 20h)

This register is used to enable and disable the various interrupt event generators embedded within the device.

Table 12. INT_EN - interrupt output enable register (address 20h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	DRDY_EN	BUF_EN	SDCD_ OT_EN	SDCD_ WT_EN	ORIENT_ EN	ASLP_EN	BOOT_ DIS	WAKE_ OUT_EN
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 13. INT_EN - interrupt output enable register (address 20h) bit description

Bit	Name	Description
7	DRDY_EN	Data ready interrupt output enable **0 —** Interrupt is disabled (reset value) **1 —** Interrupt is enabled and signaled on either the INT1 or INT2 output pins as configured by the setting made in INT_PIN_SEL
5	SDCD_OT_EN	SDCD outside of thresholds interrupt output enable **0 —** Interrupt is disabled (reset value) **1 —** Interrupt is routed to either the INT1 or INT2 output pin as configured by the setting made in INT_PIN_SEL

4.1.6 Output data validity

Since the self-test output response takes time to settle to a final value after placing the device in ACTIVE mode, the following factors must be considered while collecting response data.

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Table 14. Valid output sample considerations

After placing the device in ACTIVE mode

Setting		Valid sample number/ data ready interrupt
ST_IDLE	ST_DEC	
00h	0 (self-test ODR = 3200 Hz)	fourth sample and later
00h	1 (self-test ODR = 1600 Hz)	third sample and later
00h	1 < ST_DEC < 5 (200 Hz ≤ self-test ODR ≤ 800 Hz)	second sample and later
00h	ST_DEC ≥ 5 (self-test ODR ≤ 100 Hz)	first sample and later

5 Self-test sequence per axis

1. Enter Standby mode by setting **SENS_CONFIG1[**ACTIVE**]** to 0 (address 15h)
2. Set the self-test measurement phase decimation factor **SELF_TEST_CONFIG2[**ST_DEC**]** to 05h (address 38h). In this procedure, Self-test ODR is set to 100 Hz.
   Note: Complete step 3 through step 9 for each axis (i = X, Y, Z).
3. **When BT_MODE = V_{DD},** enable data ready interrupt by setting **INT_EN**[DRDY_EN] bit to 1. Interrupt is routed to INT1 line. INT2 line cannot be used, because only BOOT interrupt can be routed to INT2 line when BT_MODE = V_{DD}.
   When BT_MODE = GND, enable data ready interrupt by setting **INT_EN**[DRDY_EN] bit to 1. Interrupt is routed to INT1 line. INT2 line can also be used. Enable pulse generation option for the DRDY event by setting **SENS_CONFIG4**[DRDY_PUL] bit to 1.
4. Write **SENS_CONFIG1** register (address 15h) with the following content
   - Enable self-test on the desired axis by setting ST_AXIS_SEL[1:0] to 0b01 for X-axis, 0b10 for Y-axis or 0b11 for Z-axis
   - Select self-test positive polarity by setting ST_POL to 0
   - Select FSR measurement range. In this example ±16 *g* range is selected by setting FSR[1:0] to 0b11
   - Select Active mode by setting ACTIVE to 1
5. Wait for DRDY interrupt. Upon reception of first data ready interrupt, enter Standby mode by setting **SENS_CONFIG1[**ACTIVE**]** to 0. For valid samples/data ready interrupt for each self-test ODR, see Table 14.
6. Read the acceleration data in the output registers corresponding to the selected axis (X data at register addresses 04h and 05h, Y data at register addresses 06h and 07h, Z data at register addresses 08h and 09h). Store the output data as a temporary variable, such as ST_OUTp(i).
7. Write **SENS_CONFIG1** register (address 15h) with the following content:
   - Enable self-test on the desired axis by setting ST_AXIS_SEL[1:0] to 0b01 for X-axis, 0b10 for Y-axis or 0b11 for Z-axis
   - Select self-test negative polarity by setting ST_POL to 1
   - Select Active mode by setting ACTIVE to 1
8. Wait for DRDY interrupt. Upon reception of first data ready interrupt, enter Standby mode by setting **SENS_CONFIG1[**ACTIVE**]** to 0. For valid samples/data ready interrupt for each self-test ODR, see Table 14.
9. Read the acceleration data in the output registers corresponding to the selected axis (X data at register addresses 04h and 05h, Y data at register addresses 06h and

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07h, Z data at register addresses 08h and 09h). Store the output data as a temporary variable, such as ST_OUTm(i).

Self-test measurement phase per axis

Complete the following steps List item through step List item for each axis (i = X,Y,Z).

Assuming there was no output data clipping, such as the maximum positive value not equal to +2047 and maximum negative value not equal to –2048, the self-test output change (STOC) for each axis can be computed with the following equation:

$$STOC(i) = \frac{ST_OUTp(i) - ST_OUTm(i)}{2}$$

The STOC(i) value can be compared to the data sheet specification for a given axis and FSR *g* range. If LSL (Lower Spec Limit in LSB) ≤ STOC ≤ USL (Upper Spec Limit in LSB), the device passed self-test. The LSL and USL values are based on the FSR range and axis under test (X or Y or Z). See Table 27

As mentioned in the measurement procedure, it is important that the host MCU collects measurement data only in interrupt mode. Interrupt mode is enabled using the INT_EN (address 20h) and INT_PIN_SEL (address 21h) registers.

Map the data ready interrupt to one of the INTx pins available on the device and wait for the event to be signaled to the host MCU before reading data. See DRDY_EN field of the INT_EN register (address 20h) and DRDY_INT2 field of the INT_PIN_SEL register (address 21h). In that case, sensor data collection is handled very effectively by the host MCU with an interrupt service routine. In the case of BT_MODE = V_{DD} (motion detect mode), INT2 pin function is reserved for boot output pulse, thus is not available for this purpose. Consequently, only INT1 pin can be used.

The user-selected ODR and power mode are overridden during self-test operation. They are restored when self-test is disengaged, such as when ST_AXIS_SEL[1:0] = 0b00 and ACTIVE is set back again to 1.

6 Sensor Data Change Detection (SDCD) block validation through self-test

Besides basic verification of MEMS transducer and ASIC signal chain, the self-test feature can also be utilized to verify some of the embedded features of the sensor. This section describes how to verify the SDCD block in the ASIC through self-test.

After reviewing Section 6 "Sensor Data Change Detection (SDCD) block validation through self-test", see Section 9.3 "Example implementation for SDCD block validation"

6.1 SDCD block validation principle

The Sensor Data Change Detection (SDCD) block is an inertial event detection function available to assist host software algorithms in detecting various inertial events such as motion/no-motion (key fob), high-*g*/low-*g*, tap/double tap and transient acceleration events.

It incorporates a flexible digital window comparator block useful for implementing several different interrupt generation functions. The circuit may be operated in either relative or

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absolute modes and features user-programmable debounce times, polarity detection and interrupt generation logic.

Since **self-test response is an inertial event caused by an electrostatic actuation force applied to the proof mass**, this event can be detected by the SDCD block as a motion event. The generation of a motion detection interrupt in response to self-test stimulus verifies proper operation of the SDCD block. It is also to be noted that, indirectly, the interrupt capabilities of the sensor are also being validated.

The device's response to a self-test stimulus on a specific axis and polarity (direction) is a DC signal that does not vary with any physical acceleration applied to the device. Thus, the device need not be static while executing self test.

When this response signal is used as an input to the SDCD block in absolute comparison mode against a defined threshold (as shown in Figure 1), this inertial event caused by the self-test stimulus is detected as an Outside-of Thresholds (OT) event, when the magnitude of the response signal is greater than the threshold. A corresponding motion detection interrupt will also be triggered for the event.

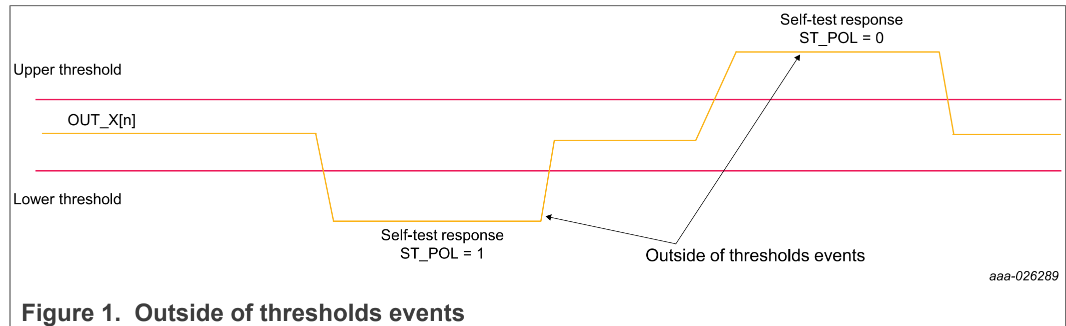

Figure 1. Outside of thresholds events

6.2 Registers used in the SDCD block validation procedure

Apart from the registers configured for self test (Section 4.1), the following SDCD registers require configuration.

Table 15. SDCD registers requiring configuration

Name	Address	Access	Comment	Accessibility
SDCD_CONFIG1	2Fh	R/W	Sensor Data Change Detection function configuration register 1 – Event latch enable and individual axis enable bits for OT and WT logic function participation.	Read: always Write: standby mode only
SDCD_CONFIG2	30h	R/W	Sensor Data Change Detection function configuration register 2 – SDCD function enable, reference values initialization and update behavior, relative/absolute operating mode selection, debounce counter behavior.	Read: always Write (REF_UPD bit): always Write (all other bits): standby mode only
SDCD_LTHS_LSB	33h	R/W	Sensor Data Change Detection lower threshold value LSB - sdcd_lths[7:0]	Read: always Write: standby mode only

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Table 15. SDCD registers requiring configuration*...continued*

Name	Address	Access	Comment	Accessibility
SDCD_LTHS_MSB	34h	R/W	Sensor Data Change Detection lower threshold value MSB - sdcd_ lths[11:8].	Read: always Write: standby mode only
SDCD_UTHS_LSB	35h	R/W	Sensor Data Change Detection upper threshold value LSB - sdcd_ uths[7:0]	Read: always Write: standby mode only
SDCD_UTHS_MSB	36h	R/W	Sensor Data Change Detection upper threshold value MSB - sdcd_ uths[11:8]	Read: always Write: standby mode only
INT_EN	20h	R/W	Interrupt output enable register	Read: always Write: standby mode only

As these registers are thoroughly described in the data sheet, the following tables mainly summarize the bit fields relevant to the validation procedure.

6.2.1 SDCD_CONFIG1 - SDCD function configuration register 1 (address 2Fh)

Table 16. SDCD_CONFIG1 - SDCD function configuration register 1 (address 2Fh) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	OT_ELE	WT_ELE	X_OT_EN	Y_OT_EN	Z_OT_EN	X_WT_EN	Y_WT_EN	Z_WT_EN
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	0	1	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 17. SDCD_CONFIG1 - SDCD function configuration register 1 (address 2Fh) bit description

Bit	Name	Description
5	X_OT_EN	SDCD function X-axis outside-of-thresholds condition 0: X-axis data or delta is not used in the outside of thresholds condition evaluation. 1: X-axis data or delta is used in the outside of thresholds condition evaluation.
4	Y_OT_EN	SDCD function Y-axis outside-of-thresholds condition 0: Y-axis data or delta is not used in the outside of thresholds condition evaluation. 1: Y-axis data or delta is used in the outside of thresholds condition evaluation.
3	Z_OT_EN	SDCD function Z-axis outside-of-thresholds condition 0: Y-axis data or delta is not used in the outside of thresholds condition evaluation. 1: Y-axis data or delta is used in the outside of thresholds condition evaluation.

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6.2.2 SDCD_CONFIG2 - SDCD function configuration register 2 (address 30h)

Table 18. SDCD_CONFIG2 - SDCD function configuration register 2 (address 30h) bit allocation

Bit	7	6	5	4	3	2	1	0
Read	SDCD_EN	REF_UPDM[1:0]		OT_ DBCTM	WT_ DBCTM	WT_ LOG_SEL	MODE	REF_UPD
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	1	1	0	1	1	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 19. SDCD_CONFIG2 - SDCD function configuration register 2 (address 30h) bit description

Bit	Name	Description
7	SDCD_EN	SDCD function 0 (default after a POR or soft reset event when BT_MODE = GND): SDCD function is disabled. All clocks and power for the function are turned off. 1 (default after a POR or soft reset event when BT_MODE = V_{DD} and MOT_DET = 1): SDCD function is enabled. When this bit is set, the 12-bit reference values (**REF_X/Y/Z**) are initialized per the settings made in REF_UPDM[1:0].
6 to 5	REF_UPDM	SDCD internal reference values update mode 00: The function stores the first 12-bit X/Y/Z decimated and trimmed input data (OUT_X/Y/Z[n=0]) as the internal REF_X/Y/Z values after the function is enabled (SDCD_EN is set to 1). The REF_X/Y/Z values are updated with the current 12-bit X/Y/Z decimated input data (OUT_X/Y/Z[n]) at the time the SDCD_OT_EA flag transitions from False to True. 01: The function stores the first decimated and trimmed X/Y/Z acceleration input data (OUT_X/Y/Z[n=0]) as the internal REF_X/Y/Z values when the SDCD function is enabled; the REF_X/Y/Z values are then held constant and never updated until the SDCD function is disabled and subsequently re-enabled, or asynchronously when the REF_UPD bit is set by the host. 10: The function updates the SDCD_REF_X/Y/Z values with the current decimated and trimmed X/Y/Z acceleration input data after the function evaluation. This allows for acceleration slope detection with Data(n) to Data(n–1) always used as the input to the window comparator. 11: The function uses a fixed value of 0 for each of the SDCD_REF_X/Y/Z registers, making the function operate in absolute comparison mode.
4	OT_DBCTM	SDCD outside-of-threshold event debounce counter behavior 0 (default): Debounce counter is decremented by 1 when the current outside of thresholds result for the enabled axes is false. In this mode, the debounce counter de-bounces the outside of thresholds event in both directions, meaning that once the event flag has been set (after SDCD_OT_DBCNT ODR periods with the condition true), the condition must also remain false for at least SDCD_OT_DBCNT + 1 consecutive ODR periods before the next event detection cycle can begin. 1: Debounce counter is cleared whenever the current outside of thresholds result for the enabled axes is false.

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6.2.3 SDCD_LTHS_LSB - SDCD lower threshold value register LSB (address 33h)

Sensor Data Change Detection function 12-bit 2's complement lower threshold least significant byte. **SDCD_LTHS[**11:0**]** must always be set to a lower value than **SDCD_UTHS[**11:0**]** to ensure that the SDCD circuit functions correctly and produces meaningful results.

The scaling for this register is always the same as the selected FSR's sensitivity.

Table 20. SDCD_LTHS_LSB - SDCD lower threshold value register LSB (address 33h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SDCD_LTHS[7:0]							
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	1	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.4 SDCD_LTHS_MSB - SDCD lower threshold value register MSB (address 34h)

Sensor Data Change Detection function 12-bit 2's complement lower threshold most significant byte (nibble). **SDCD_LTHS[**11:0**]** must always be set to a lower value than **SDCD_UTHS[**11:0**]** to ensure that the SDCD circuit functions correctly and produces meaningful results.

The scaling for this register is always the same as the selected FSR's sensitivity.

Table 21. SDCD_LTHS_MSB - SDCD lower threshold value register MSB (address 34h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	—				SDCD_LTHS[11:8]			
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	0	0	0	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.5 SDCD_UTHS_LSB - SDCD upper threshold value LSB (address 35h)

Sensor Data Change Detection function 12-bit 2's complement upper-threshold least significant byte. **SDCD_UTHS[**11:0**]** must always be set to a higher value than **SDCD_LTHS[**11:0**]** to ensure that the SDCD circuit functions correctly and produces meaningful results.

The scaling for this register is the same as the selected FSR sensitivity.

Table 22. SDCD_UTHS_LSB - SDCD upper threshold value LSB (address 35h) bit allocation

Bit	7	6	5	4	3	2	1	0
Name	SDCD_UTHS[7:0]							
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	1	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

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6.2.6 SDCD_UTHS_MSB - SDCD upper threshold value MSB (address 36h)

Sensor Data Change Detection function 12-bit 2’s complement upper-threshold most-significant byte (nibble). **SDCD_UTHS[**11:0**]** must always be set to a higher value than **SDCD_LTHS[**11:0**]** to ensure that the SDCD circuit functions correctly and produces meaningful results.

The scaling for this register is always the same as the selected FSR’s sensitivity.

Table 23. SDCD_UTHS_MSB - SDCD upper threshold value MSB (address 36h) bit allocation

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	—				SDCD_UTHS[11:8]			
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

6.2.7 INT_EN - interrupt output enable register (address 20h)

This register is used to enable and disable the various interrupt event generators embedded within the device.

Table 24. INT_EN - interrupt output enable register (address 20h) bit allocation

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DRDY_EN	BUF_EN	SDCD_ OT_EN	SDCD_ WT_EN	ORIENT_ EN	ASLP_EN	BOOT_ DIS	WAKE_ OUT_EN
Reset (BT_MODE = GND)	0	0	0	0	0	0	0	0
Reset (BT_MODE = V_{DD})	0	0	1	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 25. INT_EN - interrupt output enable register (address 20h) bit description

Bit	**Name**	**Description**
7	DRDY_EN	Data ready interrupt output enable **0 —** Interrupt is disabled (reset value) **1 —** Interrupt is enabled and signaled on either the INT1 or INT2 output pins as configured by the setting made in INT_PIN_SEL
5	SDCD_OT_EN	SDCD outside of thresholds interrupt output enable **0 —** Interrupt is disabled (reset value) **1 —** Interrupt is routed to either the INT1 or INT2 output pin as configured by the setting made in INT_PIN_SEL

6.3 Self-test sequence for SDCD block validation (BT_MODE = V_{DD})

SDCD block validation phase per axis

Complete the following procedure for each axis (i = X, Y, Z).

The steps below refer to the serial commands as shown in Figure 2 and Figure 3.

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1. Enter Standby mode by setting **SENS_CONFIG1[**ACTIVE**]** to 0 (address 15h).
2. Configure registers.
   a. Set the Self-test measurement phase decimation factor by setting **SELF_TEST_CONFIG2[**ST_DEC**]** to 05h (address 38h). In this example, Self-test ODR is set to 100 Hz. Note that when BT_MODE pin is connected to VDD, the data ready interrupt is signaled for $T_{PULSE\text{-}MOT}$ seconds (5 ms typ) and it clears itself automatically. Hence maximum recommended ODR when BT_MODE pin is connected to VDD is 100 Hz.
   b. Enable data ready interrupt by setting **INT_EN**[DRDY_EN] bit to 1. Interrupt is routed to INT1 line. INT2 line cannot be used, because only BOOT interrupt can be routed to INT2 line when BT_MODE = V_{DD}.
   c. Write **SENS_CONFIG1** register (address 15h) with the following content:
      i. Self-test enabled on the desired axis by setting ST_AXIS_SEL[1:0] to 0b01 for X-axis, 0b10 for Y-axis or 0b11 for Z-axis
      ii. Self-test positive polarity selected by setting ST_POL to 0
      iii. Select FSR measurement range. In this example ±16 *g* range is selected by setting FSR[1:0] to 0b11
      iv. Active mode selected by setting ACTIVE to 1
3. Wait for DRDY interrupt. Upon reception of the first data ready interrupt, put device in Standby mode by setting **SENS_CONFIG1[**ACTIVE**]** to 0 (address 15h). Read the acceleration data in the output registers corresponding to the selected axis (X data at register addresses 04h and 05h, Y data at register addresses 06h and 07h, Z data at register addresses 08h and 09h). Store the output data as a temporary variable, such as ST_OUTp(i).
4. Write **SENS_CONFIG1** register (address 15h) with the following content:
   a. Self-test enabled on the desired axis by setting ST_AXIS_SEL[1:0] to 0b01 for X-axis, 0b10 for Y-axis or 0b11 for Z-axis
   b. Self-test negative polarity selected by setting ST_POL to 1
   c. Active mode selected by setting ACTIVE to 1
5. Wait for DRDY interrupt. Upon reception of the first data ready interrupt, put device in Standby mode by setting **SENS_CONFIG1[**ACTIVE**]** to 0 (address 15h). Read the acceleration data in the output registers corresponding to the selected axis (X data at register addresses 04h and 05h, Y data at register addresses 06h and 07h, Z data at register addresses 08h and 09h). Store the output data as a temporary variable, such as ST_OUTm(i).
6. Measure self-test output change, self-test offset and configure registers.
   a. Calculate Self-Test Output Change (STOC). If LSL (Lower Spec Limit in LSB) ≤ STOC ≤ USL (Upper Spec Limit in LSB), the device passed self-test. LSL and USL values are based on the FSR range and axis under test (X or Y or Z). See Table 27.
   b. Calculate Self-Test Offset in LSBs (counts).
      Set SDCD thresholds based on Self-test Offset Value.
      Let W = min(abs(LSL), abs(USL)).
      SDCD Upper Threshold = Self-Test Offset + 'W' LSBs.
      SDCD Lower Threshold = Self-Test Offset – 'W' LSBs.

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   c. Write the calculated threshold values into the appropriate registers SDCD_LTHS_LSB (33h), SDCD_LTHS_MSB (34h), SDCD_UTHS_LSB(35h), SDCD_UTHS_MSB (36h).
   d. Write **SDCD_CONFIG1** register (address 2Fh) with the following content:
      i. Enable SDCD function for OT event detection- X_OT_EN for X-axis, Y_OT_EN for Y-axis, Z_OT_EN for z-axis. Enable OT event only for the selected axis and disable for the other two axes.
   e. Write **SDCD_CONFIG2** register (address 30h) with the following content:
      i. Enable SDCD function in absolute mode by setting SDCD_EN bit to 1 and REF_UPDM[1:0] = 0b11.
      ii. Set OT debounce counter behavior to clear by setting OT_DBCTM bit to 1.
   f. Disable data ready interrupt and enable OT interrupt by setting SDCD_OT_EN bit to 1 and DRDY_EN bit to 0 in INT_EN (20h) register. Let SDCD_OT interrupt be routed to INT1 by default. INT2 line cannot be used, because only BOOT interrupt can be routed to INT2 line under BT_MODE = V_{DD}.
   g. Write **SENS_CONFIG1** register (address 15h) with the following content:
      i. Self-test enabled on the desired axis by setting ST_AXIS_SEL[1:0] to 0b01 for X-axis, 0b10 for Y-axis or 0b11 for Z-axis
      ii. Self-test positive polarity selected by setting ST_POL to 0
      iii. Active mode selected by setting ACTIVE to 1
7. Wait for motion detection interrupt. Self-test stimulus should cause an OT event and motion detection interrupt should be obtained on INT1. Upon reception of motion detection interrupt, put device in Standby mode by setting **SENS_CONFIG1 [**ACTIVE**]** to 0 (address 15h).
8. Write **SENS_CONFIG1** register (address 15h) with the following content:
   a. Self-test enabled on the desired axis by setting ST_AXIS_SEL[1:0] to 0b01 for X-axis, 0b10 for Y-axis or 0b11 for Z-axis
   b. Self-test negative polarity selected by setting ST_POL to 1
   c. Active mode selected by setting ACTIVE to 1
9. Wait for motion detection interrupt. Upon reception of motion detection interrupt, put device in Standby mode by setting **SENS_CONFIG1 [**ACTIVE**]** to 0 (address 15h).
10. Disable self-test (ST_AXIS_SEL = 0b00). Place device back in Active mode by setting **SENS_CONFIG1 [**ACTIVE**]** to 1 (address 15h).

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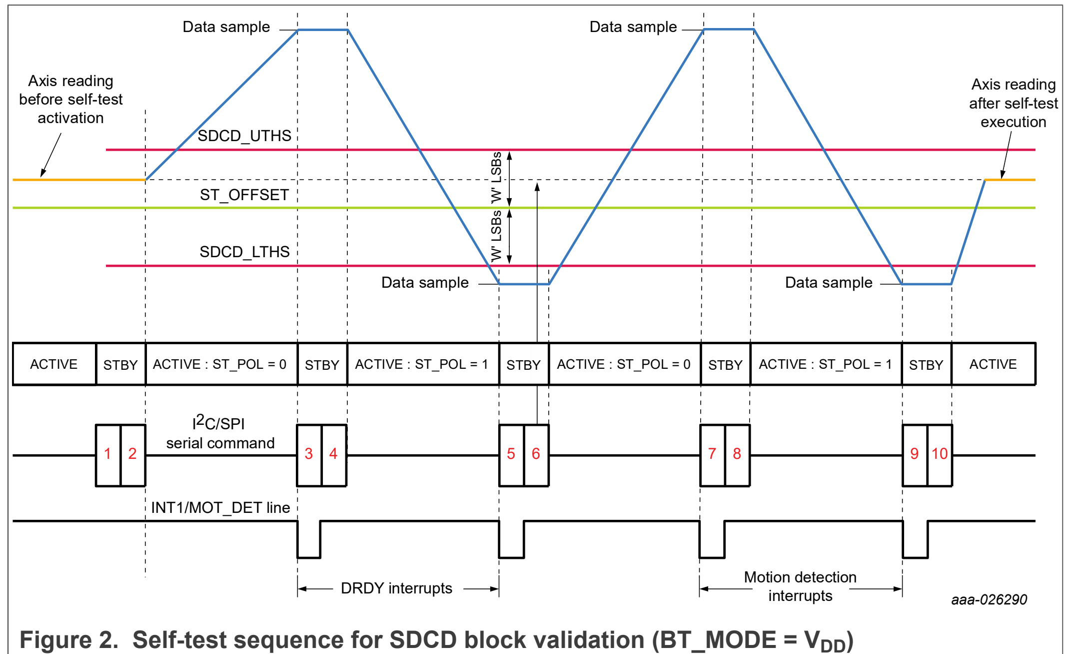

Figure 2. Self-test sequence for SDCD block validation (BT_MODE = V_{DD})

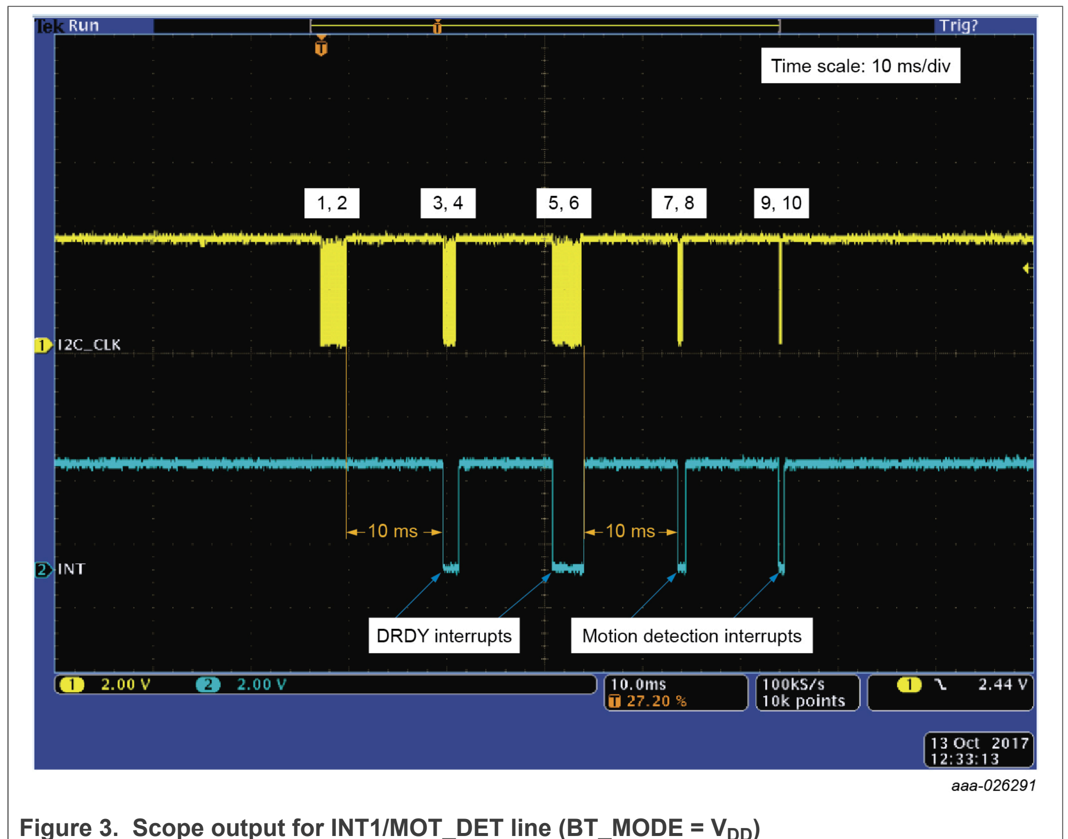

Figure 3. Scope output for INT1/MOT_DET line (BT_MODE = V_{DD})

In BT_MODE = V_{DD}, DRDY interrupt and motion detection interrupt pulse width = 5 ms ($T_{PULSE-MOT}$ (typ)). The current interrupt pulse will be terminated when the device undergoes Active-Standby-Active transition before the pulse completion and thus may not span for entire 5 ms ($T_{PULSE-MOT}$ (typ)).

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For example, command 5 in Figure 2 puts the device in Active mode. The corresponding DRDY interrupt is terminated immediately.

6.4 Self-test sequence for SDCD block validation (BT_MODE = GND)

SDCD block validation phase per axis

Complete the following procedure for each axis (i = X,Y,Z).

The steps below refer to the serial commands as shown in Figure 4 and Figure 5.

1. Enter Standby mode by setting **SENS_CONFIG1[**ACTIVE**]** to 0 (address 15h).
2. Configure registers.
   a. Set the Self-test measurement phase decimation factor by setting **SELF_TEST_CONFIG2[**ST_DEC**]** to 04h (address 38h). In this example, Self-test ODR is set to 200 Hz.
   b. Enable data ready interrupt by setting **INT_EN**[DRDY_EN] bit to 1. Interrupt is routed to INT1 line. INT2 line can also be used.
   c. Enable pulse generation option for DRDY event by setting **SENS_CONFIG4**[DRDY_PUL] bit to 1.
   d. Write **SENS_CONFIG1** register (address 15h) with the following content
      i. Self-test enabled on the desired axis by setting ST_AXIS_SEL[1:0] to 0b01 for X-axis, 0b10 for Y-axis or 0b11 for Z-axis
      ii. Self-test positive polarity selected by setting ST_POL to 0
      iii. Select FSR measurement range. In this example ±16 *g* range is selected by setting FSR[1:0] to 0b11
      iv. Active mode selected by setting ACTIVE to 1
3. Wait for DRDY interrupt. Upon reception of the first data ready interrupt, no action is required. Discard the data ready interrupt (no need to read the data -ignore this sample) (see Section 4.1.6). Since the pulse generation option is enabled for data ready interrupt (through DRDY_PUL bit), the data ready interrupt clears itself after 32 µs.
4. Upon reception of second data ready interrupt, put device in Standby mode by setting **SENS_CONFIG1[**ACTIVE**]** to 0 (address 15h). Read the acceleration data in the output registers corresponding to the selected axis (X data at register addresses 04h and 05h, Y data at register addresses 06h and 07h, Z data at register addresses 08h and 09h). Store the output data as a temporary variable, such as ST_OUTp(i).
5. Write **SENS_CONFIG1** register (address 15h) with the following content:
   a. Self-test enabled on the desired axis by setting ST_AXIS_SEL[1:0] to 0b01 for X-axis, 0b10 for Y-axis or 0b11 for Z-axis
   b. Self-test negative polarity selected by setting ST_POL to 1
   c. Active mode selected by setting ACTIVE to 1
6. Wait for DRDY interrupt. Upon reception of the first data ready interrupt, no action is required. Discard the data ready interrupt (no need to read the data -ignore this sample) (see Section 4.1.6). Since the pulse generation option is enabled for data ready interrupt (through DRDY_PUL bit), the data ready interrupt clears itself after 32 µs.
7. Upon reception of second data ready interrupt, put device in Standby mode by setting **SENS_CONFIG1[**ACTIVE**]** to 0 (address 15h). Read the acceleration data in the output registers corresponding to the selected axis (X data at register addresses 04h

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and 05h, Y data at register addresses 06h and 07h, Z data at register addresses 08h and 09h). Store the output data as a temporary variable, such as ST_OUTm(i).

8. Measure self-test output change, self-test offset and configure registers.
   a. Calculate Self-Test output change (STOC). If LSL (Lower Spec Limit in LSB) <= STOC <= USL (Upper Spec Limit in LSB), the device passed self-test. LSL and USL values are based on the FSR range and axis under test (X or Y or Z). See Table 27.
   b. Calculate Self-test Offset in LSBs (counts).
      Set SDCD thresholds based on Self-test Offset Value.
      Let W = min(abs(LSL), abs(USL)).
      SDCD Upper Threshold = Self-Test Offset + 'W' LSBs.
      SDCD Lower Threshold = Self-Test Offset – 'W' LSBs.
   c. Write the calculated threshold values into the appropriate registers SDCD_LTHS_LSB (33h), SDCD_LTHS_MSB (34h), SDCD_UTHS_LSB(35h), SDCD_UTHS_MSB (36h).
   d. Write **SDCD_CONFIG1** register (address 2Fh) with the following content:
      i. Enable SDCD function for Outside-of-thresholds event detection- X_OT_EN for X-axis, Y_OT_EN for Y-axis, Z_OT_EN for Z-axis. Enable OT event only for the selected axis and disable for the other two axes.
   e. Write **SDCD_CONFIG2** register (address 30h) with the following content:
      i. Enable SDCD function in absolute mode by setting SDCD_EN bit to 1 and REF_UPDM[1:0] = 0b11.
      ii. Set Outside-of-thresholds debounce counter behavior to clear by setting OT_DBCTM bit to 1.
   f. Disable data ready interrupt and enable OT interrupt by setting SDCD_OT_EN bit to 1 and DRDY_EN bit to 0 in INT_EN (20h) register. Let SDCD_OT interrupt be routed to INT1. INT2 line can also be used.
   g. Write **SENS_CONFIG1** register (address 15h) with the following content:
      i. Self-test enabled on the desired axis by setting ST_AXIS_SEL[1:0] to 0b01 for X-axis, 0b10 for Y-axis or 0b11 for Z-axis
      ii. Self-test positive polarity selected by setting ST_POL to 0
      iii. Active mode selected by setting ACTIVE to 1
9. Wait for motion detection interrupt. Self-test stimulus should cause an OT event and motion detection interrupt should be obtained on INT1. Note that since the first sample (immediately after self-test stimulus) does not reflect a truly settled response, the motion detection interrupt may not be observed until the second sample.
   Upon reception of motion detection interrupt, put device in Standby mode by setting **SENS_CONFIG1 [**ACTIVE**]** to 0 (address 15h).
10. Write **SENS_CONFIG1** register (address 15h) with the following content:
    a. Self-test enabled on the desired axis by setting ST_AXIS_SEL[1:0] to 0b01 for X-axis, 0b10 for Y-axis or 0b11 for Z-axis
    b. Self-test negative polarity selected by setting ST_POL to 1
    c. Active mode selected by setting ACTIVE to 1
11. Wait for motion detection interrupt. Note that since the first sample (immediately after self-test stimulus) does not reflect a truly settled response, the motion detection interrupt may not be observed until the second sample.
    Upon reception of motion detection interrupt, put device in Standby mode by setting **SENS_CONFIG1 [**ACTIVE**]** to 0 (address 15h).
12. Disable Self-test (ST_AXIS_SEL = 0b00). Place device back in Active mode by setting **SENS_CONFIG1[**ACTIVE**]** to 1 (address 15h).

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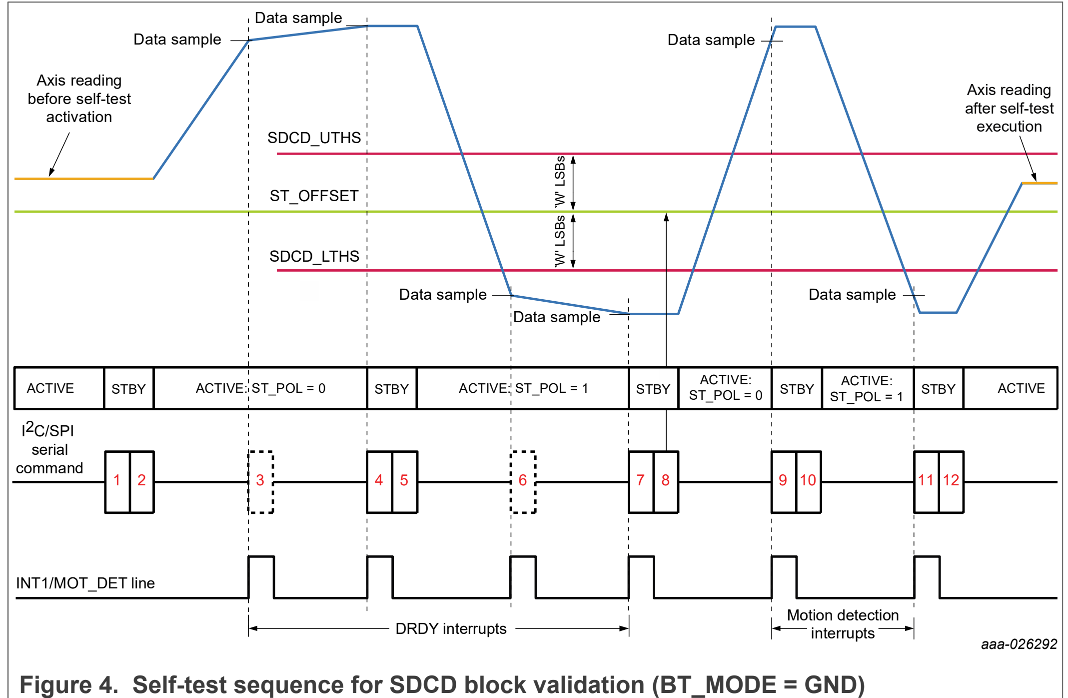

Figure 4. Self-test sequence for SDCD block validation (BT_MODE = GND)

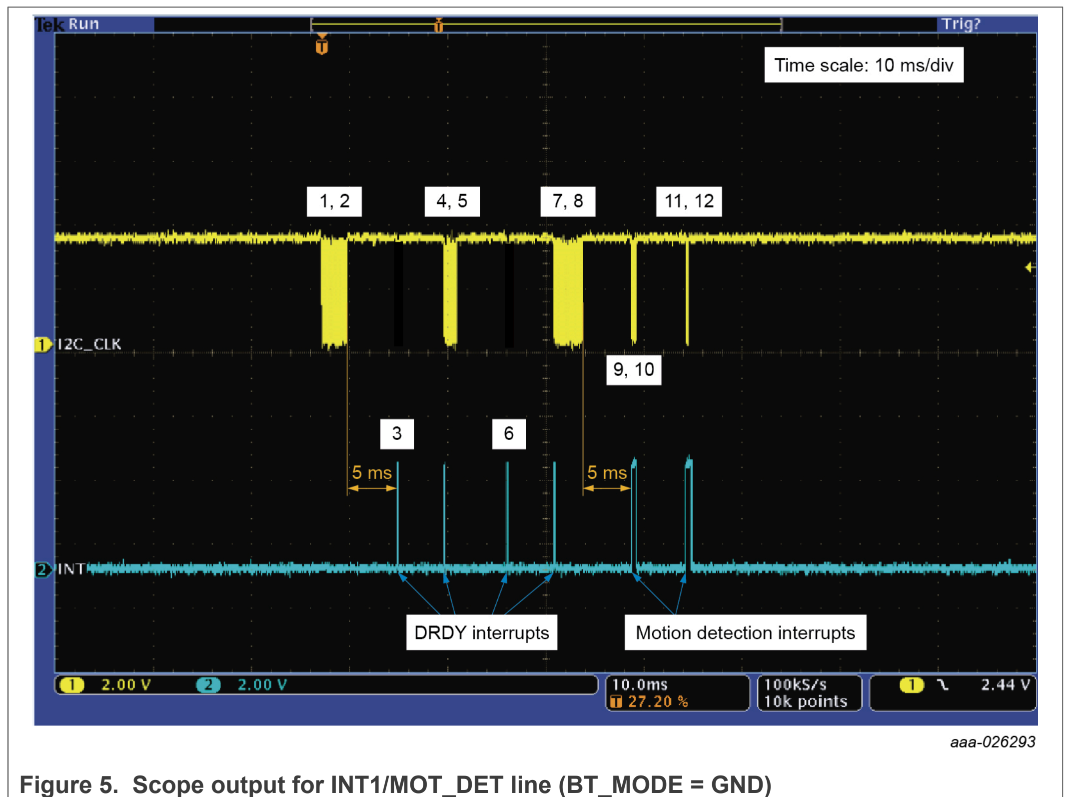

Figure 5. Scope output for INT1/MOT_DET line (BT_MODE = GND)

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7 Important considerations

As already mentioned in Section 4, it is important to avoid read or write transactions on the digital communication interface while the sensitive self-test measurements are being performed by the sensor. Toggling data/clock lines may induce digital noise and degrade accuracy of the measurement.

The best solution to achieve this is to use the sensor data ready interrupt line to ensure the measurement phase is completed before fetching the output data registers. As the total self-test sequence duration is small (for example: 6 x 10 ms when self-test ODR = 100 Hz), preventing the interface usage during that time is not a severe restriction.

If the Data Ready interrupt synchronous reading scheme cannot be implemented, instead of polling the sensor status register to check when data ready flag is set, NXP recommends programming a fixed delay (e.g. with host MCU programmable timer) to trigger the data reading. This delay corresponds to the slowest measurement period taking into account the ODR tolerance.

Numerical example for self-test ODR = 100 Hz: Delay = 1/100 Hz × (1 + 10 %) = 10 ms × 1.1 = 11 ms.

Another suggestion to make the self-test sequence highly robust and reliable, is to perform an immediate retest to confirm or discard a potential self-test failure diagnostic.

In other words, if the outcome of a first self-test sequence is “not ok” (at least one axis is out of spec), NXP advises running it again (immediately afterwards) to confirm the failure is indeed consistent and repeatable. This sort of “debouncing” method avoids an incorrect diagnosis made on the DUT whereas the measurement or sequence was corrupted by an unexpected external factor such as a significant and fast mechanical shock or transient electrical perturbation.

8 Summary and conclusion

The self-test feature available in FXLS896xAF and FXLS897xCF accelerometer family provides a first level diagnostic for device functionality. An automated sequence can be performed quickly by the host MCU to ensure that sensor MEMS and ASIC signal chain are operating properly. The outcome of the sequence can be compared to sensor self-test specification as a pass/fail criteria or, even better, to part-specific self-test data baseline captured during end product manufacturing and stored in the host NVM for future reference in the field. Apart from basic signal chain verification, the self-test feature can also be utilized to validate some of the embedded functional blocks in the sensor such as the Sensor Data Change Detection Block.

9 Appendix A

9.1 Reference self-test procedure results

The following section presents reference self-test sequence results for FXLS8964AF. Refer to respective device data sheet to check on valid MIN/MAX ranges for self-test output. The self-test-sequence was run on a sample set of parts (DUTs) and the outcome is presented hereafter. To review the procedure, see Section 4 "Self-test procedure".

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Table 26. Self-test measurement results for ±16G full scale range configuration

Axis	Output data (counts)[1]			
	ST_POL = 0	ST_POL = 1	Self-test Offset	Self-test output change (STOC)
X	–45	23	–11	–34
Y	25	–38	–6	31
Z	–121	91	–15	–106

[1] For related data plots, see Section 9.2 "Output data plots during self-test sequence".

Note: *Refer to the FXLS8964AF data sheet for valid self-test limits.*

$$Self\text{-}test\ offset(i) = \frac{ST_OUTp(i) + ST_OUTm(i)}{2}$$

Table 27. Self-test output change limits

FSR range (axes)	Min	Typ	Max	Unit
±4 *g* mode, X axis	–206	–139	–81	LSB
±4 *g* mode, Y axis	78	137	207	
±4 *g* mode, Z axis	–727	–448	–120	
±8 *g* mode, X axis	–103	–69	–40	
±8 *g* mode, Y axis	38	68	103	
±8 *g* mode, Z axis	–355	–223	–71	
±16 *g* mode, X axis	–52	–35	–19	
±16 *g* mode, Y axis	19	34	52	
±16 *g* mode, Z axis	–178	–112	–35	

9.2 Output data plots during self-test sequence

This section presents example output X, Y, Z plots for FXLS8964AF during self-test sequence. To review the procedure, see Section 5 "Self-test sequence per axis".

At the beginning, the sensor is operating in low-power active mode with the device in an approximately horizontal position. Therefore, X- and Y-axis data are close to 0 *g* and Z-axis data is close to 1 *g*.

A self-test sequence is then engaged for X-axis with positive polarity (first transition), and later on with negative polarity (second transition).

Then self-test is changed to Y-axis with positive polarity (third transition), and later on with negative polarity (fourth transition).

Note: *The signal chain is only processing the selected axis during self-test. Therefore, the output data registers content for the two others axes is frozen (preserved and not updated). NXP does not recommend using the output data from those unselected axes.*

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The self-test is then changed to Z-axis with positive polarity (fifth transition), and later on with negative polarity (sixth transition).

Finally, at the end of the plot, the sensor normal operation is restored (seventh transition, low-power active mode), and the XYZ data reflect the DUT horizontal position such as prior to the self-test sequence. Figure 6 describes complete self-test response (X, Y, Z axes).

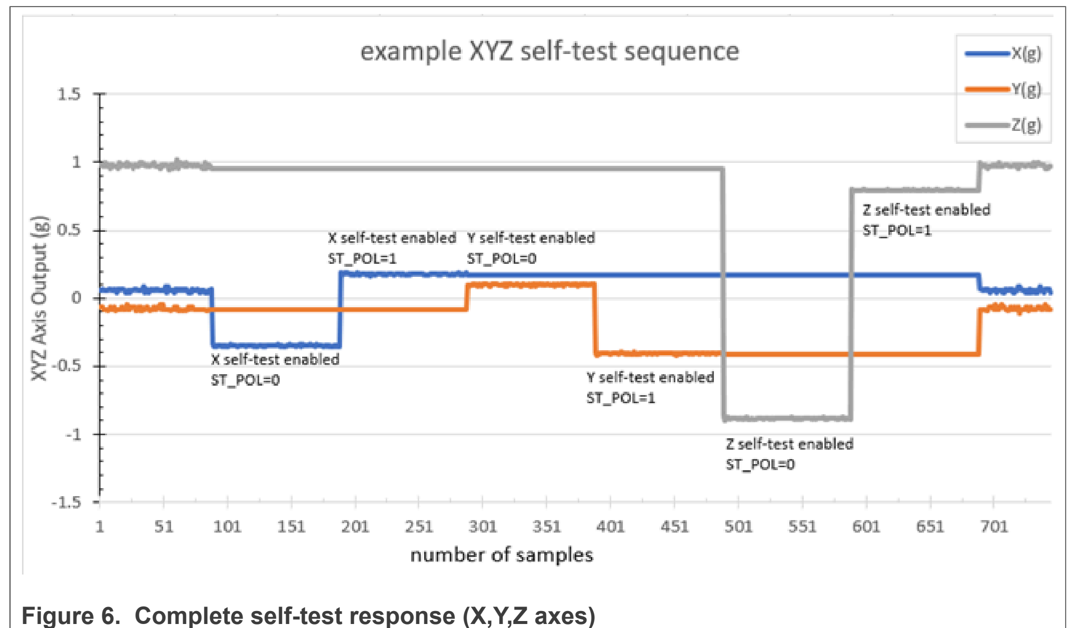

Figure 6. Complete self-test response (X,Y,Z axes)

9.3 Example implementation for SDCD block validation

Following is a sample implementation of the validation sequence discussed in Section 6.3 (with BT_MODE = V_{DD}). X-Axis is considered here. Full scale range is set to ±16 *g*. Self-test ODR is set to 100 Hz. To review the procedure, see Section 6 "Sensor Data Change Detection (SDCD) block validation through self-test".

All values shown in the sample calculation are in counts (LSBs) and showing self-test reference results performed on FXLS8964AF. The steps are:

1. Measure self-test response for both positive and negative stimulus.

Table 28. Self-test measurements for X-axis

Self-test polarity	X (LSBs)	Y (LSBs)	Z (LSBs)
ST_POL = 0	–45	7	129
ST_POL = 1	23	7	129

2. Calculate Self-test Offset.

Self-test Offset = (–45 + (23)) / 2

= –11

Self-test Offset = –11 LSBs

Calculate Self-test output change (STOC)

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STOC = (–45 – (23)) / 2
= –34

STOC = –34 LSBs Self-test has passed. Check valid STOC range in FXLS8964AF data sheet.

3. Set SDCD thresholds.

SDCD_UTHS = Self-test Offset + 'W' LSBs (See Table 27 for ±16 *g* mode value of 'W')

W = min(abs(–52), abs(-19))
= +19

SDCD_UTHS = –11 + 19
= 8

SDCD_UTHS = 8 LSBs

SDCD_LTHS = Self-test Offset – 'W' LSBs
= –11 – 19
= –30

SDCD_LTHS = –30 LSBs

Configure other SDCD parameters as discussed previously in Section 6.3.

4. After SDCD configuration, run self-test with ST_POL = 0. **Motion detection interrupt should be observed**.
5. Run self-test with ST_POL = 1. **Motion detection interrupt should be observed**. This completes SDCD block validation through self-test.

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