AN13900

Adjusting PWM Phase in LPC804 using Programmable Logical Unit

Rev. 0 — 9 May 2023 Application note

Document Information

Information	Content
Keywords	LPC804, PWM wave phase, PLU
Abstract	This application note introduces how to use PLU to adjust a PWM waveform phase and give a demonstration to show the PLU configuration procedure.

1 Introduction

LPC804 has a CTIMER and a Programmable Logical Unit (PLU) module. This application note introduces how to use PLU to adjust a PWM waveform phase and gives a demonstration to show the PLU configuration procedure.

2 PWM waveform phase adjustment requirement

2.1 LPC804 PWM output using CTIMER

LPC804 CTIMER can use two methods to produce the PWM outputs by setup the PWMENx bit in PWMC register.

- Method 1: Use CTIMER match output. In this mode, the External Match Register (EMR) controls PWM output. When a match register equals the Timer Counter (TC), the corresponding match output can either toggle, go LOW, go HIGH, or do nothing.
- Method 2: Each match output can be independently set to perform as PWM output. When a match occurs, the PWM output is set to **HIGH**.

The PWM waveforms produced by these two methods are similar. For simplicity, this application note uses Method 2 to introduce and analyze.

2.2 PWM waveform phase adjustment requirement

To produce PWM output, LPC804 can use a maximum of three single edge controlled PWM outputs. One additional match register determines the PWM cycle length. When a match occurs in any of the other match registers, the PWM output is set to **HIGH**. The timer is reset by the additional match register that is configured to set the PWM cycle length. When the timer is reset to zero, all currently HIGH match outputs configured as PWM outputs are cleared.

The easy understanding wave behavior of PWM output is as shown in Figure 1.

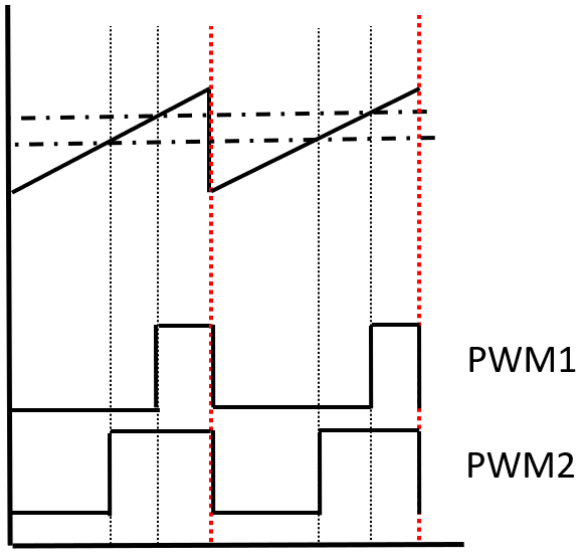

Figure 1. PWM waveform for LPC804

From the PWM output waveform, we can observe this kind PWM output wave has limitation. The limitation is that users can adjust PWM output waveform duty cycle, but cannot adjust its phase. The PWM waveform is always at the end of PWM period.

Applications need adjust PWM duty cycle and its phase. The requirement is as shown in Figure 2.

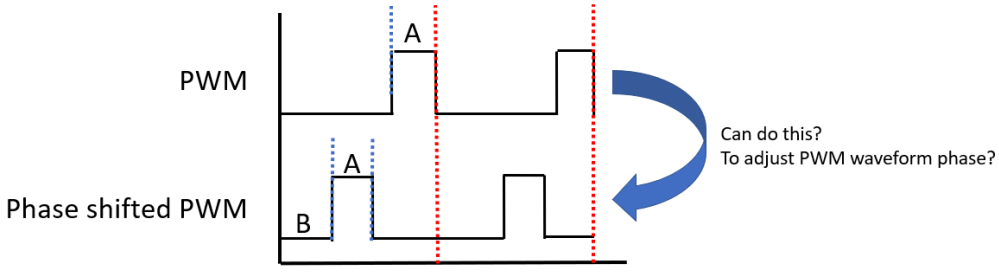

Figure 2. PWM waveform phase adjustment requirement

This application note introduces a method using LPC804 PLU to adjust the PWM waveform phase.

3 LPC804 PLU introduction

LPC804 has a PLU module. The PLU is used to create some logical combinations (such as, AND, OR, NOR) while it does not need the core to interrupt. The logical operation can be programmed using software configuration. NXP provides free tools (PLU Config Tool) to help designer easily implement circuit design and automatically generate the required register setting.

3.1 Look Up Tables (LUTs)

The PLU module has 26 LUTs, which can implement any combinational function of up to five possible inputs.

The inputs include:

- Other LUT outputs
- State FF outputs
- All inputs available from PLU I/O pads

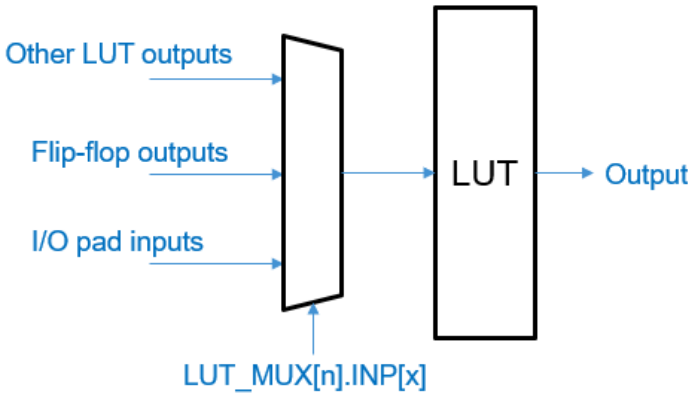

Figure 3. Look Up Tables (LUTs)

Each LUT is programmable using LPC804 registers which implements the logical mapping from five input lines to one output line with the **Logical Truth Value Table**. The output is immediately determined (allowing for propagation delays) by matching the input values of input lines with the entry in the table that matches the input values.

An example of Logic Truth Value Table for a 5-input customized LUT

IDX	IN4	IN3	IN2	IN1	IN0	OUT	IDX	IN4	IN3	IN2	IN1	IN0	OUT
0x0	0	0	0	0	0	0	0x10	1	0	0	0	0	1
0x1	0	0	0	0	1	0	0x11	1	0	0	0	1	1
0x2	0	0	0	1	0	0	0x12	1	0	0	1	0	1
0x3	0	0	0	1	1	0	0x13	1	0	0	1	1	1
0x4	0	0	1	0	0	0	0x14	1	0	1	0	0	1
0x5	0	0	1	0	1	0	0x15	1	0	1	0	1	1
0x6	0	0	1	1	0	0	0x16	1	0	1	1	0	1
0x7	0	0	1	1	1	0	0x17	1	0	1	1	1	1
0x8	0	1	0	0	0	1	0x18	1	1	0	0	0	1
0x9	0	1	0	0	1	1	0x19	1	1	0	0	1	0
0xA	0	1	0	1	0	1	0x1A	1	1	0	1	0	0
0xB	0	1	0	1	1	1	0x1B	1	1	0	1	1	0
0xC	0	1	1	0	0	1	0x1C	1	1	1	0	0	0
0xD	0	1	1	0	1	1	0x1D	1	1	1	0	1	0
0xE	0	1	1	1	0	1	0x1E	1	1	1	1	0	0
0xF	0	1	1	1	1	1	0x1F	1	1	1	1	1	0

Figure 4. An example of Logical Truth Value Table for a 5-input customized LUT

3.2 Multiplexer

Multiplexers in the PLU are used to set up the connections between units and select the right output signals.

The LUT input and output multiplexers for each channel are shown in Figure 5.

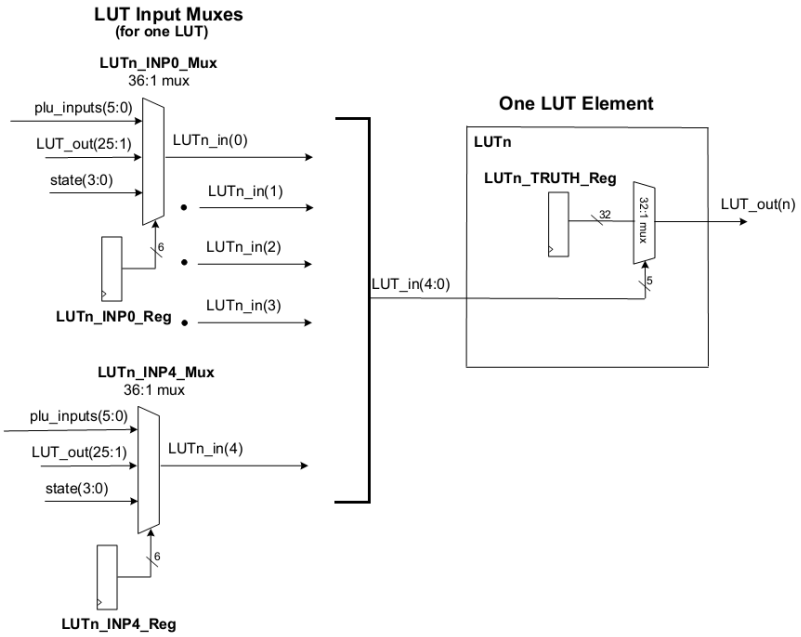

Figure 5. LUT input mux for each channel

PLU output mux for each LUT:

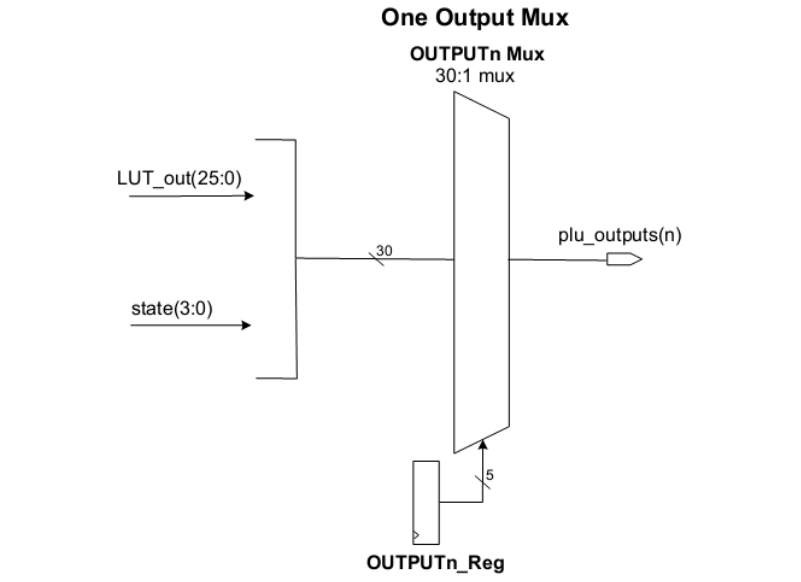

Figure 6. PLU output mux for each LUT

3.3 Steps for using the PLU

The PLU works as a general peripheral. To configure the PLU, use the following steps:

- Enable clocks.
- Assign pins.
- Create a logical network.

3.3.1 Enable clocks

Enable PLU and SWM clock in `SYSCON_SYSAHBCLKCTRLx` register. Toggle the PLU Reset bit in the `SYSCON_PRESETCTRLx` register.

3.3.2 Assign pins

Assign PLU inputs and outputs to specific pins using SWM_PINASSIGNFIXED0. Some pins can be configured as both an input and an output of the PLU. For example, `PIO0_08` can be assigned to `PLU_OUT1` and `PLU_INPUT0`.

3.3.3 Create a logical network

To implement a logical design with the PLU, use the following steps:

- Considering the approach to be used – direct LUT implementation or using primitive logical gates (or a mix of both approaches).
- Programming the customized LUTs (if primitive logical gates are not used).
- Programming the connection of PLU inputs and outputs to LUTs (Primitive logical gates used).

To help developers create a logical design, NXP provides a PLU configuration tool to help user create logical networks easily. This tool can be downloaded for free from NXP official website. This document illustrates how to build a simple design with the PLU Design Tool in the following demo.

4 Using LPC804 PLU to adjust PWM waveform phase

If the application requires PWM0 phase, adjust from B to C as shown in Figure 7.

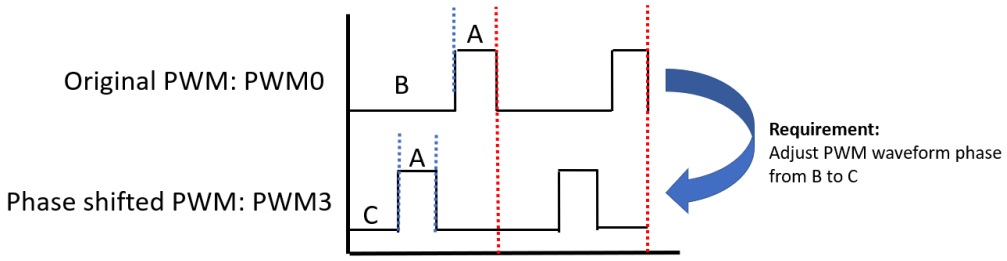

Figure 7. Adjust PWM waveform phase requirement

Then we can use another two PWMs: PWM1 and PWM2. Combine the two PWM waveforms according to some logical relationship, to create a PWM waveform whose phase fits the above requirement.

Figure 8 shows PWM1 and PWM2 waveform.

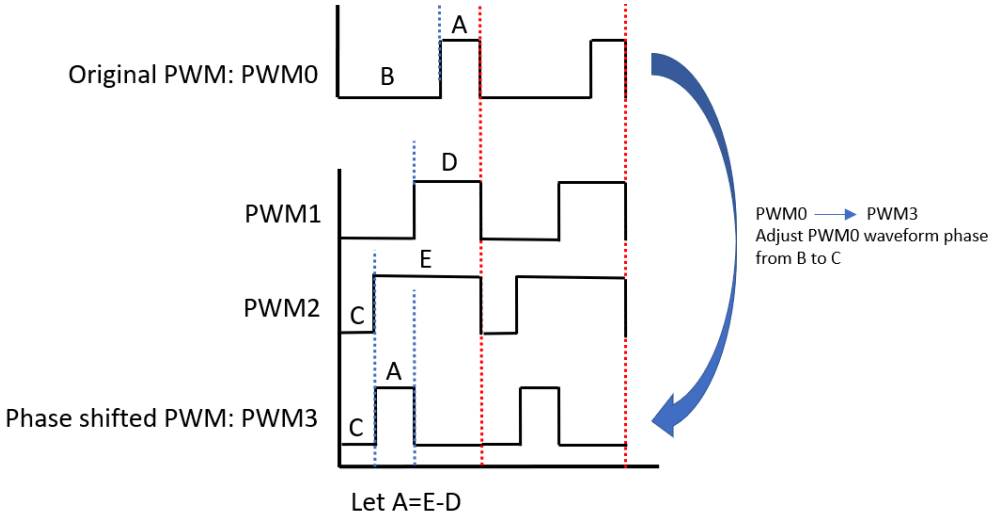

Figure 8. PWM1 and PWM2 waveform

Analyze the PWM1, PWM2, and PWM3, and Figure 9 shows their logical relationship.

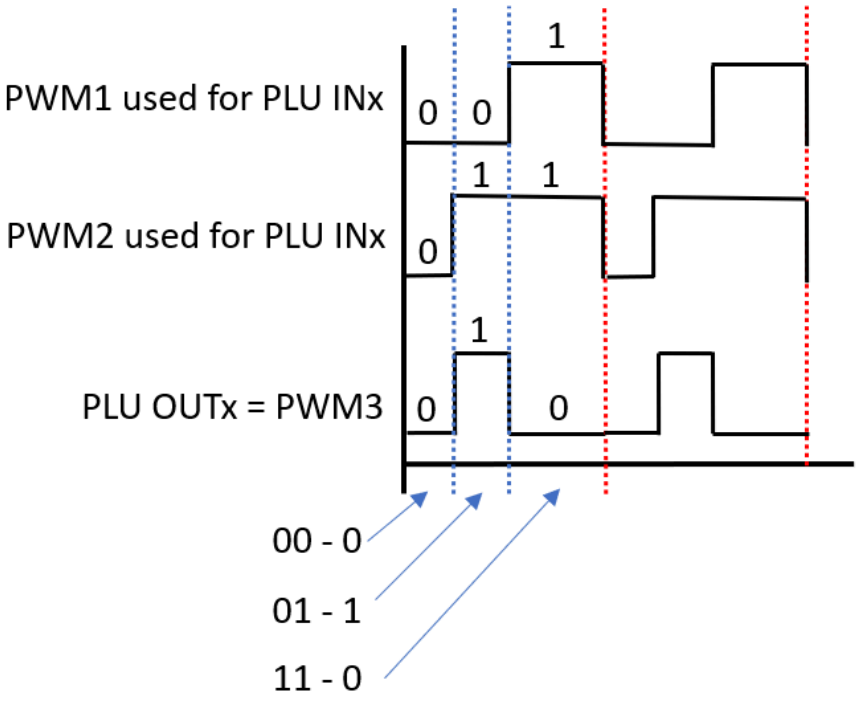

Figure 9. Logical relationship among PWM1, PWM2, and PWM3

PWM1 and PWM2 can be used as PLU inputs, by relative logical combination as shown in Figure 9. The PLU output can get the required PWM3 which adjusts PWM0 waveform phase from B to C.

5 Demonstration

The following demo shows how to adjust a PWM waveform phase by using LPC804 PLU and how to configure the LPC804 PLU step by step to use the PLU configuration tool. An example code is provided together with this application note.

5.1 DEMO environment

5.1.1 Hardware

- LPCXpresso804 evaluation board
- Logical analyzer - Saleae logical pro16 (easier to copy output graph than oscilloscope)
- USB cable
- Host computer

5.1.2 Software

- Provided demo code bases on: SDK_2_12_0_LPCXpresso804
- IDE: MDK5.37
- Demo project: PWM_Phase_Adjust_by_PLU

5.2 Demo description

In this demo, the original PWM is PWM0. To adjust PWM0 phase 144° to get PWM3, see Figure 10.

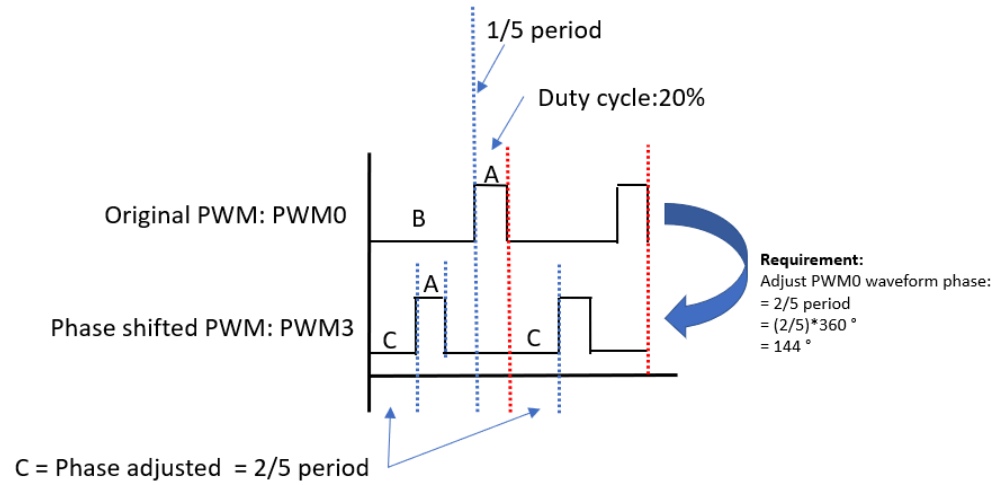

Figure 10. Adjust PWM0 phase 144° to get PWM3

To achieve the result, use PWM1 and PWM2 as shown in Figure 11.

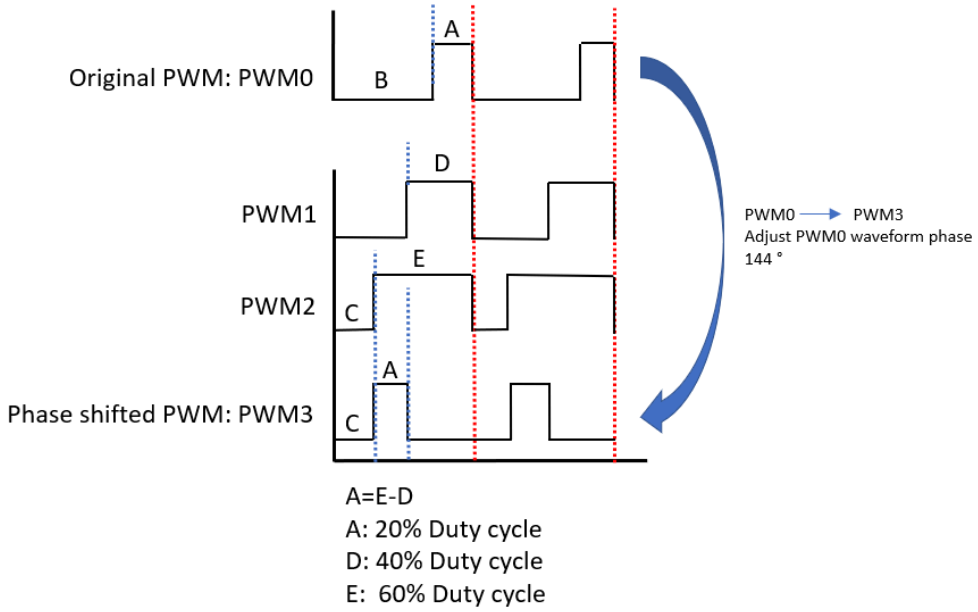

Figure 11. Using PWM1 and PWM2 to adjust the PWM0 phase

5.3 Logical relationship achieved by PLU

In this demo, PWM1 is used as PLU IN4 (P0_12), PWM2 as PLU IN5 (P0_13), and PLU OUT0 (P0_14) to output PWM3. According to analysis in Figure 12, the logical relationship between PLU OUT0 and PLU IN4 and IN5 is XOR.

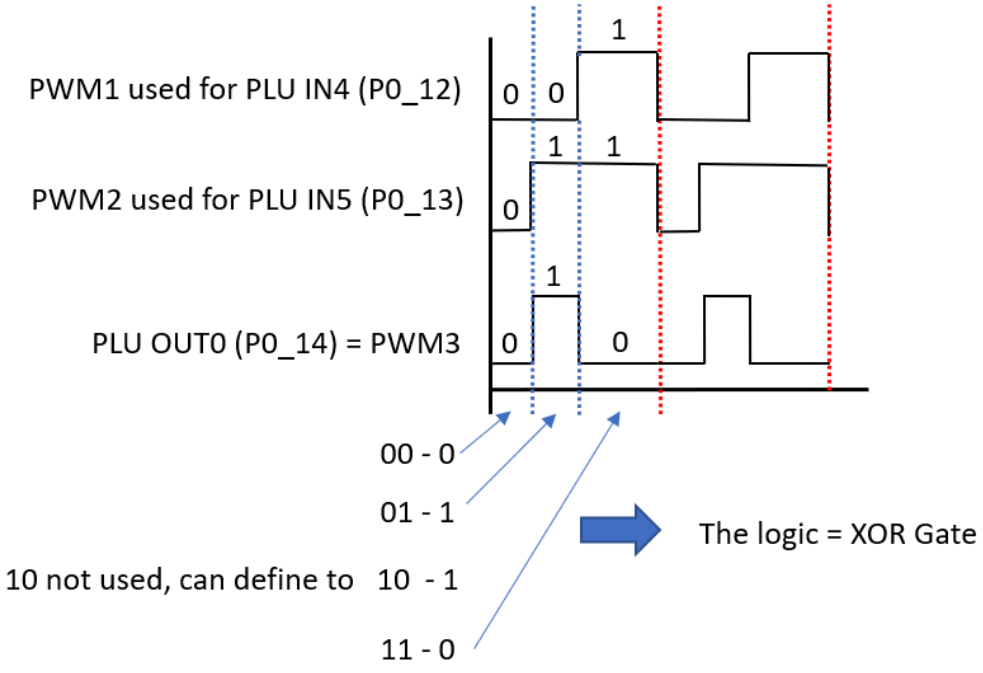

Figure 12. Logical relationship between PLU inputs and outputs

When the logical relationship is determined, we can use PLU LUT to realize this logical relationship. In this demo, we can use PLU LUT to realize an XOR gate to complete the phase adjust function between PWM0 and PWM3.

Figure 13 shows the total function diagram.

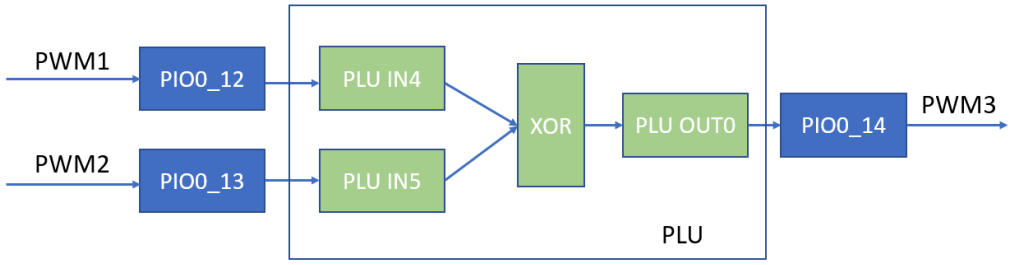

Figure 13. Function diagram

When configuring the PWM output and PLU input on the same pin by Switch Matrix, the two functions are connected internally. Therefore, the board setup is not required for the connection.

5.4 PLU configuration tool usage

In this demo, we use schematic method to define the LUT truth table. By schematic method, the user places inputs, outputs, and logical primitive gates, such as, AND, OR, XOR, connects them, and allows the tool to synthesize the logical network into LUTs.

Following steps illustrate how to use schematic method in PLU configuration tool to configure an XOR Gate which is required to complete the function to adjust the PWM waveform phase.

From MCUXpresso configuration tool V12.1, the PLU config tool is integrated in the MCUXpresso configuration tool and cannot be downloaded from NXP web as a standalone tool.

Open MCUXpresso configuration tool and click the **+** next to **register initialization**. A dialog pops up and you select PLU to enter the PLU Config tool. Choose the schematic design option and open the schematic view. Place needed INPUT1, INPUT2, and OUTPUT1, add logical gates XOR1 in the schematic, then draw the connections between inputs, logical units, and output, as shown in Figure 14.

Note: *The number of gates that can be added is unlimited. Only inputs, outputs, and flip-flops have a restricted quantity.*

When completing the schematic, select **Save** and **Optimize & apply** tabs to complete the PLU configuration.

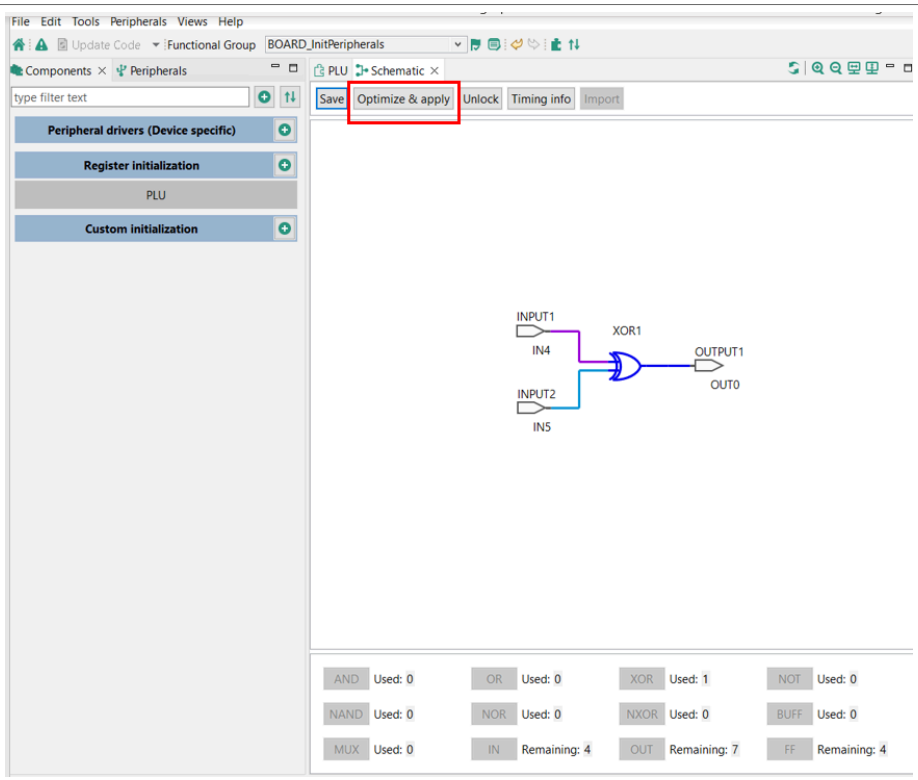

Figure 14. Setup connections between input, LUT, and outputs

Once the optimize operation is completed, click the **Code Preview**, **peripherals.c**, and **peripherals.h** tabs in the right-hand panel of the tool and observe the generated C code. This C code can be used to set up the PLU configuration register for customer own project.

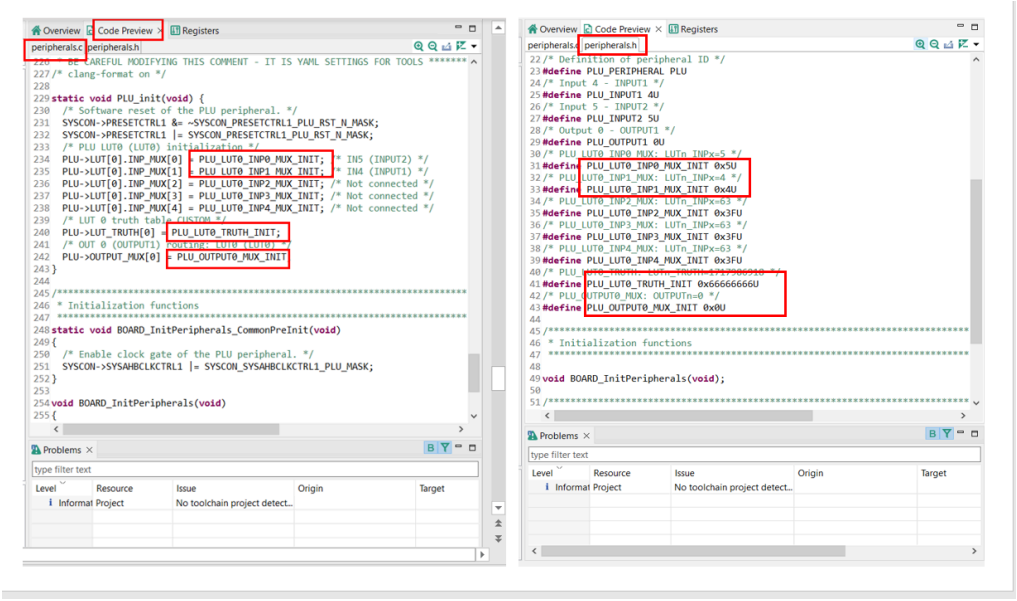

Figure 15. Generate the C code to set up PLU configuration register

5.5 Demo result

Connect Pin P0_12 (PWM1 - PLU IN4), P0_13 (PWM2 - PLU IN5), and P0_14 (PWM3 - PLU OUT0) to an oscilloscope or logical analyzer. Users can observe the relative PWM waveform.

PWM3 waveform phase is adjusted 144° compared with a 20 % duty cycle PWM0 waveform. This PWM0 is not output for display but can be drawn out, as shown in Figure 16.

Figure 16 shows the three observed PWM waveforms from logic analyzer.

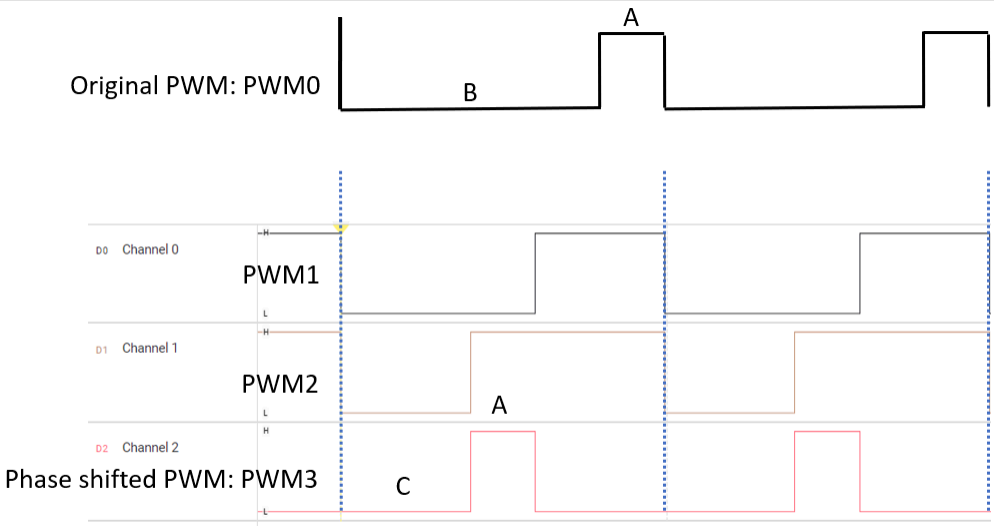

Figure 16. Demo result

6 Revision history

Table 1 summarizes the revisions to this document.

Table 1. Revision history

Revision number	Date	Substantive changes
0	09 May 2023	Initial release

7 Legal information

7.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

7.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Suitability for use in non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. - NXP B.V. is not an operating company and it does not distribute or sell products.

7.3 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Contents

Date of release: 9 May 2023
Document identifier: AN13900