AN2265

Assembly guidelines for land grid array (LGA) package

Rev. 3 — 18 September 2023 **Application note**

Document information

Information	Content
Keywords	land grid array (LGA) package matrix, flip chip land grid array (FCLGA), flip chip interconnect
Abstract	This application note provides guidelines for the handling and assembly of NXP land grid array (LGA), sometimes referred to as laminated quad flat no lead (QFN), packages during printed-circuit board (PCB) assembly.

Revision history

Rev	Date	Description
3	20230918	• Changed remaining references from Freescale to NXP • Added FCLGA • Section 11: updated references • Removed Section 4.2.1
2	6/2019	• Changed all references from Freescale to NXP • Added Section 4.2.3
1	7/2015	Rewrite. Combined AN3311, AN3484, AN2920, and AN3241 with this version.
0	3/2002	initial version

1 Introduction

This application note provides guidelines for the handling and assembly of NXP LGA, sometimes referred to as laminated QFN, packages during PCB assembly. Also included for reference are the following:

- PCB design and rework
- Package performance information, such as moisture sensitivity level (MSL) rating
- Board level reliability
- Mechanical resistance data
- Thermal resistance data

2 Scope

This document contains generic information that encompasses various NXP LGA packages assembled internally or at external subcontractors. Specific information about each device is not provided. When developing a specific solution, experience and development efforts are required to optimize the assembly process and application design. This development process must consider individual device requirements, industry standards (such as IPC and JEDEC), and prevalent practices in the assembly environment. For more details about the specific devices contained in this note, visit http://www.nxp.com or contact the appropriate product application team.

3 LGA package

3.1 Package description

The LGA is a molded area array matrix package. This package can be used in a socket or connected to a board using solder paste. The LGA package is identical in construction to the mold array process ball grid array (MAPBGA) and overmolded ball grid array (BGA), such as the plastic ball grid array (PBGA). However, the BGA spheres are not attached in the LGA package.

The individual units are arranged in a matrix array on a substrate strip, molded together, and then singulated by sawing. Singulated units are distinguished by mold compound completely covering the substrate. An LGA package with lands only at the periphery of the substrate is sometimes referred to as a laminated QFN package.

Figure 1 shows a typical LGA offering from NXP, including examples of a fully populated LGA matrix, and a depopulated LGA matrix. Different sizes and configurations of LGA packages are available. Contact your NXP representative for specific size and LGA matrix configuration requirements.

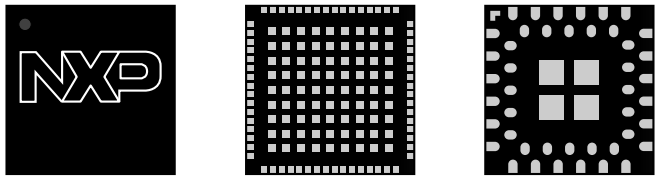


Figure 1. Examples of NXP LGA packages

3.2 Package dimension

NXP offers industry standard LGA sizes and thicknesses with various options of input/output quantity and pitch. Package sizes range from 2 × 2 mm to 27 × 27 mm, with ball pitch ranging from 0.4 mm to 1.27 mm. Refer to NXP package case outline drawings to obtain detailed dimensions and tolerances. Package size and ball pitch are updated as new products are introduced. Check with the NXP sales team for more information.

3.3 Package cross-section

The cross-section drawing in Figure 2 is included to show the representative internal layers of a typical LGA package with a 2-layer substrate. The term 2-layer substrate refers to the 2 conductive metal layers used to redistribute the I/O within the substrate. Standard configuration for an LGA typically uses 2-layer substrates. High-performance products may use 4-layer substrates.

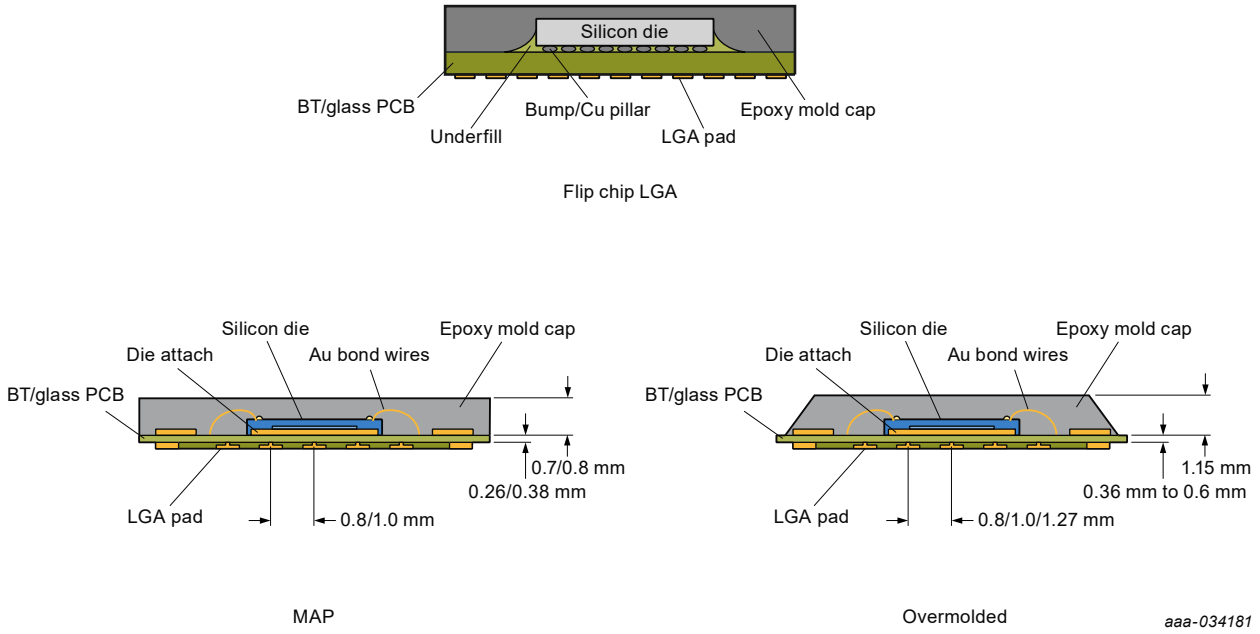


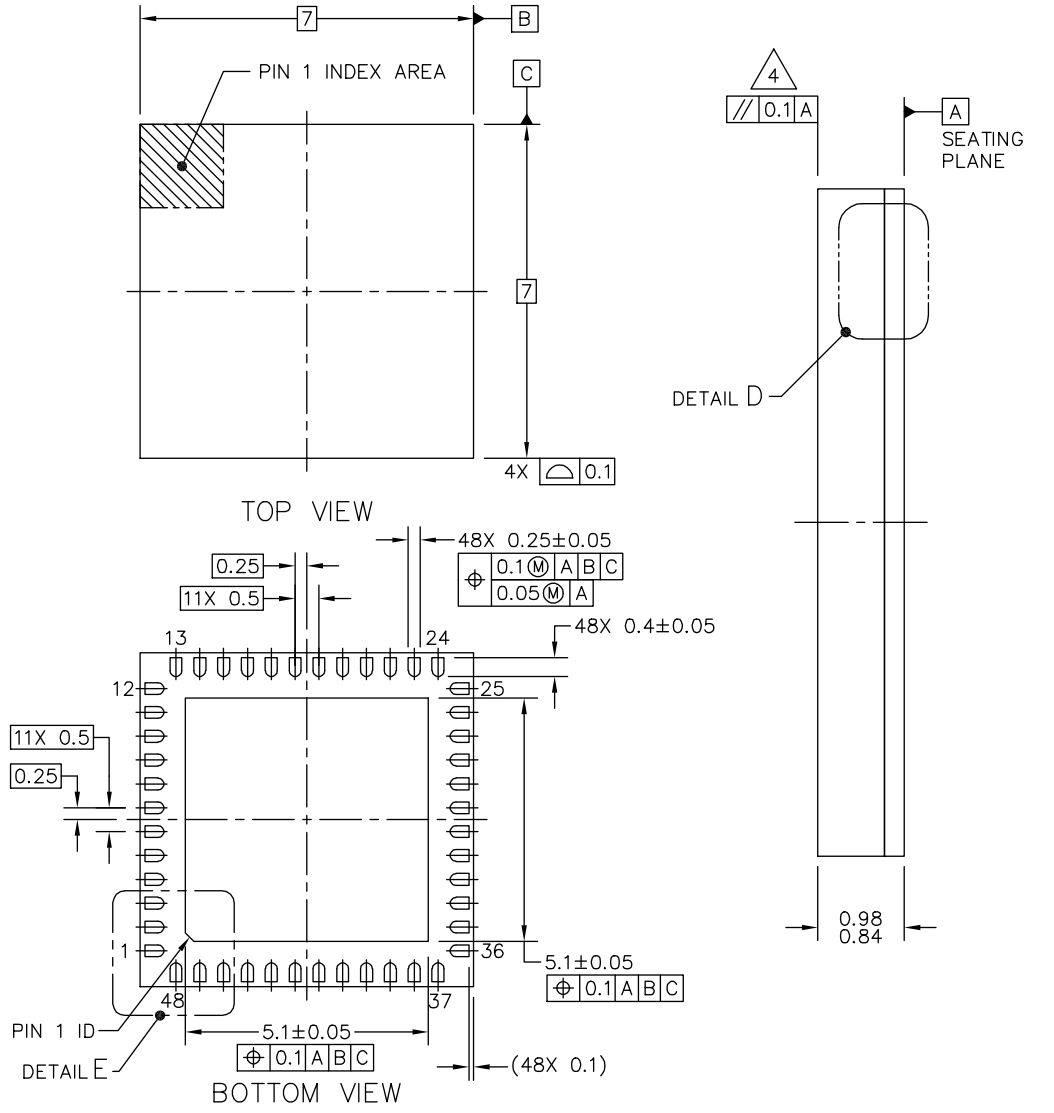
Figure 2. LGA cross-section with 2-layer substrate configuration

4 PCB guidelines

4.1 PCB design guidelines

Proper PCB footprint and stencil designs are critical to ensure high surface-mount-assembly yields, and electrical and mechanical performance. The design starts with obtaining the correct package drawing. Package case outline drawings are available at www.nxp.com.

Follow the procedures in Section 9.1 "Downloading the information from NXP". Usually, PCB designs for BGA can be used for LGA without any modification. Some LGA footprints are similar to a QFN package. See the QFN package application note (AN1902) for more details. Figure 3 shows an example of a 7 × 7 mm, 48-lead mold array process land grid array (MAPLGA) case outline drawing. The goal is a well-soldered MAPLGA as shown in Figure 4.



TITLE: MAPLGA, THIN PROFILE, FINE PITCH, 48 I/O, 7 X 7 PKG, 0.5 MM PITCH (LAMINATE QFN)	DOCUMENT NO: 98ASA00212D REV: A
	STANDARD: NON–JEDEC
	SOT1549–1

Figure 3. 7 x 7 mm 48-lead MAPLGA case outline

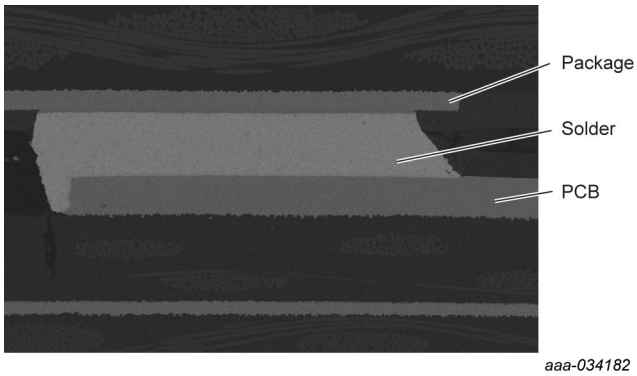


Figure 4. Scanning electron microscope (SEM) image of a well-soldered MAPLGA solder joint

4.2 PCB pad design

NXP follows the generic requirements for surface mount design and land pattern standards from the institute for printed circuits (IPC), IPC-7351B. This document and an accompanying land pattern calculator can be purchased from the website of IPC http://ipc.org/. The document includes guidelines for BGAs, based on assumed package dimensions.

Many LGA products do not have fully populated arrays. This design allows a better PCB routing. PCB design must ensure that the final footprint matches the part.

4.2.1 Pad surface finishes

Almost all PCB finishes are compatible with LGAs including hot air solder leveling (HASL), organic solderability preservatives (OSP), electroless nickel immersion gold (ENIG), immersion Sn, and immersion Ag. NXP suggests the PCB surface finish shelf life be monitored to ensure the life has not expired. Surfaces should always be free of dirt and other contaminants before PCB assembly.

4.2.2 Segmented exposed pad land pattern design

Alternatively, the land pattern for the exposed pad can be segmented into a symmetric array of square or rectangular lands, as shown in Figure 5. This design also applies to packages with multiple exposed pads. The land array can be created either by segmentation of a full copper area by solder mask openings or by non-solder mask defined (NSMD) copper lands.

- Recommended edge length/width of a matrix land is between 1.0 mm to 2.0 mm
- Distance between the lands should be 0.40 mm

The segmented PCB design facilitates the solder paste flux outgassing during reflow, thereby promoting a lower voiding level of the completed solder joint. The maximum size of a single solder void is limited by the dimensions of a single matrix segment at the same time.

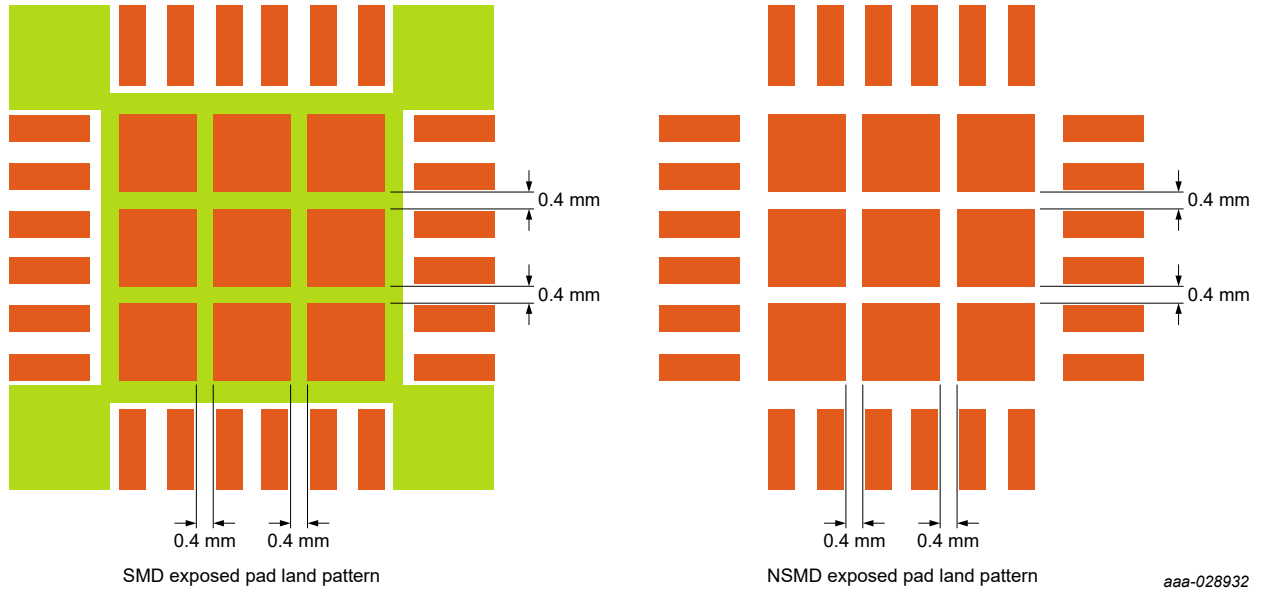


Figure 5. Segmented exposed pad land patterns

4.2.3 Solder mask layer

NXP encourages customers to use NSMD PCB pad designs. These designs typically provide better thermal fatigue life. Some field use conditions require the use of solder mask defined (SMD) pads for better drop/shock survivability. The difference between NSMD and SMD is shown in Figure 6.

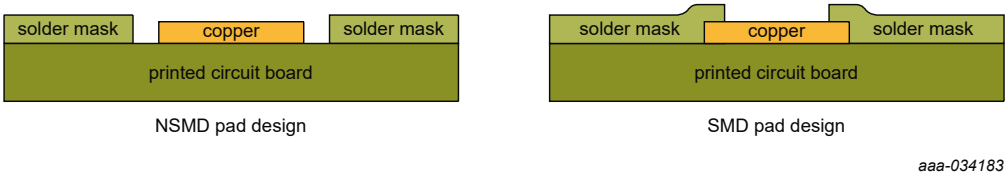


Figure 6. NSMD and SMD pad designs

5 Board assembly

5.1 Assembly process flow

A typical surface mount technology (SMT) process flow is shown in Figure 7.

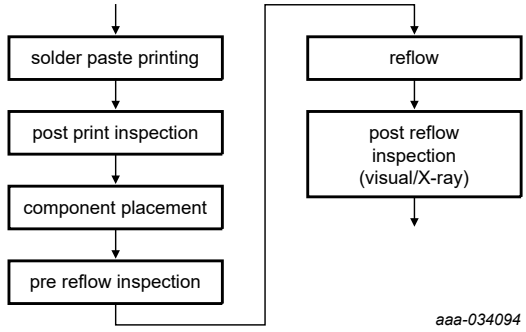


Figure 7. SMT process flow

5.2 Solder stencil and solder paste

5.2.1 Stencil thickness

Solder paste stencil design is critical for good solder joint formation, especially as the LGA pitch decreases. The thickness of the stencil determines the amount of solder paste deposited onto the printed-circuit board land pattern.

For 1.0 mm pitch parts, a common stencil thickness is 0.125 mm (5.0 mils), while 0.100 mm thick stencils (4.0 mils) are also used. In high reliability applications, 0.150 mm (6.0 mils) thick stencils are preferred. For 0.80 mm pitch, the 0.100 mm thick stencil is common.

For these stencils, well cut openings created with a laser or by chemical etch is preferred. The opening walls should be polished and an Ni finish is recommended. The goal is to have a stencil that properly releases a consistent volume of solder paste, print after print.

The stencils for BGA pitches at or below 0.65 mm require other factors to be considered, as well. Usually on a PCB, there may be other small size and small pitch components that prevent the stencil opening size to be reduced. Instead, the total stencil thickness is decreased. Typically, stencils are from 0.075 mm to 0.125 mm thick.

At smaller pitches, it may help to use square openings in place of round, as shown in Figure 8. The square openings allow a slightly larger volume of solder paste to be released. Generally, the opening length or diameter is 1 : 1, with the solderable PCB diameter. For additional solder paste volume, the opening length or diameter can be increased.

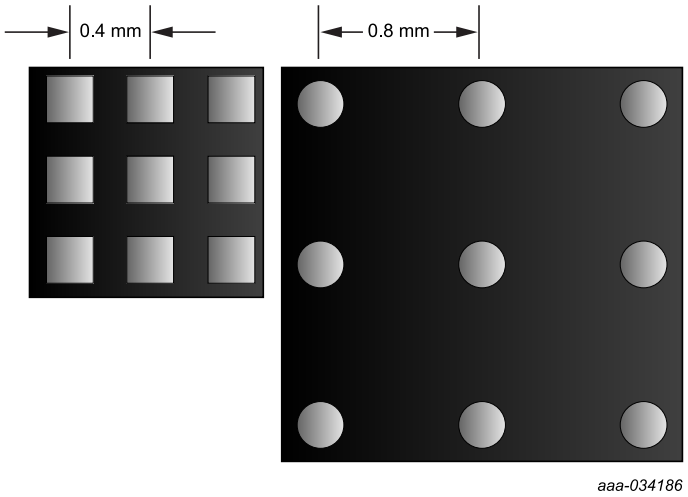


Figure 8. Square 0.4 mm and round 0.8 mm pitch stencil openings

Small pitch stencils frequently have specialized coatings to help with paste release. These coatings, frequently called nano-coatings, eventually wear out. A monitoring program for stencil age (number of prints) may be needed.

5.2.2 Solder paste properties

Solder paste is one of the most important materials in the SMT assembly process. It is a homogenous mixture of metal alloy, flux, and viscosity modifiers. The metal alloy particles are made in a specific size and shape. Flux has a direct effect on soldering and cleaning, and it is used to precondition the surfaces for soldering (by removing minor surface contamination and oxidation).

There are two different flux systems commonly available:

- The first type of flux system requires cleaning, such as standard rosin chemistries and water-soluble chemistries. Standard rosin chemistries are normally cleaned with solvents, semi-aqueous solutions, or aqueous/saponifier solutions, while the water-soluble chemistries are cleaned with pure water.
- The second type of flux system type requires no cleaning, but normally a little residue remains on the PCB after soldering.

Solder paste grain size can be useful to manipulate by pitch. For larger pitch parts, 0.80 mm and larger, Type 3 solder powder (25 micron grain size to 45 micron grain size) is widely used. At pitches that are 0.65 mm and smaller, Type 4 solder powder (20 micron grain size to 38 micron grain size) might provide a better solder joint.

5.3 Component placement

The high lead interconnection and insertion density require precise and accurate placement tools. To meet this requirement, the placement machine should be equipped with optical recognition systems, such as a vision system. These systems are used for the centering of the PCB and handling the components during the pick and place motion. A placement accuracy study is recommended. NXP follows the EIA-481-F standard for tape-and-reel orientation as shown in Figure 9. Also see Section 10.3 "Packing of devices" for additional details.

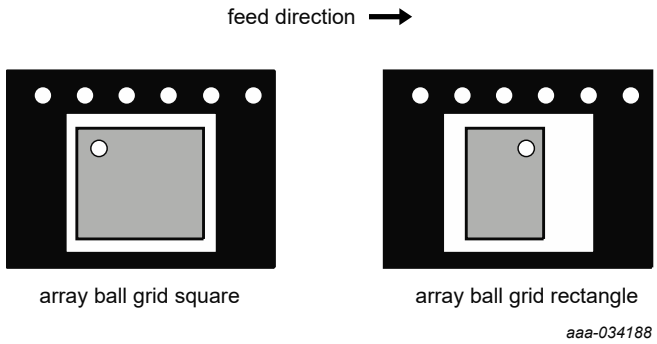


Figure 9. LGA orientation in tape-and-reel

5.4 Soldering

A typical temperature profile band is shown in Figure 10. The actual profile parameters depend upon the solder paste used. Recommendations from paste manufacturers should be followed. Temperature profile is the most important control in reflow soldering and it must be fine-tuned to establish a robust process. Usually, thermocouples should be placed under the heaviest thermal mass device on the PCB, to monitor the reflow profile. Generally, when the heaviest thermal mass device reaches reflow temperatures, all other components on the PCB reach reflow temperatures as well.

Dry air is a common reflow furnace atmosphere. Nitrogen reflow is recommended to improve solderability and to reduce defects, such as solder balling. It is also recommended to monitor the temperature profile of package top surfaces to validate that the package peak temperature does not exceed the MSL classification of individual devices.

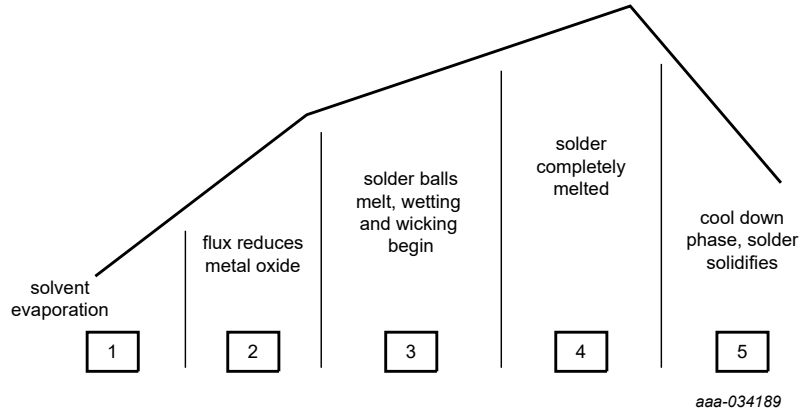


Figure 10. General solder reflow phases

The solder paste must be considered for the reflow profile for all devices on the PCB. Every paste has a flux, and the flux dominates the reflow profile for steps such as soak time, soak temperature, and ramp rates. Peak reflow temperature is the melting temperature of the metals in the paste, plus an extra percent to ensure all solder paste on the PCB reflows.

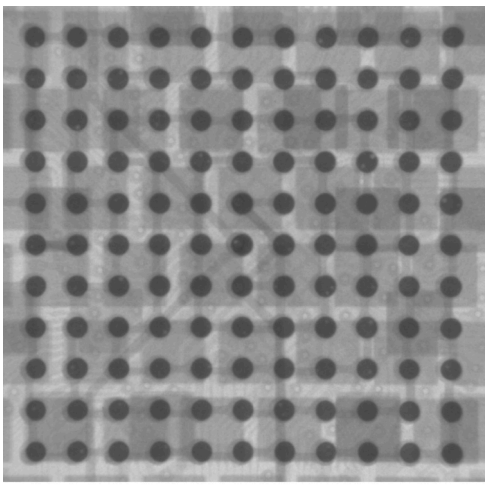
Deviation from the reflow profile recommended by the paste manufacturer should be evaluated first using a copper (Cu) coupon test. The horizontal size for a typical solder paste volume is measured as either a diameter or as X and Y lengths. The Cu coupon is then reflowed and the solder paste volume is measured for either diameter or X and Y. The goal is to have a reflow profile with the most horizontal spread. For best results, the Cu coupon should be lightly sanded before use, to remove Cu-oxide build up. The PCB should be rated for

multiple reflows of MSL classification. Cross-referencing with the device data sheet is recommended for any additional board assembly guidelines specific to the exact device used.

NXP provides an application note AN3300, general soldering temperature process guidelines at http://www.nxp.com. This application note has general comments on reflow profiles. It is a useful starting point.

5.5 Inspection

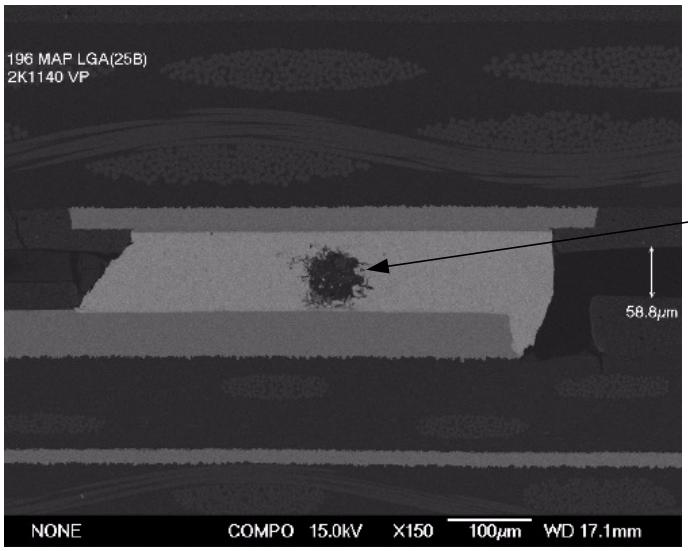
The solder joints of LGA parts are formed underneath the package. To verify any open or short-circuits (bridging) after reflow, non-destructive vision/optical inspection and x-ray inspection are recommended. Micro-sectioning is another method of inspecting solder joint quality during process optimizations. However, micro-sectioning is less suitable to production inspection, due to slow processing. Figure 11 shows the expected x-ray image of a soldered component.



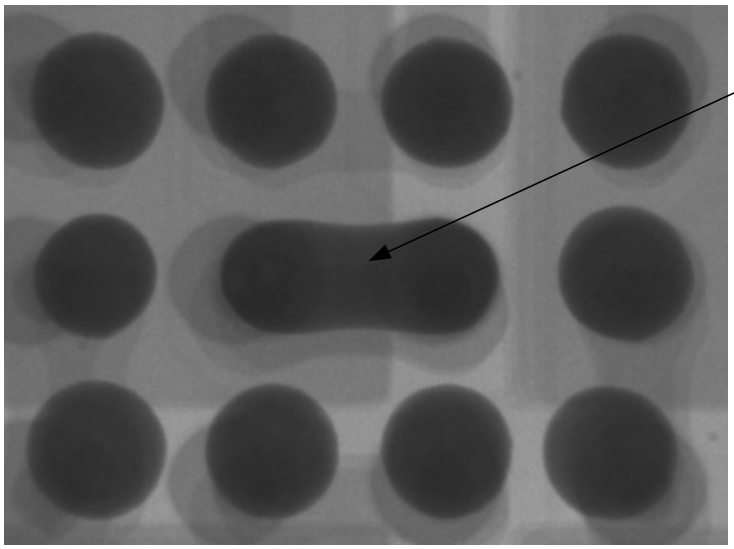
aaa-034191

Figure 11. Inspection x-ray of an LGA package

5.6 Common LGA solder joint defects



aaa-034192



aaa-034193

Figure 12. Two common LGA solder joint defects

5.7 Additional precautions

The following precautions must be observed with sensor products.

- To fix the PCB into an enclosure, avoid screwing down the PCB near the accelerometer sensor. Doing so can cause the PCB to bend.
- Avoid using HASL, which can cause uneven surface issues.
- Avoid washing the boards for pressure sensor parts, because these packages have a hole in the lid.

6 Repair and rework procedure

6.1 Repairing

Repairing a single solder joint of an LGA component is not recommended, because the joint is underneath the package.

6.2 Reworking

If a defective component is observed after board assembly, the device can be removed and replaced with a new one. This rework can be performed using the heating methods described in this section.

When performing the rework:

- The influence of the heat on adjacent packages must be minimized. Do not exceed the temperature rating of the adjacent packages.
- Heating conditions differ due to contrasting heat capacities of the PCB (board thickness, number of layers) and mounted components used. Therefore, the conditions must be set to correspond to the actual product and its mounted components.
- NXP follows industry standard component-level qualification requirements, which include three solder reflow passes. The three reflow passes simulate board level attach to a double-sided board and includes one rework pass. The removed package should be properly disposed of so it does not mix in with any new components.

A typical package rework flow process is:

1. Tooling preparation
2. Package removal
3. Site redressing
4. Solder paste printing
5. Remount package
6. Reflow soldering

Note: *NXP product quality guarantee/warranty does not apply to products that have been removed. Therefore, component reuse should be avoided.*

In any rework, the PCB is heated. The thermal limits of PCB and components (for example, MSL information) must be followed. During heating, the combination of rapid moisture expansion, material mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the components and PCB. To prevent moisture-induced failures, it is recommended that the PCBs and components have strict storage control with a controlled environment, such as dry air or nitrogen. In addition, a prebake (for example, 125 °C for 24 hours for boards with SMT components or 95 °C for 24 hours for boards with temperature sensitive components) is recommended to remove moisture from components and PCB prior to removal of the package, if the maximum storage timeout of the dry pack (see label on packing material) is exceeded after board assembly.

Individual process steps for reworking a package are explained in Section 6.2.1 to Section 6.2.6.

6.2.1 Tooling preparation

Various rework systems are available. In general, the rework station should have a split light system, an XY table for alignment, and a hot air system with a top and bottom heater for component removal. For processing LGA packages, a system should meet the following requirements:

- **Heating:** Controlled hot air transfer (temperature and air flow) to both the LGA package and its mounted PCB is strongly recommended. The heating must be appropriate for the correct package size and thermal mass. PCB preheating from beneath is recommended. Infrared heating can be applied, especially for preheating the PCB from the underside, but it should only augment the hot air flow from the upper side. Nitrogen can be used instead of air. Additional information can be found in Section 6.2.2 "Package removal".
- **Vision system:** The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of the package to the PCB, a split light system should be implemented. Microscope magnification and resolution should be appropriate for the pitch of the device.
- **Moving and additional tools:** Placement equipment should have good accuracy. In addition, special vacuum tools may be required to remove solder residue from PCB pads.

6.2.2 Package removal

No further defects must be introduced to the device during removal of the component from the PCB if it is suspected to be defective and intended to be returned. These defects could interfere with subsequent failure analysis. The following recommendations are intended to reduce the chances of damaging a component during removal:

- **Moisture removal:** Dry bake components at the following settings before removal
  - Boards with SMT components, 125 °C for 16 to 24 hours
  - Boards with temperature sensitive components, 95 °C for 16 to 24 hours
- **Temperature profile:** During desoldering, ensure that the package peak temperature is not higher and temperature ramps are not steeper than the standard assembly reflow process.
- **Mechanics:** Do not apply high mechanical forces for removal. High force can damage the component and/or the PCB, which may limit failure analysis of the package. For large packages, vacuum wands can be used (implemented on most rework systems); for small packages, tweezers may be more practical.

If suspected components are fragile, it is especially necessary to determine if they can be electrically tested directly after desoldering, or if these components have to be preconditioned prior to testing. In this case, or if safe removal of the suspected component is not possible or too risky, the whole PCB or the part of the PCB containing the defective component should be returned.

To remove the faulty component from the board, apply hot air from the top and bottom heaters. Use an air nozzle of the correct size to conduct the heat to the LGA package such that a vacuum pickup tool can properly remove the component. The temperature setting for the top heater and the bottom heater depends on the component rating. Many assembly sites have extensive in-house with experts regarding rework. These experts should be consulted for further guidance.

If the PCB is large, it is important to avoid bending of the printed circuit material due to thermal stress. A bending prevention tool must be placed on the bottom of the printed-circuit board. In addition, a bottom heater should be installed to allow heating of the entire printed-circuit board, to raise work efficiency.

6.2.3 Site redressing

After the component is removed, the PCB pads must be cleaned to remove solder residue in preparation for the new component placement. Solder sucker, solder wick braid, and so on, complete this vacuum desoldering after applying flux. Remaining solder residue and projections cause the solder stencil not closely to adhere to the PCB during solder paste printing, leading to improper solder paste supply during component mount.

Moreover, when the solder residue flows all the way to an adjacent through-hole, the solder paste printed on the pad can be transferred, via suction, to the through-hole during reflow, which may cause improper connection. A solvent may be necessary to clean the PCB of flux residue. A desoldering station can be used for solder dressing. The applied temperature must not exceed 245 °C, which can contribute to PCB pad peeling from the PCB. This manual operation is typically a manual operation, which is directly attributed to experience and skill.

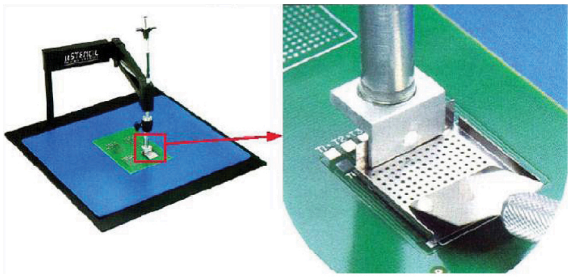
Non-abrasive or soft bristle brushes should be used. Abrasive brushes, such as steel brushes, can contribute to bad solder joints. Prior to placing a new component on the site, solder paste should be applied to each PCB pad by printing or dispensing. A no-clean solder paste is recommended.

6.2.4 Solder paste printing

Solder supply during rework is done using specialized templates and tools. A mini stencil with the same stencil thickness, aperture opening, and pattern as the normal stencil, is placed in the component site. A mini metal squeegee blade deposits solder paste in the specific area. See Figure 13. The printed pad should be inspected to ensure even and sufficient solder paste before component placement.

In situations where neighboring parts are near to the LGA components, and the mini-stencil method is not an option, apply solder paste carefully on each pad using a paste dispensing system. The volume of solder paste must be controlled to prevent shorting on the component and/or neighboring components.

Depending upon allowed customer reliability standards, a flux only application to either the replacement part or to the reworked PCB may be sufficient for joining an LGA part to the board. Flux choice is critical and should be of the same standards as for the original PCB assembly.



(photos courtesy of OK Industries)

aaa-034105

Figure 13. Mini stencil and mini squeegee

6.2.5 Package remount

After preparing the site, the new package can be placed onto the PCB. Handling of the replacement package should also follow the guidelines of Section 9.2 "Moisture sensitivity level". When remounting the package, it is recommended to use rework equipment having good optical or video vision capability. A split light system displays images of both package balls and PCB pads by superimposing the two images. Alignment of the balls and pads is completed by adjusting the XY table.

A regular array LGA exhibits self-alignment in any direction including x-axis shift, y-axis shift, and rotational misplacement. Therefore, perfect placement is not required. At least 50 % on solder ball on PCB pad for all pads is the minimum goal for part placement accuracy.

6.2.6 Reflow soldering

The new component is soldered to the PCB using the same temperature profile as the normal reflow soldering process, shown in Section 5.4 "Soldering". Reflow furnaces are not typically used for rework. Rather, a dedicated rework station is used for part removal and new part joining. During soldering, the package peak temperature and temperature ramps cannot exceed those temperatures of the standard assembly reflow process.

In infrared (IR) or convection processes, the temperature can vary greatly across the PCB depending on the furnace type, size, and mass of components, and the location of components on the assembly. Additionally, rework stations only apply heat locally, not to the entire PCB. If nozzles are used to direct the heat, the nozzle

size must be sufficiently large to encompass the entire part. Profiles must be carefully tested to determine the hottest and coolest points on the assembly. The hottest and coolest points should fall within recommended temperatures in the reflow profile. To monitor the process, thermocouples must be carefully attached with very small amounts of thermally conductive grease or epoxy directly to the solder joint interface between the package and board.

The materials used in rework have a higher potential to create conductive traces, corrosion, and so on, compared to standard materials. Residual solder and flux must be removed from the soldering lands and cleaned with a solvent. The solvent is specific to the type of paste used in the original assembly. Follow the solder paste recommendations of the manufacturer. Use low-residue and no-clean solder paste for soldering.

7 Board level reliability

7.1 Testing details

Solder joint reliability (SJR) testing is performed to determine a measure of board level reliability when exposed to thermal cycling. There are several different names for board level reliability (BLR) customers may see. These BLRs include: second-level reliability, SJR, and temperature cycling on board (TCoB).

The information provided here is based on experiments executed on MAPLGA devices using a daisy chain configuration. Actual surface mount process and design optimizations are recommended to develop an application-specific solution.

- For Automotive-grade product applications, the widely accepted temperature range for testing is –40 °C to +125 °C.
- Consumer SJR temperature cycling conditions may vary widely, depending on the application and specific user. Typically, NXP consumer SJR testing is performed from 0 °C to 100 °C.

The preferred test method varies by market and industry. For automotive, the primary test is a version of IPC-9701A, air temperature cycling. For the consumer market, drop test of JEDEC is the primary test (JESD22-B111). Telecommunications uses both IPC-9701A and IPC-9702 (monotonic bend). NXP may not test an electronic package at all and may not have all the tests for each market and industry.

Table 1 shows the NXP standard test set-up for performing automotive board level solder joint reliability testing. For consumer markets, the board stack-up found in JESD22-B111 is commonly used, 8 Cu layers, and 1.0 mm total thickness. Telecommunications market parts use IPC-9701A/9702 stack-ups of 8 Cu layers and 2.25 mm total thickness.

Table 1. Board level reliability testing: material and test setup

Printed-circuit board	• 1.58 mm thickness • Four Cu layers • OSP surface finish
Test board assembly	• Pb-free solder paste SAC387 • Reflow peak temperature for SnAgCu (SAC) assembly ~ 240 °C • Pb solder paste Sn63Pb37 • Reflow peak temperature for SnPb assembly ~ 220 °C • 0.100 mm thickness, Ni plated, laser cut and electro-polished stainless steel stencil

Table 1. Board level reliability testing: material and test setup*...continued*

Cycling conditions	• Continuous in-situ daisy chain monitoring per IPC-9701A and IPC-SM-785 • Air temperature cycling (ATC) for automotive – –40 °C to +125 °C – 15 minute ramp and 15 minute dwell – 1.0 hour cycle time • ATC for commercial and industrial – 0 °C to 100 °C – 10 minute ramp and 10 minute dwell – 40 minute cycle time
Package test vehicle	• Production BOM package including die (die mechanically present, without wire bond connection) • Daisy chain in the LGA pattern connecting pairs of solder balls

7.2 Solder joint reliability results

NXP experimentally gathers board-level reliability data for various packages. To get results from these experiments, including Weibull plots, contact the NXP sales team. Customers should interpret the NXP solder joint reliability data to see how well they meet the final application requirements.

8 Thermal characteristics

8.1 General thermal performance

Because the thermal performance of the package in the final application depends on a number of factors, such as board design, power dissipation of other components on the same board, ambient temperature, the thermal package properties provided by NXP should serve only as a guideline for the thermal application design. In applications where the thermal performance is considered to be critical, NXP recommends running application-specific thermal calculations in the design phase to confirm the onboard thermal performance.

8.2 Package thermal characteristics

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

Additional factors to consider in PCB design and thermal rating of the final application include:

- Thermal resistance of the PCB
  - Thermal conductivity of PCB traces
  - Number of thermal vias
  - Thermal conductivity of thermal vias
- Quality and size of PCB solder joints
  - Effective PCB pad size
  - Potential solder voiding in the thermal path solder joints, which may reduce the effective solder area

The thermal characteristics of the package provide the thermal performance of the package when there are no nearby components dissipating significant amounts of heat. The stated values are meant to define the package thermal performance in a standardized environment.

Thermal properties of the individual products are given in the NXP product data sheets as appropriate. Product data sheets are available within http://www.nxp.com. Additional thermal properties may be available upon request.

8.3 Definition of package thermal properties

The definition of thermal properties, $R_{\theta JA}$, $R_{\theta JMA}$, $R_{\theta JB}$, $R_{\theta JC}$, and ψ_{JT} (in °C/W) specifies the thermal performance of an LGA package. Physical measurements and running complex simulation models perform thermal characterization under the following conditions.

- Two thermal board types:
  - Single layer board (1s) per JEDEC JESD51-3 and JESD51-5 (exposed pad packages only)
  - Four layer board (2s2p) per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only)
- Four boundary conditions:
  - Natural convection (still air) per JEDEC JESD51-2
  - Forced convection per JEDEC JESD51-6
  - Thermal test board on ring style cold plate method per JEDEC JESD51-8
  - Cold plate method per MIL SPEC-883 method 1012.1

8.3.1 $R_{\theta JA}$: theta junction-to-ambient natural convection (still air)

Junction-to-ambient thermal resistance (theta-JA or $R_{\theta JA}$ per JEDEC JESD51-2) is a one-dimensional value measuring the conduction of heat from the junction (hottest temperature on die) to the environment (ambient) near the package in still air environment. The heat generated on the die surface reaches the immediate environment along two paths:

- Convection and radiation of the exposed surface of the package
- Conduction into and through the test board followed by convection and radiation of the exposed board surfaces

8.3.2 $R_{\theta JMA}$: theta junction-to-moving-air forced convection

Junction-to-moving-air (theta-JMA or $R_{\theta JMA}$ per JEDEC JESD51-6) is similar to $R_{\theta JA}$, but it measures the thermal performance of the package mounted on the specified thermal test board exposed to a moving air (at 200 feet/minute) environment.

8.3.3 $R_{\theta JB}$: theta junction-to-board

Junction-to-board thermal resistance (theta-JB or $R_{\theta JB}$ per JEDEC JESD51-8) measures the horizontal spreading of heat between the junction and the board. The board temperature is measured on the top surface of the board near the package. The measurement uses a highly effective thermally conductive four layer test board (2s2p) per JEDEC JESD51-7. $R_{\theta JB}$ is frequently used by customers to create thermal models considering both package and application board thermal properties.

8.3.4 $R_{\theta JC}$: theta junction-to-case

Junction-to-case thermal resistance (theta-JC or $R_{\theta JC}$ per MIL SPEC-883 method 1012.1) indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method per MIL SPEC-883 method 1012.1, with the cold plate temperature used for the case temperature. $R_{\theta JC}$ can be used to estimate the thermal performance of a package when the board is adhered to a metal housing or heat sink, or when a complete thermal analysis is done.

8.3.5 ψ_{JT}: psi junction-to-package top

Junction-to-package top (psi JT or ψ_{JT}) indicates the temperature difference between package top and the junction temperature, optionally measured in still air condition (per JEDEC JESD51-2) or forced convection environment (per JEDEC JESD51-6). Do not confuse ψ_{JT} with the parameter $R_{\theta JC}$. $R_{\theta JC}$ is the thermal

resistance from the device junction to the external surface of the package, with the package surface held at a constant temperature, while ψ_{JT} is the value of the temperature difference between package surface and junction temperature, usually in natural convection.

8.4 Example of package thermal properties

An example of the thermal characteristics as typically shown in the NXP product data sheet is shown in Table 2. The example applies to a package size 17 × 17 × 1.5 mm (max), pitch 0.8 mm, 364 I/O, die size ~ 4.9 mm × 5.9 mm (NXP case outline drawing SOT1517-1).

Table 2. Thermal resistance example

Parameter	Conditions	Symbol	Without heatsink (HS), 0.7 mold	With HS, 0.7 mold	Without HS, 0.8 mold	With HS, 0.8 mold	Unit	Notes
Junction to ambient, natural convection	single layer board (1s)	$R_{\theta JA}$	45	37	45	37	°C/W	[1] [2]
Junction to ambient, natural convection	four layer board (2s2p)	$R_{\theta JA}$	28	22	28	23	°C/W	[1] [2] [3]
Junction to ambient (at 200 ft/min)	single layer board (1s)	$R_{\theta JMA}$	37	29	37	30	°C/W	[1] [3]
Junction to ambient (at 200 ft/min)	four layer board (2s2p)	$R_{\theta JMA}$	24	19	24	19	°C/W	[1] [3]
Junction to board		$R_{\theta JB}$	17	11	17	12	°C/W	[4]
Junction to case		$R_{\theta JC}$	8.0	8.0	10	9.0	°C/W	[5]
Junction to package top	natural convection	ψ_{JT}	2.0	7.0	2.0	8.0	°C/W	[6]

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[2] Per JEDEC JESD51-2 with the single layer board horizontal board meets JESD51-9 specification.
[3] Per JEDEC JESD51-6 with the board horizontal.
[4] Thermal resistance between the die and the printed-circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
[5] Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
[6] Thermal characterization parameter indicating the temperature difference between package top the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as psi-JT.

9 Case outline drawing, MCDS, and MSL rating

9.1 Downloading the information from NXP

NXP offers packaging, environmental and compliance information at http://www.nxp.com in the parametric tables and also in the device information details. Enter the part number in the search box and review the package information details of the specific part.

The complete case outline drawing and the material composition declaration sheet (MCDS), following the IPC-1752 reporting format, can be downloaded as a PDF file. Information on product specific MSL is also available in the part details.

9.2 Moisture sensitivity level

The MSL indicates the floor life of the component, its storage conditions, and handling precautions after the original container has been opened. The permissible time, from opening the moisture barrier bag until the final soldering process, a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity.

In many cases, moisture absorption leads to moisture concentrations in the component high enough to damage the package during the reflow process. The expansion of trapped moisture can result in interfacial separation, known as delamination, of the mold compound from the die or substrate, wire bond damage, die damage, and internal cracks. In the most severe cases, the component bulges and pops, known as the popcorn effect.

Therefore, it is necessary to dry moisture-sensitive components then seal them in a moisture barrier antistatic bag with a desiccant and a moisture indicator card. The bag must be vacuum sealed according to IPC/JEDEC J-STD-033 and components removed immediately prior to assembly to the PCB.

Table 3 presents the MSL definitions per IPC/JEDEC J-STD-020. Refer to the moisture sensitivity caution label on the packing material, which contains information about the moisture sensitivity level of NXP products. Components must be mounted and reflowed within the allowable period (floor life out of the bag), and the maximum reflow temperature must not be exceeded during board assembly at the facility of the customer.

If moisture-sensitive components have been exposed to ambient air for longer than the specified time, according to their MSL rating, or the humidity indicator card indicates too much moisture after opening a moisture barrier bag (MBB), bake the components prior to the assembly process. To determine the allowable maximum temperature, refer to imprints or labels on the respective packing.

The higher the MSL value, the more attention is needed to store the components. NXP packages use JEDEC standard IPC/JEDEC J-STD-020 for classification of its package.

Table 3. MSL descriptions

Level rating	Floor life	
	Time	Conditions
1	unlimited	30 °C at 85 % relative humidity (RH)
2	1 year	30 °C at 60 % RH
2a	4 weeks	30 °C at 60 % RH
3	168 hours	30 °C at 60 % RH
4	72 hours	30 °C at 60 % RH
5	48 hours	30 °C at 60 % RH
5a	24 hours	30 °C at 60 % RH
6	time on label (TOL)	30 °C at 60 % RH

10 Package handling

10.1 Handling ESD devices

Semiconductor ICs and components are electrostatic discharge sensitive (ESDS) devices. Proper precautions are required for handling and processing these devices. Electrostatic discharge (ESD) is one of significant factors leading to damage and failure of semiconductor ICs and components, and comprehensive ESD controls to protect ESDS during handling and processing must be considered.

The following industry standards describe detailed requirements for proper ESD controls. NXP recommends that users meet the standards before handling and processing ESDS. Detailed ESD specifications of devices are available in each device data sheet.

- JESD625C - Requirements for handling electrostatic-discharge-sensitive (ESDS) devices
- IEC-101/61340-5 - Specification for the Protection of Electronic Devices from Electrostatic Phenomena

10.2 Handling moisture-sensitive SMD

LGA devices are moisture/reflow sensitive surface mount devices (SMDs). Proper precautions are required for handling, packing, shipping, and using these devices. Moisture from atmospheric humidity enters permeable packaging materials by diffusion. Assembly processes used to solder SMD packages to PCBs expose the entire package body to temperatures higher than 200 °C. As noted in Section 9.2 "Moisture sensitivity level", during solder reflow, the combination of rapid moisture expansion, material mismatch, and material interface degradation can result in package cracking and/or delamination of critical interfaces within the package. Cracking and/or delamination can lead to failure and reliability concerns, and proper handling of SMDs should be considered.

Dried moisture-sensitive SMDs are placed in tray or tape-and-reel, and dry packed for proper transportation and storage. SMDs are sealed with desiccant material and a humidity indicator card inside an MBB. The shelf life of dry packed SMDs is 12 months from the dry pack seal date when stored in < 40 °C at 90 % RH environment.

Proper use and storage of moisture-sensitive SMDs are required after the MBB is opened. Improper use and storage increases various quality and reliability risks. SMDs that are subjected to reflow solder or other high temperature processes must be mounted within the period of floor environment specified by MSL, or stored per J-STD-033D standard.

The baking of SMDs is required before mounting if any of the following conditions is experienced:

- SMDs exposed to a specified floor environment greater than specified period
- Humidity indicator card reading > 10 % for level 2a to 5a or > 60 % for level 2 devices when read at 23 °C ± 5.0 °C environment
- SMDs not stored according to J-STD-033D standard

The baking procedure, and more detailed requirements and procedures of handling moisture-sensitive SMDs can be found in the following industry standard:

- IPC/JEDEC J-STD-033D - Handling, Packing, Shipping and Use of Moisture, Reflow, and Process Sensitive Devices

10.3 Packing of devices

LGA devices are contained in a tray or tape-and-reel configuration. The trays and tape-and-reels are dry packed for transportation and storage. Packing media are designed to protect devices from electrical, mechanical, and chemical damages as well as moisture absorption, but proper handling and storage of dry packs is recommended. Improper handling and storage (dropping dry packs, storage exceeding 40 °C at 90 % RH environment, excessive stacking of dry packs, and so on) increase various quality and reliability risks.

- Tray
  - NXP complies with standard JEDEC tray design configuration; see Figure 14.
  - Pin 1 of the device is oriented with lead 1 toward the chamfered corner of the tray.
  - Trays are baked for moisture sensitive SMDs, but the temperature rating of a tray must not be exceeded when devices are baked. Temperature rating can be found at the end-tab of a tray. The recommended baking temperature of trays is 125 °C.
  - Trays are typically banded together with 5 + 1 (five fully loaded trays and one cover tray) stacking and dry packed in MBB. Partial stacking (1 + 1, 2 + 1, and so on) is also available depending on individual requirements.

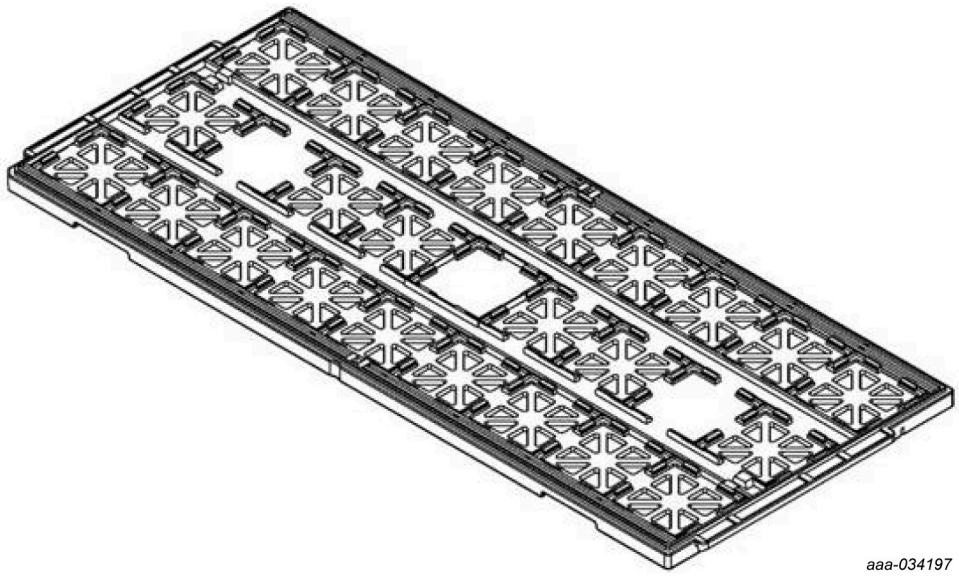


Figure 14. JEDEC tray example

- Tape-and-reel
  - NXP complies with EIA-481-F for carrier tape-and-reel configuration; see Figure 15.
  - NXP complies pin 1 orientation of devices with EIA-481-F.
  - Do not bake tape-and-reels at high temperature.

Each tape-and-reel is typically dry packed in an MBB.

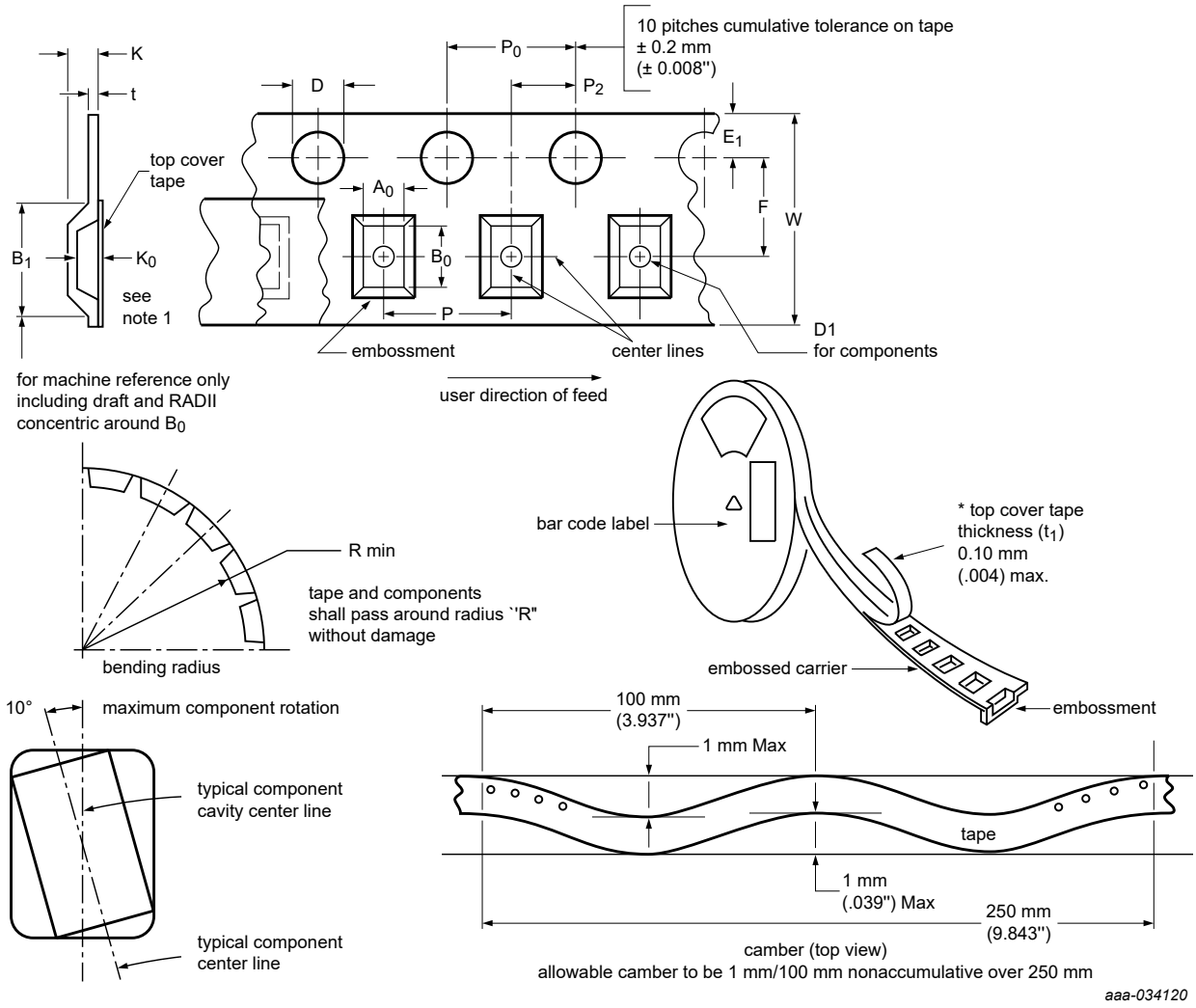


Figure 15. Tape-and-reel example

- Dry packing
  - Trays and tape-and-reels, loaded with devices, are sealed in an MBB, which are labeled and packed in dedicated boxes with dunnage for the final shipment.
  - Each dry pack bag contains a desiccant pouch and a humidity indicator card.
  - NXP encourages the recycling and reuse of materials whenever possible.
  - NXP does not use packing media items processed with or containing Class 1 ozone-depleting substances.
  - Whenever possible, NXP designs its packing configurations to optimize volumetric efficiency and package density to minimize the amount of packing material entering the industrial waste stream.

NXP complies with the following environmental standards conformance guidelines/directives:

- ISPM 15, Guidelines for regulation Wood Packaging Material in International Trade
- European Parliament and Council Directive 94/62/EC of 20 December 1994 on packaging and packaging waste

11 References

[1] IPC/JEDEC J-STD-020F, Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices, December 2022.

[2] IPC/JEDEC J-STD-033D, Joint IPC/JEDEC Standard for handling, packing, shipping, and use of moisture/reflow sensitive surface-mount devices, April 2018.

[3] EIA-783, Guideline Orientation Standard for Multi-Connection Package (Design Rules for tape-and-reel Orientation), November 1998.

[4] JESD51-2A, Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air), January 2007.

[5] EIA/JESD51-8, Integrated Circuit Thermal Test Method Environmental Conditions - Junction-to-Board, October 1999.

[6] EIA/JESD 51-6, Integrated Circuits Thermal Test Method Environment Conditions - Forced Convection (Moving Air), March 1999.

[7] MIL SPEC-883 Method 1012.1, Thermal characteristics, February 2006.

[8] IPC-7351B, Generic Requirements for Surface Mount Design and Land Pattern Standards, June 2010.

[9] IPC-9701A, Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments, February 2006.

[10] IPC/JEDEC-9702, Monotonic Bend Characterization of Board-Level Interconnects, June 2004.

[11] IPC-SM-785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments, November 1992.

[12] JESD22-B111A, Board Level Drop Test Method of Components for Handheld Electronic Products, November 2016.

[13] IPC-1752, Materials Declaration Management, June 2005.

[14] EIA-481, Standards - Excerpts used to assure complete alignment.

[15] JESD625-C, Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices, October 2022.

[16] IEC-101/61340-5, Specification for the Protection of Electronic Devices from Electrostatic Phenomena.

12 Legal information

12.1 Definitions

Draft — A draft status on a document indicates that the content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included in a draft version of a document and shall have no liability for the consequences of use of such information.

12.2 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

Suitability for use in automotive applications — This NXP product has been qualified for use in automotive applications. If this product is used by customer in the development of, or for incorporation into, products or services (a) used in safety critical applications or (b) in which failure could lead to death, personal injury, or severe physical or environmental damage (such products and services hereinafter referred to as "Critical Applications"), then customer makes the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, safety, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. As such, customer assumes all risk related to use of any products in Critical Applications and NXP and its suppliers shall not be liable for any such use by customer. Accordingly, customer will indemnify and hold NXP harmless from any claims, liabilities, damages and associated costs and expenses (including attorneys' fees) that NXP may incur related to customer's incorporation of any product in a Critical Application.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Evaluation products — This product is provided on an "as is" and "with all faults" basis for evaluation purposes only. NXP Semiconductors, its affiliates and their suppliers expressly disclaim all warranties, whether express, implied or statutory, including but not limited to the implied warranties of non-infringement, merchantability and fitness for a particular purpose. The entire risk as to the quality, or arising out of the use or performance, of this product remains with customer.

In no event shall NXP Semiconductors, its affiliates or their suppliers be liable to customer for any special, indirect, consequential, punitive or incidental damages (including without limitation damages for loss of business, business interruption, loss of use, loss of data or information, and the like) arising out the use of or inability to use the product, whether or not based on tort (including negligence), strict liability, breach of contract, breach of warranty or any other theory, even if advised of the possibility of such damages.

Notwithstanding any damages that customer might incur for any reason whatsoever (including without limitation, all damages referenced above and all direct or general damages), the entire liability of NXP Semiconductors, its affiliates and their suppliers and customer's exclusive remedy for all of the foregoing shall be limited to actual damages incurred by customer based on reasonable reliance up to the greater of the amount actually paid by customer for the product or five dollars (US$5.00). The foregoing limitations, exclusions and disclaimers shall apply to the maximum extent permitted by applicable law, even if any remedy fails of its essential purpose.

Translations — A non-English (translated) version of a document, including the legal information in that document, is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Security — Customer understands that all NXP products may be subject to unidentified vulnerabilities or may support established security standards or specifications with known limitations. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer's applications and products. Customer's responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer's applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately.

Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP.

NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

NXP B.V. — NXP B.V. is not an operating company and it does not distribute or sell products.

12.3 Trademarks

Notice: All referenced brands, product names, service names, and trademarks are the property of their respective owners.

NXP — wordmark and logo are trademarks of NXP B.V.

Tables

Figures

Contents

For more information, please visit: http://www.nxp.com

Date of release: 18 September 2023
Document identifier: AN2265