AN2467

Assembly guidelines for PwrQFN (Power Quad Flat no-Lead) packages

Rev. v.6 — December 2020

Application Note

Contents

1 Introduction

This application note provides guidelines for the handling and board mounting of NXP's PwrQFN packages including recommendations for printed-circuit board (PCB) design, board mounting, and rework. Generic information of package properties such as moisture sensitivity level (MSL) rating, board level reliability, mechanical and thermal resistance data are also provided. Semiconductor components are electrical (ESD) and mechanical sensitive devices. Proper precautions for handling, packing and processing are described.

2 Scope

This application note contains generic information about various PwrQFN packages assembled at NXP and NXP's assembly and test vendors. Refer to Section Downloading package information from NXP website of this application note for step by step instructions for retrieving package information. For more details about NXP products, visit www.nxp.com or contact the appropriate product application team.

Development efforts are required to optimize the board assembly process and application design per individual product requirements. Additionally, industry standards (such as IPC and JEDEC), and prevalent practices in the board assembly environment are good references.

3 PwrQFN packages

3.1 Package description

The PwrQFN is a surface mount plastic package with lead pads located on the bottom surface of the package. All PwrQFN packages have either been designed with a single exposed die pad or multiple exposed die pads depending on device requirements and intended application. The industry standardization committee, JEDEC, has given a registered designator of MO-251 to describe the family of single exposed pad PwrQFN packages:

Figure 1. PwrQFN Standard (Left) and PwrQFN Custom (Right)

3.2 Packages dimensioning

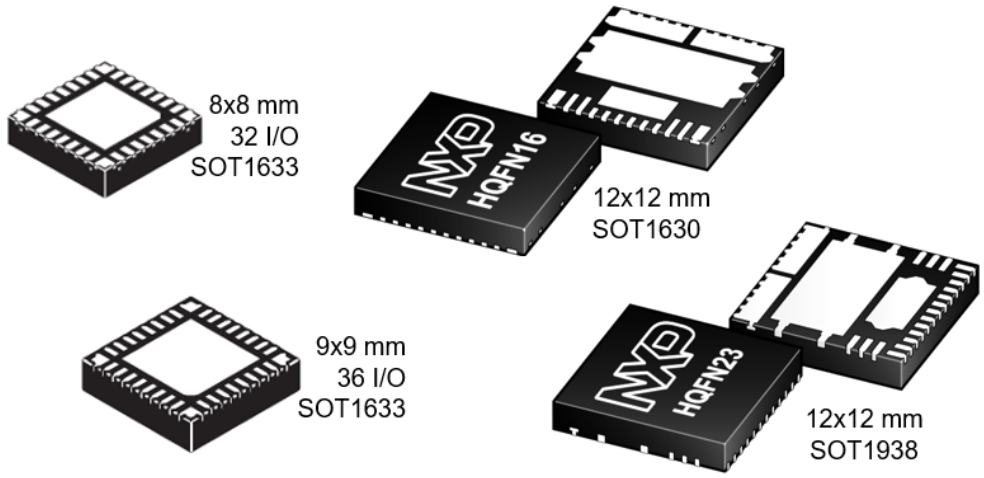


Figure 2. Examples of large size PwrQFN package types

PwrQFN packages range from 5 mm x 5 mm to 12 mm x 12 mm in body size with 2.1 mm height. Lead counts range from 16 to 36. The lead pads have been designed in single-row configurations only. The lead pitch of the perimeter leads is available in 0.65 mm, 0.80 mm and 0.9 mm designs as shown in Figure 2. PCB layout and stencil designs are critical to ensure sufficient solder coverage between the package and the Printed Circuit Board (PCB). When designing the PCB layout, refer to the NXP case outline drawing to obtain the package dimensions and tolerances.

3.3 Package design

Figure 3 shows a cross-section of a typical sawn PwrQFN. The package design is leadframe based. The die is usually soldered to NiPdAu Pre-plated thick copper leadframe with die pad (or flag) exposed external to the package. Either gold or combination of gold and heavy gauge aluminum wire are used for wire bonding between die to lead and die to die. PwrQFN design is a Molded Array Package (MAP). The die pad is exposed external to the package.

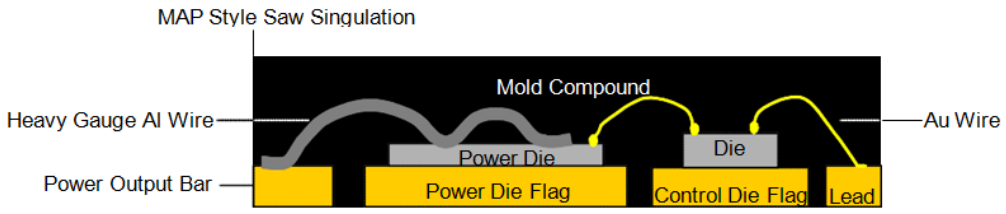


Figure 3. Cross-section of PwrQFN with Heavy wire and exposed pad

3.4 Package terminal types

PwrQFN terminal pads can vary in design, shape and dimensions. Two different terminal designs are common for sawn PwrQFN distinguishable by the geometry of the outer terminal ends.

3.4.1 Fully-exposed terminal ends

This is the standard design of NXP packages (Figure 4). Terminal ends are exposed all the way to the edge of the package when viewed from the bottom of the package. The lead ends are fully exposed to the side of the package. It is possible that a solder

fillet is formed up the side of the component if the terminal end is properly wetted. This may not be the case if the bare copper has been oxidized during NXP dry-bake step or during customer storage.

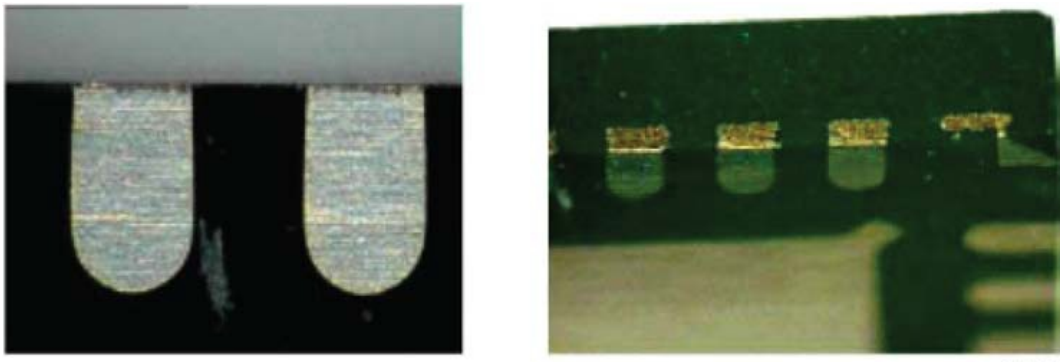


Figure 4. Fully-exposed terminal ends (package bottom and side view)

3.4.2 Pull-back terminal ends

The terminal ends are pulled back from the package edge (Figure 5). Mold compound is visible at the package edge between the edge and the end of the terminal when viewed from the package bottom side. The terminal end is slightly recessed, no solder fillet is expected after the solder reflow process.

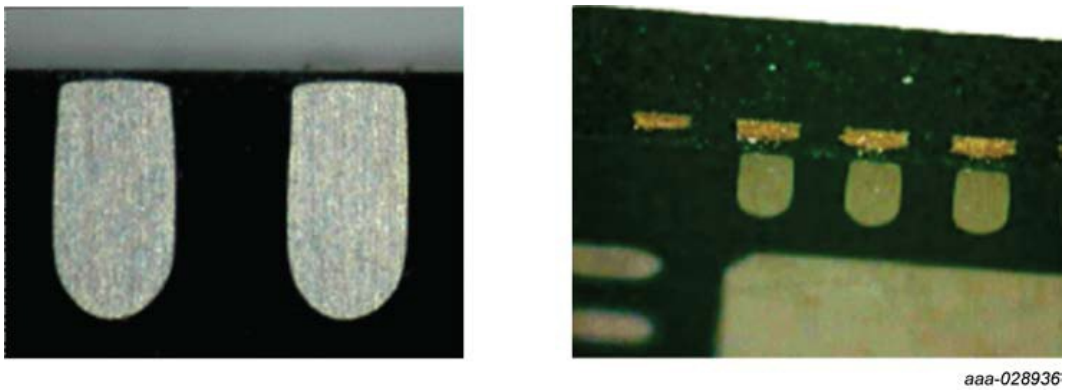


Figure 5. Pull-back terminal ends (package bottom and side view)

3.4.3 Terminal ends with side wettable flank

Wettable flanks (WF) are modifications to the fully-exposed terminal ends, which promote solder wetting for the formation of a solder fillet. Uniform solder fillets are needed to enable inspection for solder failures using automatic optical inspection (AOI) and avoids the need for x-ray inspection, with additional cost and layout restrictions for the PCB.

Figure 6 shows that NXP's primary WF features are step cuts and dimples at the terminal ends. The step cut is formed during the package singulation process, while the “dimpled” terminal is formed during the half-etching step of the leadframe fabrication process. The fillets are formed and should be visible on the PCB after the solder reflow process, as shown in Figure 7 and Figure 8.

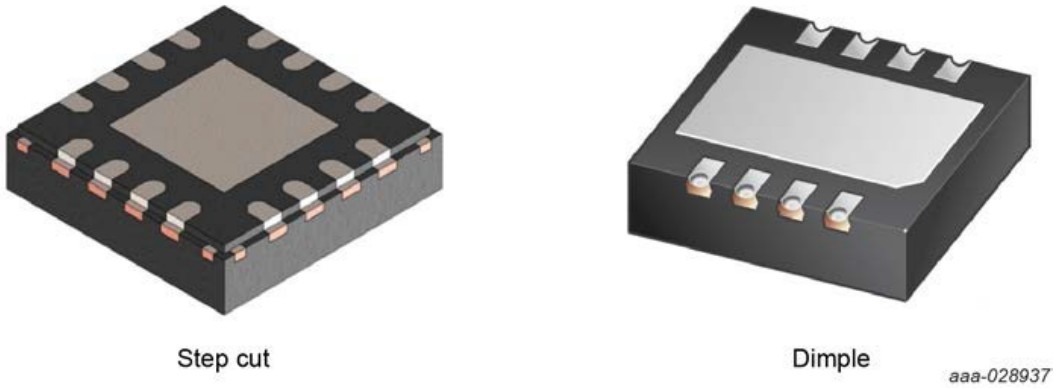


Figure 6. Wettable flank (WF) features of QFN/SON terminal ends

Fillet formation, size and shape is highly dependent upon solder paste, stencil design, board layout, reflow profile, and other PCB assembly parameters. To get optimal results, follow the guidelines in Section 4.2 PCB footprint design".

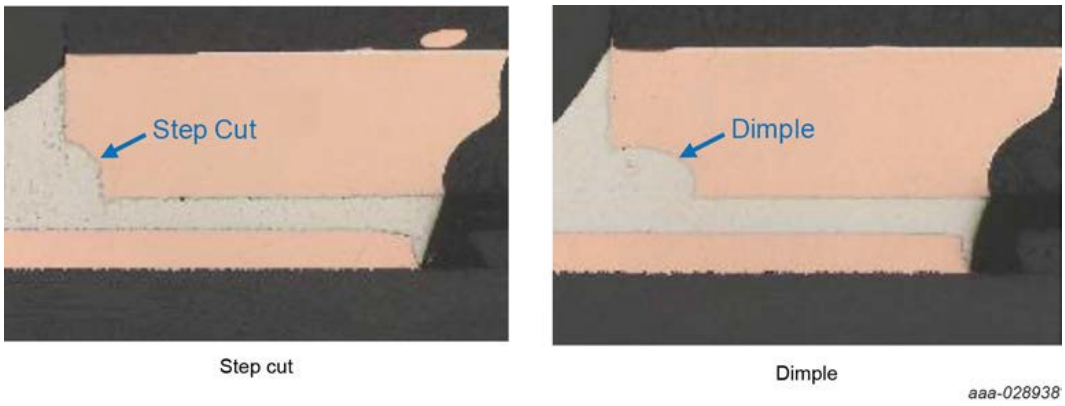


Figure 7. Solder fillets cross-sections after reflow

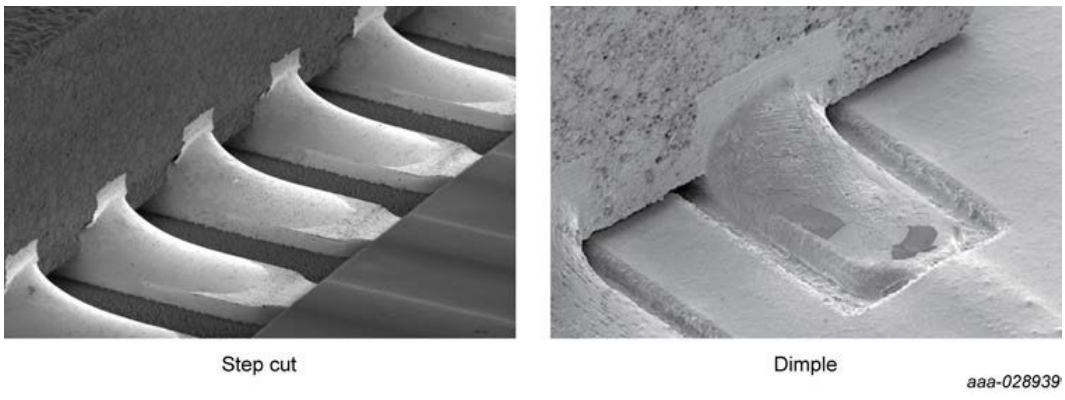


Figure 8. SEM Images of solder fillets cross-sections after reflow

4 Printed-circuit board (PCB) guidelines

4.1 PCB design guidelines and requirements

As the package size shrinks and the terminal count increases, the dimensional tolerance and positioning accuracy affects subsequent processes. Part interchangeability is also

a concern when two separate suppliers provide production parts for the PCB. The optimized PCB layout for one supplier may have issues (manufacturing yield and/or solder joint life) with the other supplier's parts. When more than one source is expected, the PCB layout should be optimized for both parts. Additional information of this topic is provided in this section.

A proper PCB footprint and stencil design is critical to surface mount assembly yields and subsequent electrical and mechanical performance of the mounted package. The design starts with obtaining the correct package drawing. Package outline drawings are available at www.nxp.com (follow the procedure described in Section Downloading package information from NXP website). The drawing contains the package dimensions as well as the recommended footprint (land pattern) for soldering.

Figure 9 shows an example package outline drawing for a PwrQFN.

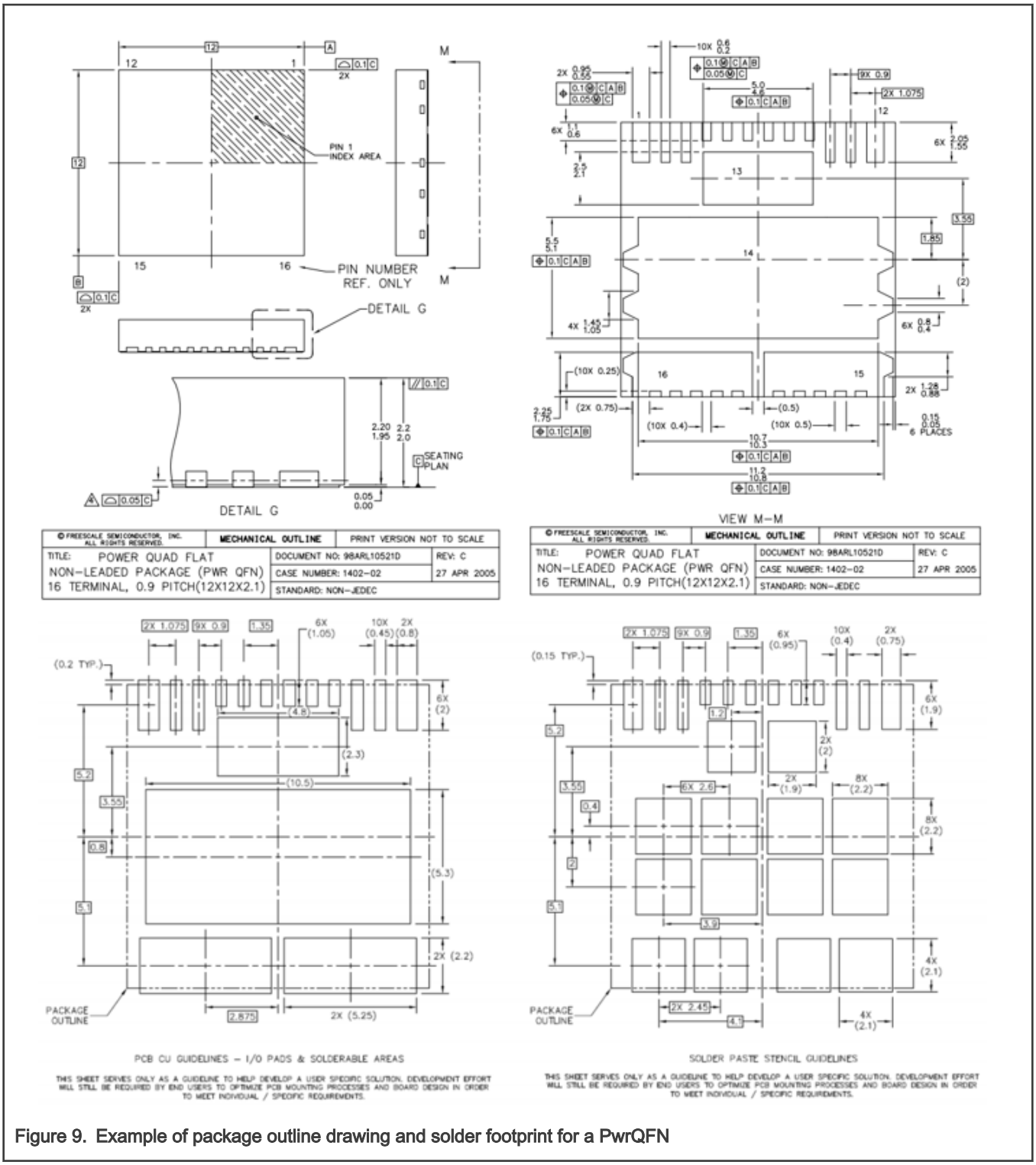


Figure 9. Example of package outline drawing and solder footprint for a PwrQFN

NOTE

This footprint is meant be used as guideline and a starting point for individual PCB designs. To achieve optimum assembly quality, the user must adapt the footprint to meet needs, assembly, and application environment

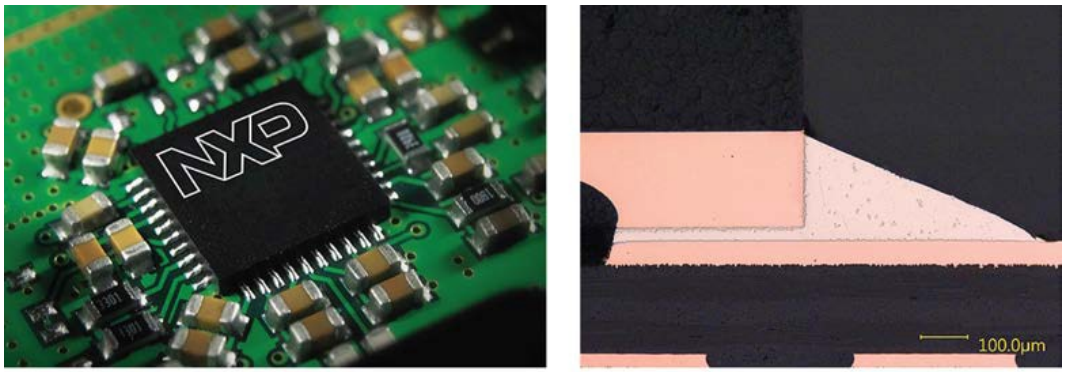


Figure 10. A well-soldered QFN/SON package

The cross-section picture in Figure 10 shows the goal of a well-soldered PwrQFN terminal, void-free solder joint and a smooth solder fillet.

4.2 PCB footprint design

4.2.1 Guidelines for perimeter land patterns

A land is the conductive pattern on the PCB used for the solder connection of a component. The land pattern is a combination of lands intended for the board mounting of a particular component. In NXP documents land patterns are also referred as footprint for reflow soldering.

NXP follows the generic requirements for surface mount design and land pattern standards from the Institute for Printed Circuits (IPC) document IPC-7351. The document can be purchased from the IPC's website http://www.ipc.org/ online store, and includes guidelines for a large number of PwrQFN, based on assumed package dimensions.

NXP also recommends considering the guidelines given in IPC-7093 Design and Assembly Process Implementation for Bottom Termination Components for PwrQFN PCB and process design.

4.2.1.1 Guidelines for size of perimeter Cu-lands:

All PCB land calculation should be based on the nominal size of the package terminal. Length of perimeter lands:

- The land should extend ~0.05 mm towards the center of the package (Figure 11).
- The land should extend ≥ 0.20 mm from the package edge to the exterior for PwrQFN with fully-exposed lead ends.
- The land should extend ≥ 0.40 mm from the package edge to the exterior for PwrQFN with side wettable flanks to form inspectable toe solder fillets (Figure 11). If board space allows, a longer land extension (such as 0.60 mm) will generally result in more consistent fillet formation because it will be influenced less by PCB assembly issues (e.g. misalignment).
- The PCB land should not extend beyond the package edge for packages with pull-back terminal ends.

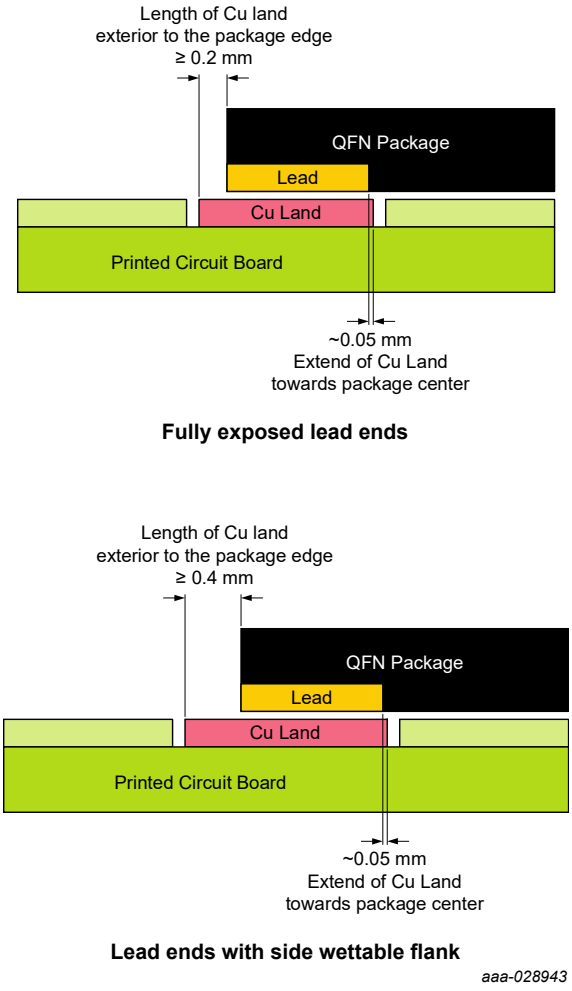


Figure 11. Length of perimeter copper lands

Width of perimeter lands:

- The PCB land width should be approximately the same as the nominal package terminal width (see Table 1).
- Terminal pitch needs to be designed using the exact dimensions of 0.40 mm, 0.50 mm, 0.65 mm, 0.80 mm and 1.00 mm.

Table 1. Recommended land width as a function of terminal pitch

Terminal pitch (mm)	Land width (mm)
0.40	0.200
0.50	0.250
0.65	0.370
0.80	0.400
1.00	0.500

4.2.1.2 Solder mask guidelines for perimeter lands

For perimeter PCB lands, it is recommended to use non-solder mask-defined (NSMD), because they provide significant advantages over solder mask-defined (SMD) lands in terms of dimensional tolerances and registration accuracy. The NSMD has a solder mask opening that is larger than the copper land, and the PCB pad area is controlled by the size of the copper land. Since the copper etching process is capable and stable, a smaller size copper land can be defined more accurately. Figure 12 shows the pad design concepts.

The solder mask should be pulled away from the perimeter lands to account for the registration tolerance of the solder mask. The opening should be 0.12 mm to 0.15 mm larger than the land size resulting in 0.060 mm to 0.075 mm clearance between the copper land and solder mask (IPC-7351).

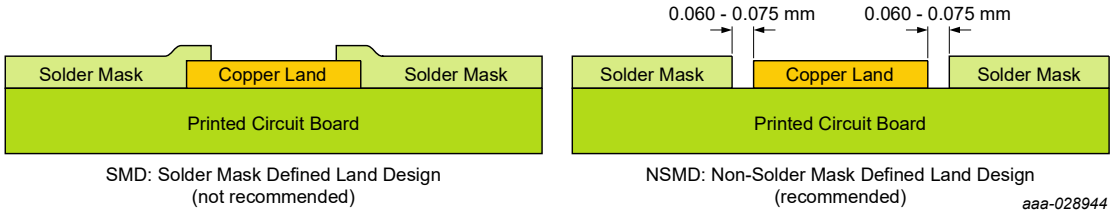


Figure 12. SMD and NSMD land designs

Each land should have its own solder mask opening with a web of solder mask between two adjacent leads (Figure 13). IPC-7351 recommends having at least 0.075 mm of web width to ensure adhesion to the PCB surface is sufficient. Minimum solder mask width will also depend on PCB manufacturer capabilities.

Individual solder mask openings will not work for pitches ≤ 0.40 mm, taking requirements for minimum spacing and width of solder mask into account. A single large solder mask opening for all lands can be used as an alternative design for small pitches (Figure 13).

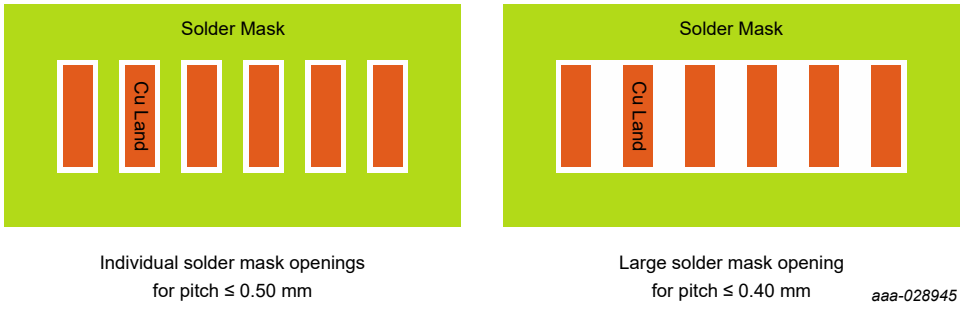


Figure 13. Solder mask design for perimeter land pattern

4.2.1.3 Clearance to vias and adjacent components

Placement of exposed, not covered by solder mask, PCB vias and traces near package corners should be avoided to eliminate potential shorting between exposed package tie- bar features.

Other surface mount devices and insertion components (THT or through hole technology) should be placed sufficiently away from package land pattern area to avoid potential package and board defects.

4.2.1.4 Keep out areas for QFN accelerometer sensors

Avoid positioning screw holes for PCB attachment near the accelerometer location. Doing so may flex the PCB and affect product performance.

To prevent the risk of package tie-bar shorting with PCB traces, it is recommended that vias and other insertion components are kept at least 2 mm away from the package edge.

4.2.2 Guideline for exposed pad land patterns

PwrQFN packages with an exposed pad (EP) on the bottom, enhance the thermal and electrical performance of the package. The die is attached directly to the exposed pad thus providing an efficient heat removal path, as well as excellent electrical grounding to the PCB as shown in Figure 14. To further optimize thermal performance, the PCB design should include thermal vias and a thermal plane(s).

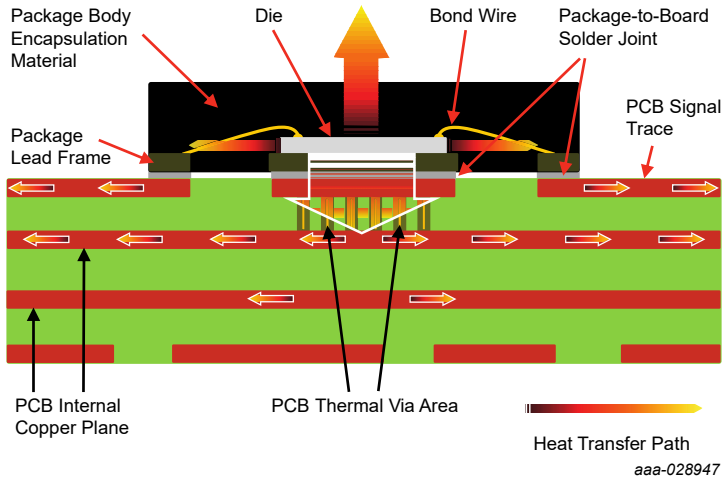


Figure 14. Cross-section of QFN/SON package and PCB showing heat transfers

Although the land pattern design of the perimeter lands for exposed pad packages should be the same as that for non-thermally/electrically enhanced packages, extra features are required during the PCB design and assembly stage for effectively mounting thermally/electrically enhanced packages. In addition, repair and rework of assembled exposed pad packages may involve some extra steps, depending upon the current rework practice within the company.

4.2.2.1 Spacing between perimeter and exposed pad land pattern

The design of the land pattern and the size of the exposed thermal pad depends strongly on the thermal characteristics and power dissipation of the specific product and application. To maximize both removal of heat from the package and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad (as shown in Figure 15).

The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package. However, the area that can be soldered (which should be defined by the solder mask) should be approximately the same size/shape as the exposed pad area on the package to maximize the thermal/electrical performance. A clearance of at least 0.25 mm should be designed on the PCB between the outer edges of the exposed pad land pattern and the inner edges of perimeter land pattern to avoid any shorts.

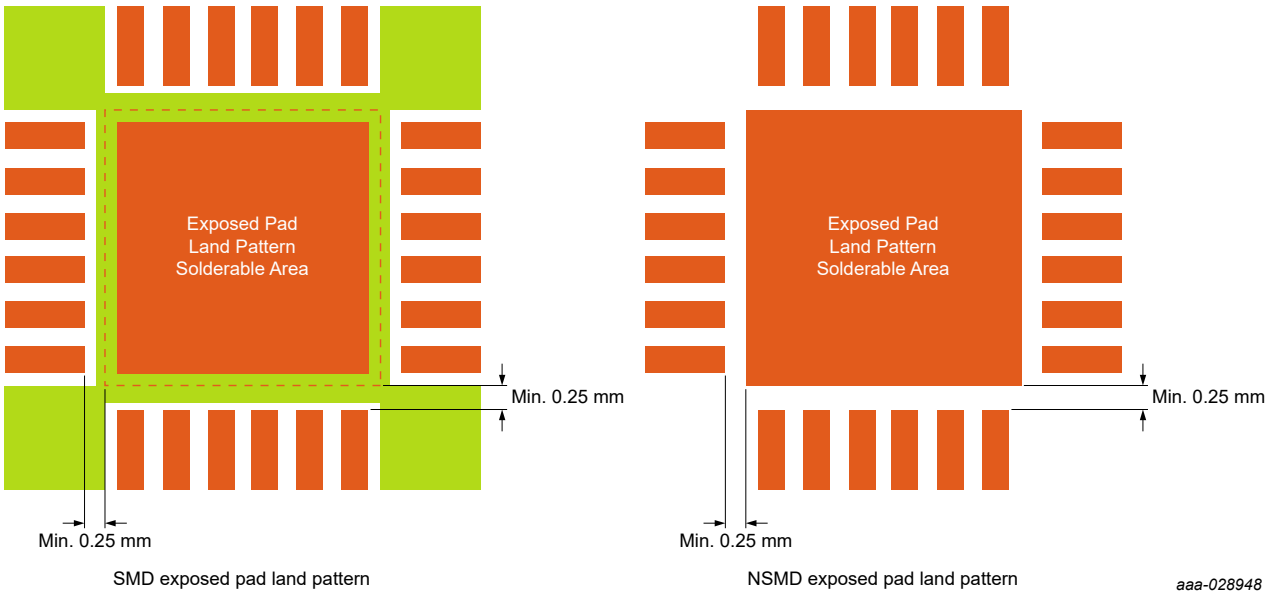


Figure 15. Minimum clearance between perimeter and exposed pad land pattern

4.2.2.2 Segmented exposed pad land pattern design

Alternatively, the land pattern for the exposed pad can be segmented into a symmetric array of square or rectangular lands, as shown in Figure 16. The land array can be created either by segmentation of a full copper area by solder mask openings, or by NSDM defined copper lands.

- Recommended edge length/width of a matrix land is between 1.0 mm to 2.0 mm
- Distance between the lands should be 0.40 mm

The segmented PCB design facilitates the solder paste flux outgassing during reflow, thereby promoting a lower voiding level of the completed solder joint. The maximum size of a single solder void is limited by the dimensions of a single matrix segment at the same time.

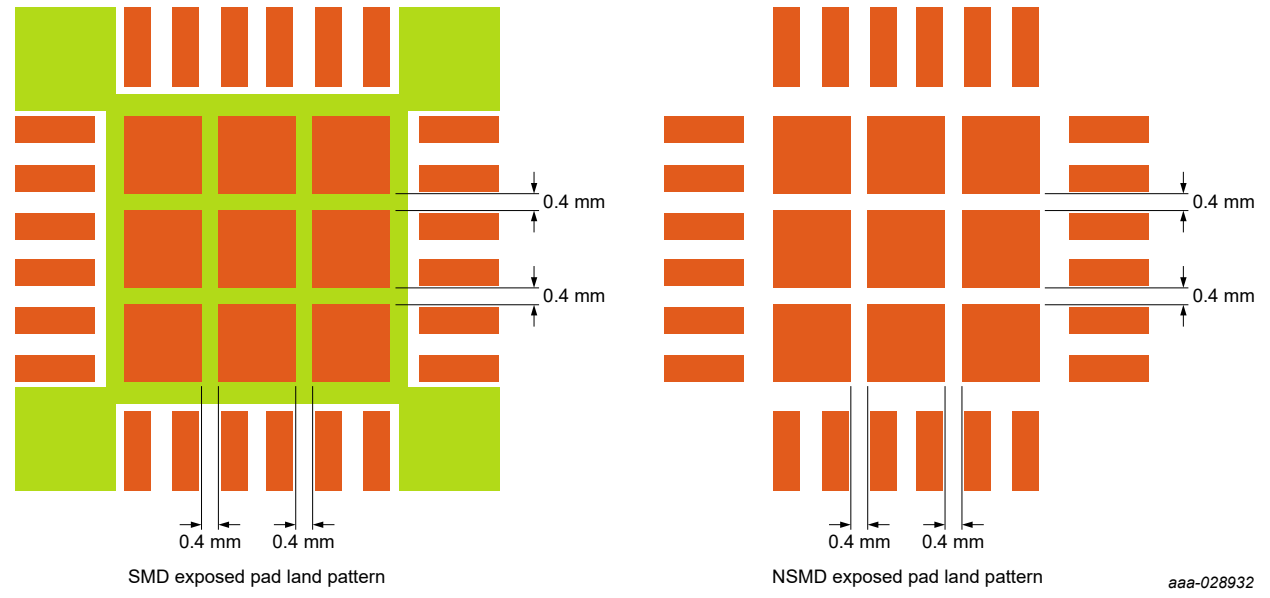


Figure 16. Segmented exposed pad land patterns

4.2.2.3 Thermal vias in the exposed pad land pattern

While the land pattern on the PCB provides a means of heat transfer/electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct the heat from the surface of the PCB to the ground plane(s). These vias act as “heat pipes”. The number of vias is application specific and depends upon the product power dissipation and electrical conductivity requirements.

- Thermal and electrical analysis and/or testing are recommended to determine the minimum number of vias required.
- Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern at a 1.20 mm grid, as shown in Figure 17.
- It is recommended that the via diameter be 0.30 mm to 0.33 mm with 35 µm Cu plating thickness (1.0 oz/ft^2). This is desirable to avoid any solder-wicking inside the via during the soldering process, which may result in solder voids in the joint between the exposed pad and the thermal land.
- If the copper plating does not plug the vias, then the thermal vias can be “tented” with solder mask on the top surface of the PCB to avoid solder wicking inside the via during assembly. The solder mask diameter should be at least 0.10 mm larger than the via diameter.

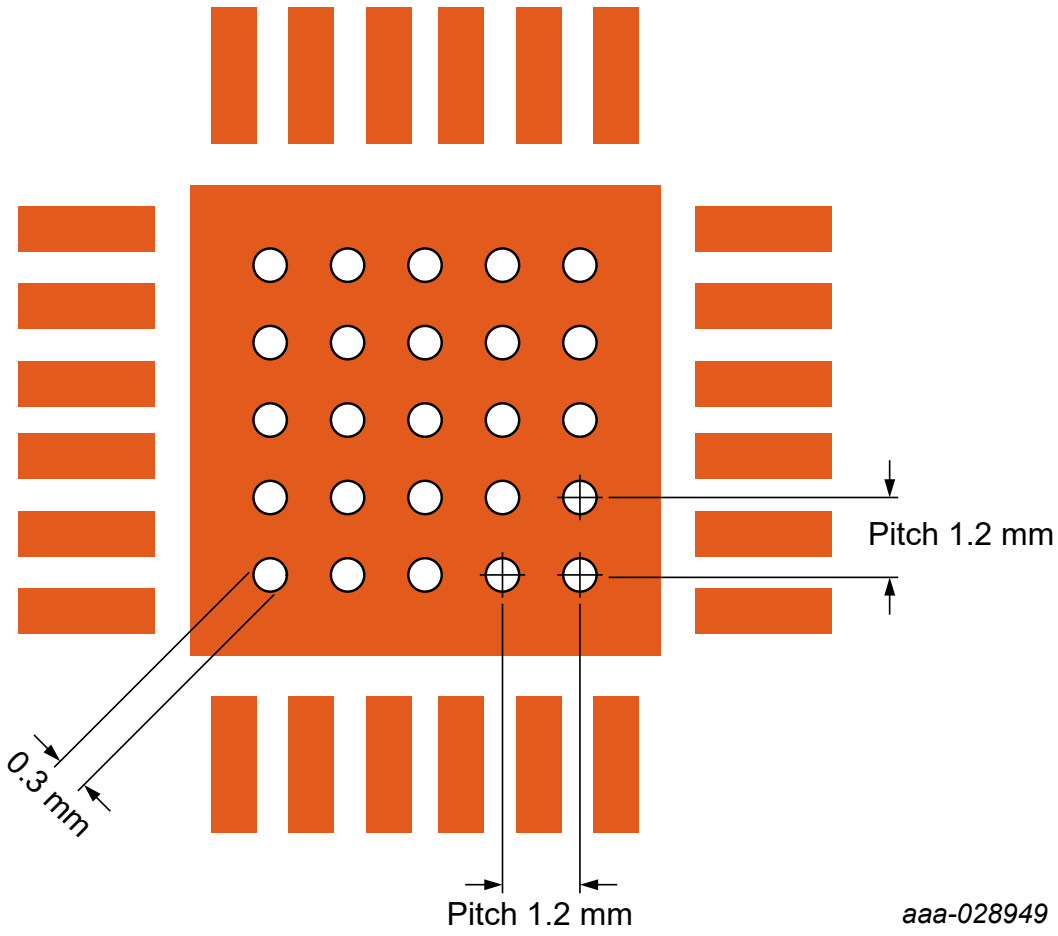


Figure 17. Exposed pad land pattern with array of thermal vias

Design options for combination of vias with a segmented exposed pad land pattern are shown in Figure 18.

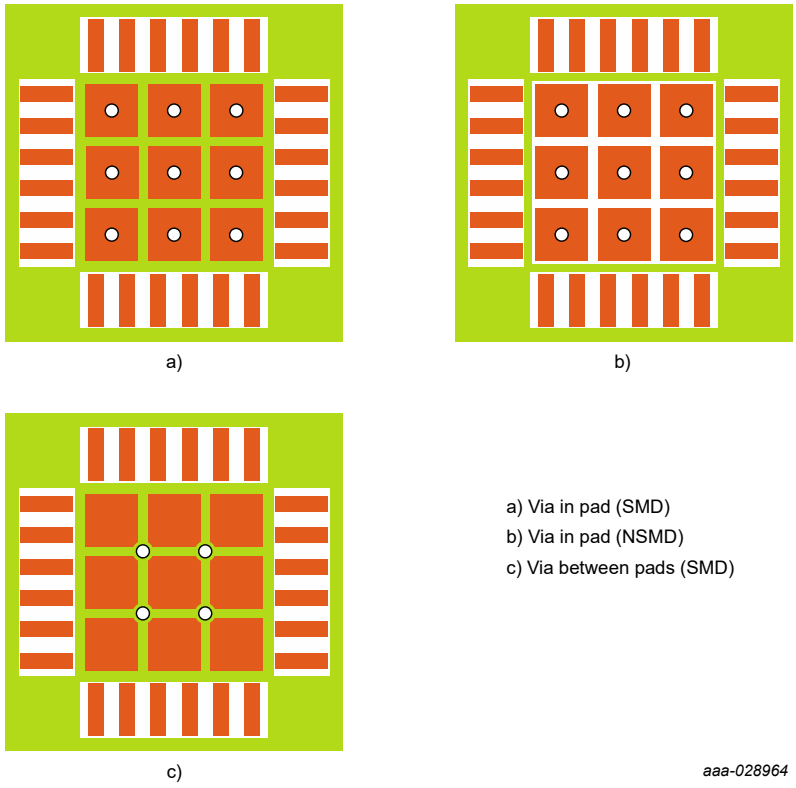


Figure 18. Segmented exposed pad land pattern with vias

4.2.3 Exposed pad design, for PwrQFN packages with non-symmetric perimeter pad design and multiple exposed pads

Figure 19. Example of PwrQFN package with non-symmetric perimeter pad and multiple exposed

The design of the land pattern and the size of the thermal pad depend strongly on the thermal characteristics and power dissipation of the specific product and application. The size of the land pattern can be larger, smaller, or even take on a different shape than the exposed pad on the package. To maximize both removal of heat from the package and electrical performance, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad as shown in Figure 19. Some general guidelines for perimeter pad on PwrQFN exposed pad footprints are: All PCB exposed pad calculation should be based on the nominal size of the package exposed pad size.

- The size of the PCB exposed pad land pattern should be approximately the same as the nominal size of the corresponding package exposed pad.
- Making the PCB pad 1:1 shape may not be valuable. Instead, the PCB pad should be "square" to the package pad side. See Figure 20 for example.
- For exposed package pads extending to the package edge (such as pad #15 and #16 in Figure 20), the PCB Cu pad lengths should extend from the package edge by 0.2 mm.
- A clearance of at least 0.25 mm should be designed on the PCB between the outer edges of the exposed pad land pattern and the inner edges of perimeter pad pattern as well as between the edges of neighboring exposed land patterns to avoid any shorts.

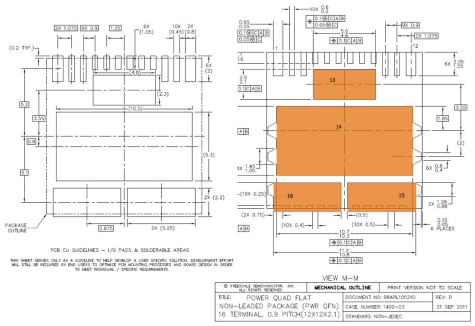


Figure 20. PCB Exposed Pad Land Pattern

If the guidelines described previously lead to unacceptably high voiding levels in board attach soldering, or prevention of high voiding levels is desired, the exposed pad PCB land pattern design can be modified as described in the following.

4.2.3.1 Alternative Exposed Pad Design – Option 1

The exposed pad solder land can be segmented into a pad array as shown below in Figure 21. The pad array should be created by segmentation of a full copper area by solder mask webbing. Recommended edge length of a matrix pad is between 1.0 mm – 2.0mm, the distance between the individual pads should be 0.2 mm - 0.4mm. The minimum distance (width of the solder mask webbing) needs to be aligned with the PCB manufacturers design rules and manufacturing capabilities

The segmented PCB design facilitates the solder paste flux outgassing during reflow, thereby promoting a lower voiding level of the completed solder joint. At the same time, the maximum size of a single solder void is limited by the dimensions of a single matrix segment

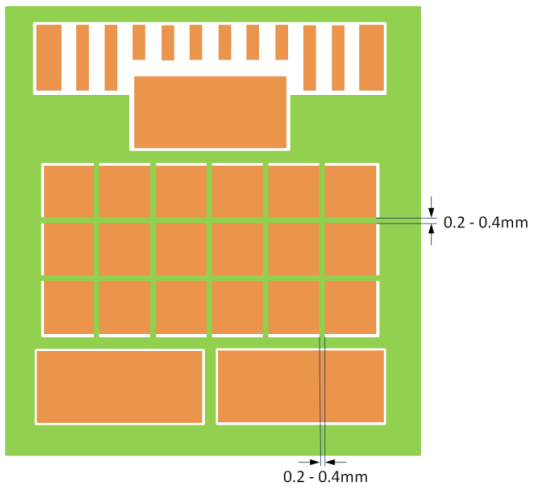


Figure 21. PCB Exposed Pad Land Pattern Segmented by Solder

4.2.3.2 Alternative Exposed Pad Design Option 2

Alternatively, the exposed pad solder land can be split up into a pad array of single Cu pads as shown below in Figure 22. Recommended edge length of a matrix pad is between 1 mm -2 mm, the distance between the pads should be between 0.2 mm - 0.4 mm. The segmented PCB design facilitates the solder paste flux outgassing during reflow, thereby promoting a lower voiding level of the completed solder joint. At the same time, the maximum size of a single solder void is limited by the dimensions of a single matrix segment.

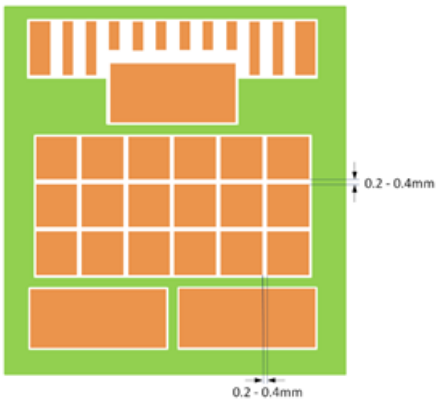


Figure 22. PCB Exposed Pad Land Pattern Segmented by Copper Defined

4.2.3.3 Vias in the PCB Exposed Pad Land Pattern

While the land pattern on the PCB provides a means of heat transfer/electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). These vias act as “heat pipes”. The number of vias is application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number required. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern at 1.2 mm grid, as shown in Figure 23.

NOTE

These recommendations are to be used as a guideline only

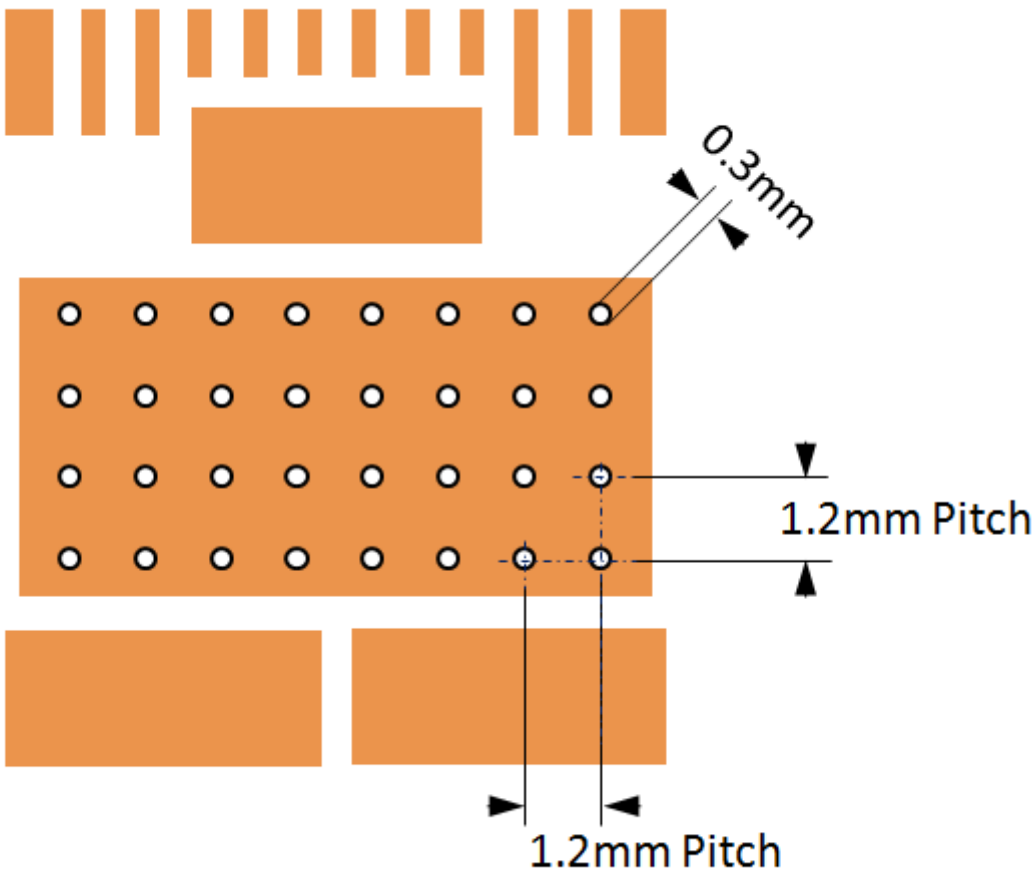


Figure 23. PCB Exposed Pad Land Pattern Via Grid

4.2.3.4 Vias in Alternative Exposed Pad Design – Option 1

For solder mask defined array pad design option, there are various thermal via arrangements possible.

- Via is placed in the center of the pad, as show in below Figure 24 on the left image. Vias are placed in the cross-points of the solder mask webbing, as shown Figure 24 on the right image.

All the vias in these two cases must be plugged, tented or plated

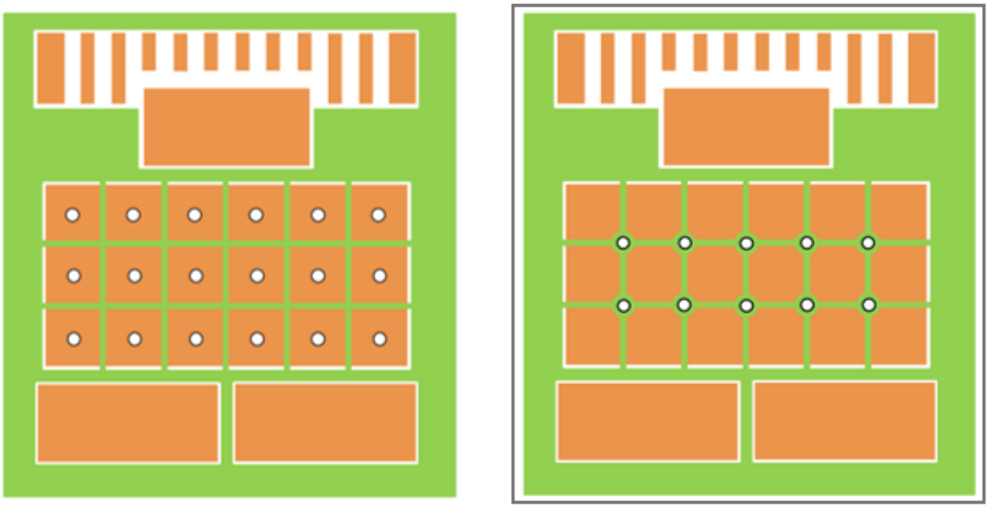


Figure 24. Via Placement Options for Solder Mask Defined Array Pad

4.2.3.5 Vias in Alternative Exposed Pad Design – Option 2

For copper defined array pad design option, it is recommended to place the thermal via in the center of the pad, as show in below Figure 25. The via must be plugged, tented or plated.

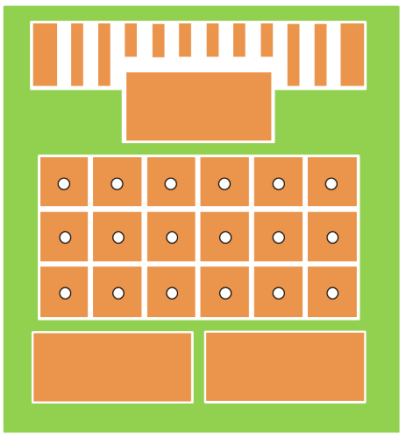


Figure 25. Via Placement Options for Copper Defined Array Pad

The typical appearance of a completed exposed pad solder joint using copper defined pad array and plugged via technology is shown in Figure 26. Fully wetted PCB pad, void free solder joints with plugged, and non-wetted via area in center of each pad can be observed as expected.

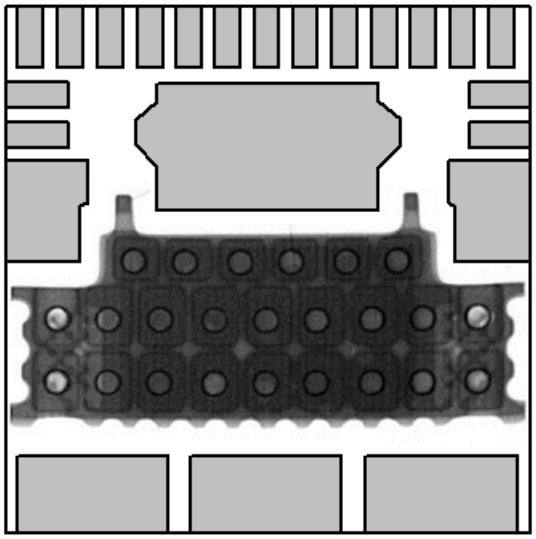


Figure 26. X-ray Image of Copper Defined Pad Array, Typical Appearance

A cross-section of a device using similar design is shown in Figure 27.

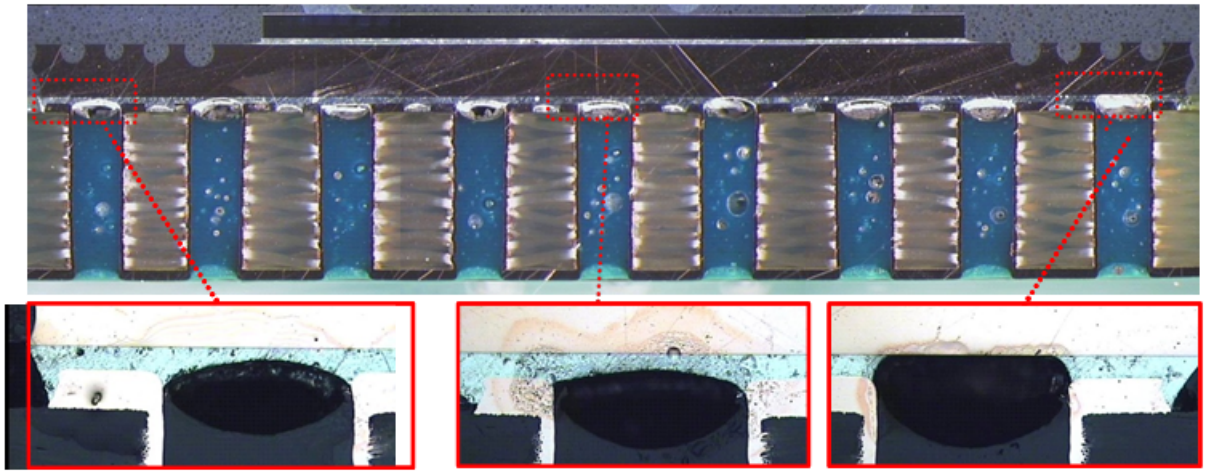


Figure 27. Cross-section image of Copper Defined Pad Array, Typical Appearance

4.2.4 Pad surface finish

Almost all PCB finishes are compatible with PwrQFN, including:

- Organic solderability protectant (OSP)
- Electroless nickel immersion gold (ENIG)
- Immersion Sn
- Immersion Ag

Hot air solder leveled (HASL) finish may cause uneven surface issues and extra caution is required.

4.2.5 Solder Mask Opening for PCB Area

The general solder mask guidelines for perimeter pads are discussed in paragraph 4.2.1. Usually solder mask should be pulled away from the perimeter pads. The solder mask opening around the PCB pads can be as large as the spacing between pads. The area in between the pads may be too thin for the solder mask, resulting in the solder mask lifting off from the PCB. In general, solder mask width should be a minimum of 0.10 mm as shown in Figure 28, but this is only possible for larger pitches. If less than 0.10 mm, there may be solder mask adhesion problems. A potential solution is modification of the solder mask along the pad-to-pad spacing so only the “toes” of the pads are covered with solder mask for better PCB strength.

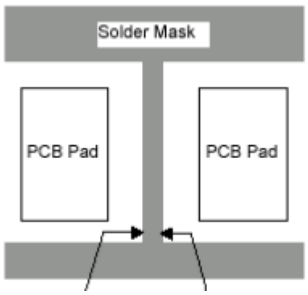
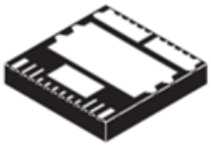


Figure 28. Pad and Solder Mask with Thin Webbing

4.2.5.1 Solder Mask Openings Exposed pad design, for PwrQFN packages with non-symmetric perimeter pad design and multiple exposed pads

The general solder mask guidelines for perimeter pads are discussed in paragraph 4.2.3



- For the PCB exposed pad land pattern, it is recommended to design for solder mask pull-back from the copper pad edge. The clearance between the copper pad and solder mask should be at least 0.15 mm. Please see also Figure 29 on solder mask design concept.
- Alternatively, the solder mask opening can be as large as the package outline, with 0.35 mm clearance on each side between nominal package edge and solder mask. Please see also Figure 30 on solder mask design concept.

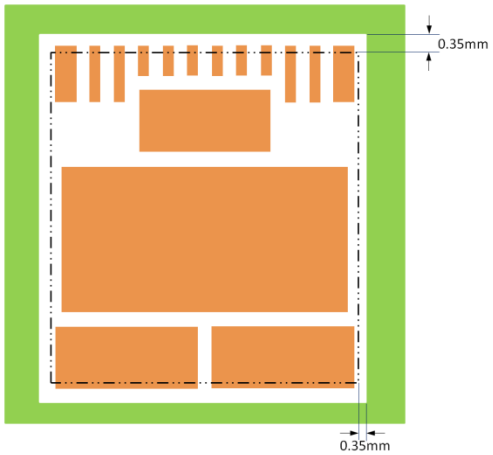


Figure 29. Standard PCB Footprint with 0.15 mm clearance around copper pads

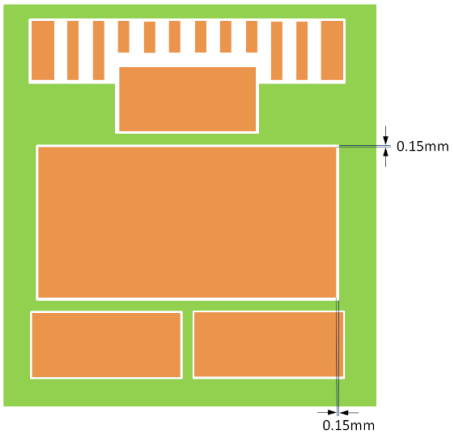


Figure 30. Standard PCB Footprint with 0.35 mm clearance between solder mask and package outline

5 Board assembly

5.1 Assembly process flow

Figure 31 shows a typical surface mount technology (SMT) process flow. Use of standard pick and place process and equipment is recommended and manual or hand soldering should be avoided.

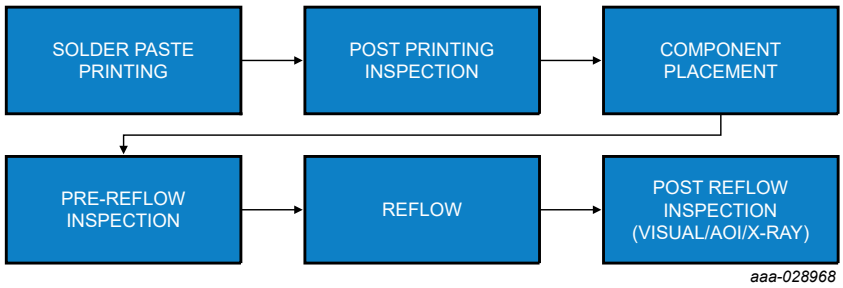


Figure 31. SMT process flow

5.2 Solder paste printing

5.2.1 Solder paste

Solder paste is a homogenous mixture of fine metal alloy particles, flux, and viscosity modifiers to adjust printing and reflow properties. The main features of solder pastes are:

- Solder alloy:

  NXP recommends using lead-free solder paste, in line with environment legislation (RoHS, ELV). A variety of lead-free alloys is available for PCB assembly, with different physical properties and melting temperatures. Common solders alloys are combinations of Tin, Silver, and Copper: SnAg3Cu0.5 (SAC305), SnAg4Cu0.5 (SAC405), or SnAg3.8Cu0.7 (SAC387), with a melting range between 217 °C to 220 °C. The peak reflow temperature for these alloys shall be > 235 °C.

- Solder spheres:

  A main component of the paste is the low-oxide spherical powder made from the solder alloy. The amount of solder powder in the paste is referred to as the metal load and is typically in the range of 83 % to 92 % by weight. The spherical shape and controlled size of the powder particles ensures a uniform printing and a stable paste volume for each solder land. The

solder pastes are classified by spheres size according to IPC standard J-STD-005 (see Table 2). Smaller spheres allow higher printing resolution and smaller pitches. The rule of thumb is that the minimum dimension of the smallest stencil opening shall be larger than 4 to 6 sphere diameters.

Table 2. Solder paste type

Paste type	Sphere diameter	
	Min. (µm)	Max. (µm)
3	25	45
4	20	38
5	10	25
6	5	15

- Flux:

  Flux is needed to remove surface oxidation, prevents oxidation during reflow and improves the wetting of the solder alloy. Solder pastes are classified into three types based on the flux type according to IPC standard J-STD-004:

  — Rosin-based flux

  — Water-soluble flux

- No-clean flux

  Rosin-based and water-soluble fluxes require cleaning of the PCB after reflow process. Standard rosin chemistries are normally cleaned with solvents, semi- aqueous solutions or aqueous/saponified solutions, while the water-soluble chemistries are cleaned with pure water.

  No-clean flux doesn't require cleaning, but normally a little residue remains on the PCB after soldering. In general, it is recommended to use a no-clean solder paste, because cleaning of flux residues from underneath the package is not feasible for a PWRQFN-style package (due to the low package standoff).

5.2.2 Stencil thickness

The thickness of the stencil determines the amount of solder paste deposited onto the printed circuit board land pattern. Due to the fine pitch and small terminal geometry used, care must be taken when printing the solder paste on to the PCB. Typical stencil thicknesses are given in Table 3.

Table 3. Typical Stencil Thickness

Package pitch (mm)	Stencil thickness (µm)
0.50	150
0.40	100 to 125

Since PwrQFN is (most likely) not the only package on the actual production PCB, the recommended stencil thickness for the other packages may be thicker than desired. For such a case, a step-down stencil is recommended, where most of the stencil for the PCB has a typical thickness, but the area for the PWRQFN would be reduced to 100 µm to 150 µm, depending on the package pitch.

NXP encourages customers of PwrQFN packages to use stainless steel foil for the stencil material. The stainless-steel stencil has a long usage life. Additionally, using a laser to cut the openings produces good opening uniformity. When followed by an electro-polish, the solder pastes release off the opening sidewalls more consistently after the printing process. Customers are

strongly encouraged to use X-ray analysis before and after reflowing to confirm that any stencil design can provide sufficient solder paste to the PCB and also keep good separation between regions of solder paste.

5.2.3 Stencil design

The dimension of the stencil openings should be a minimum 25 µm to 30 µm (5 % to 10 %) smaller than the size of the corresponding copper lands to account for alignment and PCB tolerances. A fillet at the corners reduces the adhesion to the solder paste and improves the paste release (Figure 32). The fillet radius depends on the solder paste type; i.e. it should be larger than the diameter of the solder spheres.

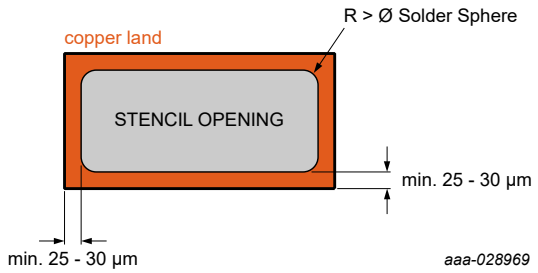
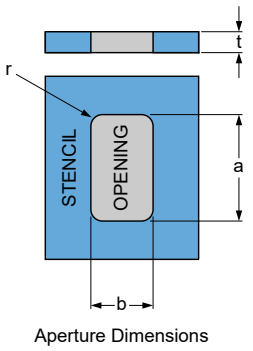


Figure 32. Stencil opening size and corner radius

A minimum aperture size is needed to ensure the proper release of the solder paste during stencil printing (Figure 33). The area ratio and the aspect ratio between stencil opening and stencil thickness are used to determine the minimum dimensions, respectively.

Some general guidelines for exposed pads on PwrQFN footprints are:

- All solder stencil design should be based on the nominal size of the corresponding PCB Cu pad, respectively on the nominal size of the Wettable area of the corresponding PCB pad.
- A large stencil opening may result in poor release. Additionally, during the solder screen print operation, a stencil blade can both deposit solder paste, and remove, or “scoop” it out, in the large aperture openings. In the large openings, the blade bends down into the opening thereby leaving less solder volume than anticipated. To mitigate the effect of scooping, the aperture should be broken up into an array of smaller openings, i.e. by subdividing the aperture opening into an array of smaller openings, similar to the pattern shown in Figure 34
- The stencil opening should have a pullback of ~0.150 mm – 0.250 mm on each side from the PCB Cu pad edge.
- The side length of a individual opening should range ~1.5 mm – 2.5 mm
- The distance/spacing between the individual array stencil openings should be at least 0.250mm, as shown in Figure 34.
- The stencil opening should be approximately 55 % – 70 % of the total PCB thermal pad area. This stencil-PCB thermal pad ratio ensures proper coverage of the thermal pad area with fewer voids and minimizes the possibility of overflow bridging to the adjacent lead.



Aperture Dimensions

$$\text{Aspect Ratio} = \frac{\text{smallest aperture dimension (a or b)}}{\text{stencil thickness}}$$

$$\text{Aspect Ratio} = \frac{\min [a, b]}{t} > 1.5$$

Example: Minimum width for stencil thickness 150 µm

$$\frac{b}{150\ \mu m} > 1.5 \Rightarrow b > 1.5 \times 150\ \mu m \Rightarrow b > 225\ \mu m$$

$$\text{Area Ratio} = \frac{\text{projected aperture area}}{\text{aperture side wall area}}$$

$$\text{Area Ratio} = \frac{ab - r2\,(4 - \pi)}{2t\,[a + b + r\,(\pi - 4)]} > 0.66$$

aaa-028970

Figure 33. Area ratio and aspect ratio

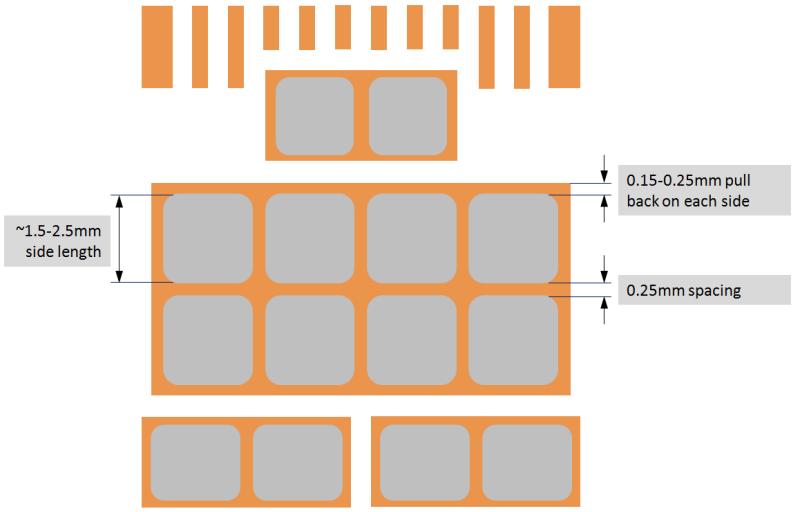


Figure 34. Examples of solder paste stencil design on exposed pad

5.3 Component placement

Increased package interconnection density requires precise and accurate pick and place tools. To meet this tight requirement, a placement machine equipped with an optical recognition system for the centering of the PCB and the components during the pick-and- place motion is recommended. A placement accuracy study is suggested to calculate compensations required.

Products in PwrQFN packages are assembled on NXP's production lines and production lines operated by NXP's assembly and test vendors. Packages with the same outline can have different design features to identify the package orientation and location of pin 1 when the package is viewed from bottom side (see Section Keep out areas for QFN accelerometer sensors). Also, the leadframe finish may reflect differently in the vision system. If parts are supplied by more than one assembly line, then it is necessary to create dedicated equipment recipes.

Refer to Section Packing of devices, for package orientation and location of pin 1 in JEDEC trays or tape and reel carriers.

5.4 Reflow soldering

The temperature profile is the most important control in reflow soldering, and it must be fine tuned to establish a robust process. The actual profile parameters depend upon the solder paste and alloy used; the recommendations from paste manufacturers should be followed. Nitrogen reflow is recommended to improve solderability and to reduce defects (like solder balls).

When a board is exposed to the reflow oven temperature, certain areas on the board will heat faster than others depending on the thermal mass. Large components and large copper areas in the board will heat up slower than small components and board areas with little copper. The actual temperature shall be measured with thermocouples at various places on the PCB surface to ensure that the reflow temperature is reached everywhere on the board.

The temperature of package top surface shall be monitored at the same time, to validate that the peak package body temperature (T_P) does not exceed the MSL classification of individual devices (see IPC/JEDEC J-STD020).

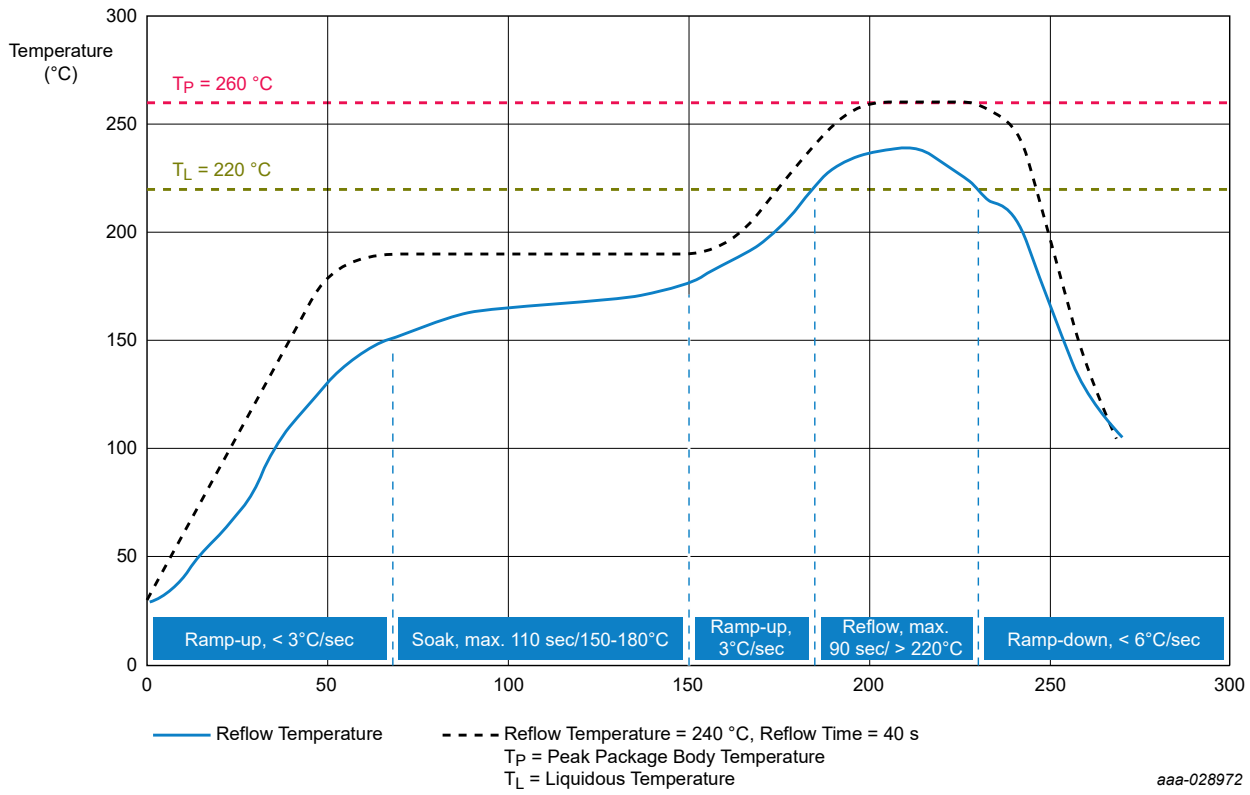


Figure 35. Typical reflow profile for PwrQFN with lead-free SAC

Figure 35 shows a typical time/temperature profile (blue) for reflow soldering with lead- free SAC solder alloys using a multi-zone reflow oven. The maximum allowed package body temperature at every stage of the process (depending on the IPC/JEDEC J-STD-020 classification of the package) is represented by the dashed gray line. The reflow profile is divided into five stages:

- Ramp-up to soak

  The printed circuit board should be heated evenly to avoid overheating of components. Volatile solvents in the solder paste start to outgas during ramp up. Too fast temperature increase could cause solder balling. The maximum ramp-up rate shall not exceed 3 °C/second to avoid overstress to the package.

- Pre-heat and soak

  The PCB assembly is held at 150 °C to 180 °C temperature for 60 to 120 seconds during thermal soak. The volatiles in the solder paste will be removed and the flux is being activated to reduce oxides from the pads and lands. Time and temperature are recommended by the paste supplier depending on the flux type.

- Ramp-up to reflow

  The PCB assembly is uniformly heated above the liquidous temperature of the solder alloy. Again, the maximum ramp-up rate shall not exceed 3 °C/second to avoid overstress to the package.

- Reflow

The recommended peak reflow temperature for SAC alloys shall be > 235 °C. The period above the liquidous temperature (T_L) is called the reflow time. It shall be long enough to allow the liquid solder to uniformly wet the pad and land surfaces and to form an intermetallic phase. Too long reflow time may lead to brittle solder joints and could cause damage to the board and components. The peak package body temperature (T_P) must not exceed 260 °C and the time above 255 °C must not exceed 30 seconds depending on IPC/JEDEC classification.

- Cool down

  Fast cool down prevents excess intermetallic formation and creates a fine grain structure of the solder alloy. The ramp-down rate can be faster than the ramp-up, but shall not exceed 6 °C/second to avoid overstress.

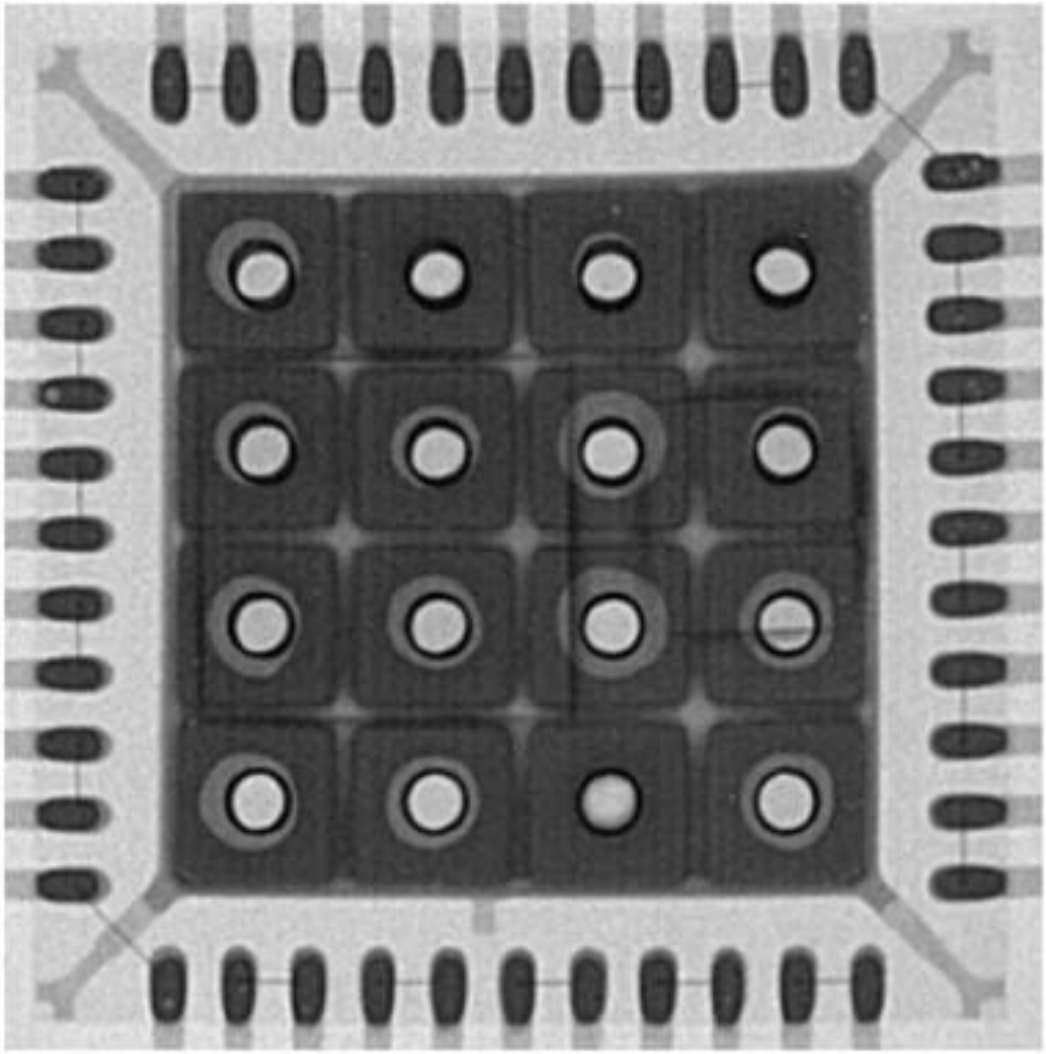
The reflow profile for exposed pad packages need not be any different than the one used for non-thermally/electrically enhanced packages.

Cross referencing with the device data sheet is recommended for any additional board assembly guidelines specific to the exact product used.

5.5 Inspection

Unlike traditional leaded components, the solder joints of PwrQFN are formed primarily underneath the package. To verify any open or short circuits (bridging) after reflow soldering, optical inspection and x-ray inspection are recommended. Micro-sectioning is another method of inspecting solder joint quality during process optimizations, but it is less suitable to production inspection (due to slow processing).

Figure 36 shows the x-ray image of a soldered QFN44 package with exposed pad and pull-back terminal ends. The dark gray areas represent the solder joints. Light gray spots within the solder joints are due to solder voids. The perimeter lands are well soldered with very little voiding. The land pattern for the exposed pad is segmented with a thermal via within each square. The voids around the vias are not regarded as defects.



HVQFN44 9x9 with segmented exposed pad land pattern, thermal vias in the exposed pad land, and a daisy-chain wire bond configuration

aaa-028973

Figure 36. X-ray inspection of a QFN package after soldering

Figure 37 shows an example of shorted solder joints caused by excess spread of solder paste during reflow or high solder amount.

Figure 37. Visual optical inspection of QFN after assembly

Figure 38 shows an issue with excess solder voids at the exposed pad. The large single copper land used for the exposed pad prevents the proper outgassing of volatile solvents from the solder paste. The perimeter solder joints show either poor wetting or shorts between terminals.

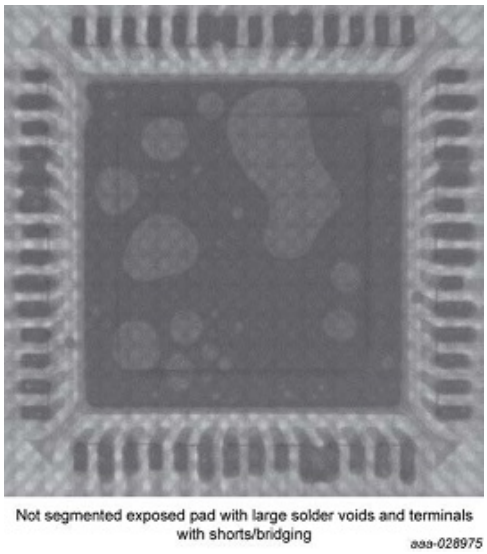


Figure 38. X-ray of QFN package after assembly

6 Repair and rework procedure

6.1 Repairing

Repairing a single solder joint of PwrQFN or the soldered exposed die pad is not recommended. The solder joints of terminals and exposed pad underneath the package cannot be soldered in a controlled way.

6.2 Reworking

If a defective component is observed after board assembly, the device can be removed and replaced by a new one. This rework can be performed using the method described in this section.

When performing the rework:

- In any rework, the PCB is heated. The thermal limits of PCB and components (e.g., MSL information) must be followed.
- During heating, the combination of rapid moisture expansion, materials mismatch, and material interface degradation can damage the component and PCB. To prevent moisture induced failures, it is recommended that the PCB assembly and components have had strict storage control with a controlled environment such as dry air or nitrogen. In addition, a pre-bake can help to remove the moisture.
- The influence of the heating on adjacent packages must be minimized. Do not exceed the temperature rating of the adjacent packages.
- Heating conditions will differ due to differences in the heat capacities of the PCB (board thickness, number of layers) and mounted components used; thus, the conditions must be set to correspond to the actual product and its mounted components.
- NXP follows industry-standard component level qualification requirements, which include three solder reflow passes. The three reflow passes simulate board level attach to a double-sided board and includes one rework pass.
- The removed PwrQFN package should be properly disposed of, so that it is not accidentally mixed with new components.

A typical PwrQFN rework flow process comprises seven stages:

1. Tooling preparation
2. Component removal
3. Site preparation
4. Solder paste printing
5. Component placement
6. Reflow soldering
7. Inspection

Individual process steps for reworking a QFN/SON package are described in subsequent sections.

NOTE

NXP product quality guaranty/warranty does not apply to products that have been removed, thus, component reuse should be avoided.

6.2.1 Tooling preparation

Various rework systems for SMD are available on the market. In general, the rework station should have a split light system, an XY table for alignment, and a hot air system with a top and bottom heater for component removal. For processing PwrQFN packages, a system should meet the requirements described in the following sections.

6.2.1.1 Heating system

The hot air temperature and the air flow must be controlled so that the component is heated in a targeted and controlled manner. The heating should be appropriate for the package size and thermal mass. PCB preheating from bottom side is recommended.

Infrared heating can be applied for preheating of the PCB, but it should only augment the hot air flow to the component side. Nitrogen can be used instead of air.

6.2.1.2 Vision system

The bottom side of the package as well as the site on the PCB should be observable. For precise alignment of the package to PCB, a split light system should be implemented.

Microscope magnification and resolution should be appropriate for the pitch of the device.

6.2.1.3 Moving and additional tools

Placement equipment should have good accuracy. In addition, special vacuum tools may be required to remove solder residue from PCB pads.

6.2.2 Component removal

If a component is suspected to be defective and is returned, no further defects must be introduced to the device during removal of the component from the PCB, because this may interfere with subsequent failure analysis. The following recommendations are intended to reduce the chances of damaging a component during removal.

6.2.2.1 Moisture removal

Dry bake components before removal at 125 °C for 16 to 24 hours for boards with SMT components, or at 95 °C for 16 to 24 hours for boards with temperature-sensitive components.

6.2.2.2 Temperature profile

During de-soldering, ensure that the package peak temperature is not higher and that the temperature ramps are not steeper than the standard assembly reflow process.

6.2.2.3 Mechanical

Do not to apply high mechanical forces for removal. High force can damage the component and/or the PCB, which may limit failure analysis of the package.

- For large packages, pipettes can be used (implemented on most rework systems)
- For small packages, tweezers may be more practical

If suspected components are fragile, then it is especially necessary to determine if they can be electrically tested directly after de-soldering, or if these components must be preconditioned prior to testing. In this case, or if safe removal of the suspected component is not possible (or too risky), the whole PCB (or the part of the PCB containing the defective component) should be returned.

An air nozzle of correct size should be used to conduct the heat to the QFN/SON component leads, so that a vacuum pick-up tool can properly remove the component (see Figure 39). The temperature setting for the top heater and the bottom heater depends on the component rating. A PCB bottom temperature setting of 150 °C is recommended. Many assembly sites have extensive in-house knowledge on rework, and their experts should be consulted for further guidance.

Figure 39. Package removal process

If the PCB is large, it is important to avoid bending of the printed circuit material due to thermal stress, so a bending prevention tool must be placed on the bottom of the printed circuit board, and a bottom heater installed (to allow heating of the entire printed circuit board, to raise work efficiency).

Reuse of removed semiconductor packages is not recommended.

6.2.3 Site preparation

After the component is removed, the PCB pads must be cleaned to remove solder residue, to prepare for the new component placement. This may be completed by vacuum de-soldering, solder sucker, solder wick braid, etc., after applying flux. Remaining solder residue and projections can cause the solder stencil to not closely adhere to the substrate during solder paste printing, leading to improper solder paste supply during component mount.

Moreover, when the solder residue flows all the way to an adjacent through-hole, the solder paste printed on the pad can be transferred via suction, to the through-hole during reflow, which may cause improper connection. A solvent may be necessary to clean the PCB of flux residue. A de-soldering station can be used for solder dressing. It should be noted that the applied temperature should not exceed the rating of PCB material which can contribute to pad peeling from the PCB. This is typically a manual operation that is directly attributed to experience and skill.

Non-abrasive or soft bristle brushes should be used as abrasive brushes (e.g., steel brushes) can contribute to bad solder joints. Before placing a new component on the site, solder paste should be applied to each PCB pad (by printing or dispensing). A no-clean solder paste is recommended.

6.2.4 Solder paste printing

Solder supply during rework is done using specialized templates and tools. A mini-stencil with the same stencil thickness, aperture opening, and pattern as the normal stencil are placed in the component site. A mini-metal squeegee blade deposits solder paste in the specific area (see Figure 40). The printed pad should be inspected, to ensure even and sufficient solder paste before component placement.

If neighboring parts are so close to the PwrQFN components that the mini-stencil method is not an option, then apply solder paste carefully on each component pad using a paste dispensing system. The volume of solder paste must be controlled, to prevent shorting on the component and/or neighboring components. Preferably, the same type of solder paste should be used as was originally applied on the board.

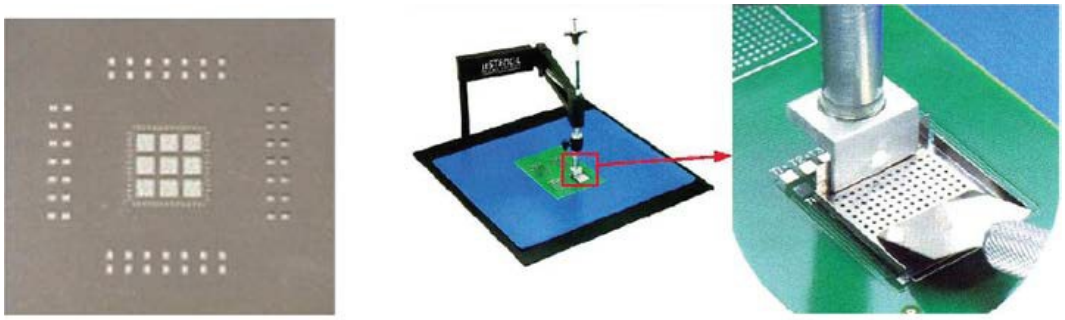


Figure 40. Mini-stencil and mini-squeegee

6.2.5 Component placement

The last step of the repair process is to solder the new semiconductor component on the board. When remounting the component, consider using rework equipment that has good optical or video vision capability. A split-light system displays images of both package leads and PCB pads by superimposing two images. Alignment of the leads and pads is completed with an adjusting XY which enables correct soldering (see Figure 41).

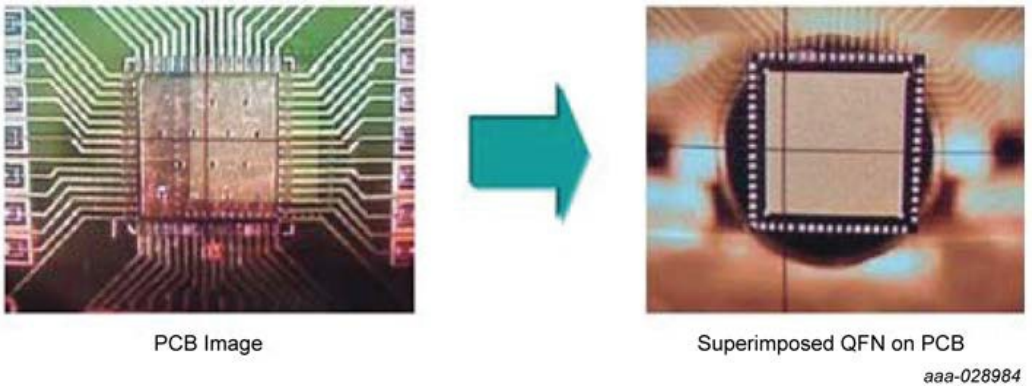


Figure 41. Split-light placement images

Regular lead array PwrQFN exhibits self alignment in any direction, including X-axis shift, Y-axis shift, and rotational misplacement. Exposed pads may not exhibit a strong self-alignment capability, so precise placement of the component on the PCB is required.

6.2.6 Reflow soldering

The new component is soldered to the PCB using the same temperature profile as the normal reflow soldering process (see Section Reflow soldering). During soldering, the package peak temperature and temperature ramps must not exceed those of the normal assembly reflow process. Note that it may be necessary to dry bake the board before it is exposed to reflow temperatures a second time.

The PCB might need to be cleaned if they do not get clean in the “normal” process, or if the rework was not done using “no clean” materials.

6.2.7 Inspection

To verify any open or short circuits (bridging) after soldering, optical inspection and x-ray inspection are recommended.

7 Board-level reliability

7.1 Solder joint reliability testing

Solder joint reliability (SJR) testing is performed to determine a measure of board level reliability when exposed to thermal cycling. The information provided here is based on experiments performed on a QFN/SON device using a daisy-chain bond configuration. Actual surface mount process and design optimizations are recommended to develop an application specific solution.

- For automotive grade product applications, NXP typically prefers to reach a minimum of 2000 cycles before first solder joint failure in SJR experiments. The widely accepted temperature range for testing is -40 °C to +125 °C.
- Consumer SJR temperature cycling conditions may vary widely, depending on the application and specific user. Typically, NXP consumer SJR testing is performed from 0° C to +100 °C.
- Table 4 shows the NXP standard test set-up for performing board-level solder joint reliability testing. Example of daisy-chain test PCB and QFN package is shown in Figure 42.

Table 4. Board-level reliability testing: Material and test setup

PCB board	1.58 mm thickness
	4 Cu layers
	OSP surface finish
Test board assembly	Pb-free solder paste (SAC387, SAC405, …)
	Reflow peak temperature for SAC assembly ~240 °C
	Pb solder paste Sn63Pb37
	Reflow peak temperature for SnPb assembly ~220 °C
	Stencil: 0.100 mm thickness, stainless steel, Ni plated, laser cut and electro-polished
Cycling conditions	Continuous in-situ daisy chain monitoring per IPC-9701 and IPC-SM-785
	Air temperature cycling (ATC) for automotive
	-40 °C to +125 °C
	15 minutes ramp/15 minutes dwell
	One hour cycle time
	ATC for commercial and industrial
	0 °C to +100 °C
	10 minutes ramp/10 minutes dwell
	40 minutes cycle time
Package test vehicle	Production bill of materials (BOM) package including die (die mechanically present, without wire bond connection)
	Daisy chain in package connecting pairs of terminal pads.

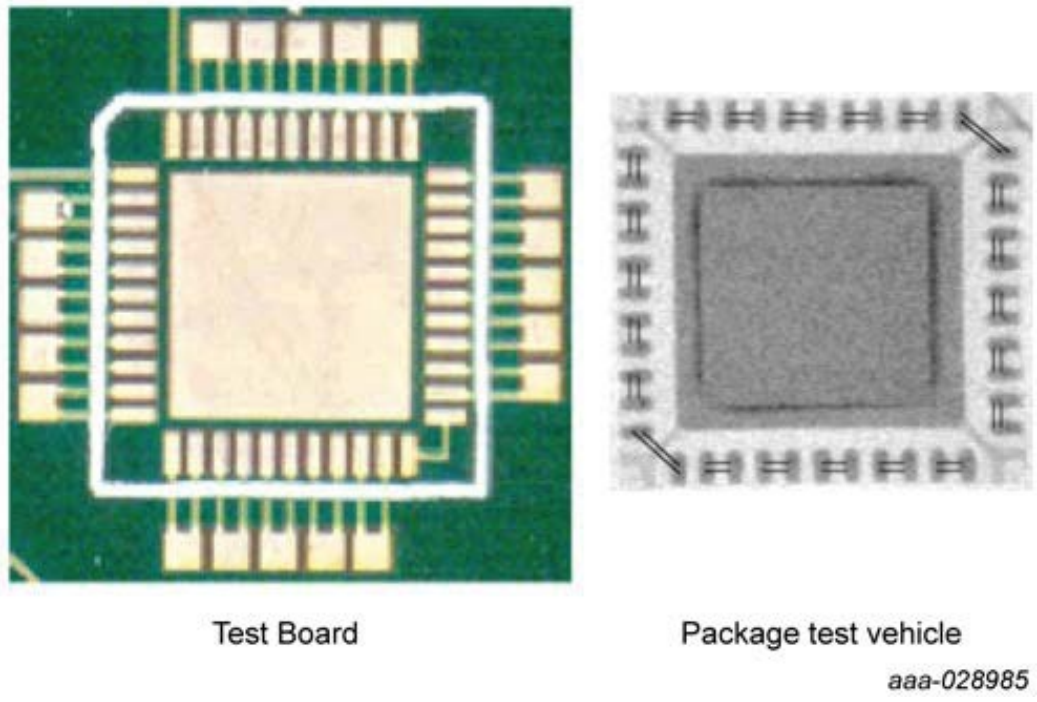


Figure 42. Daisy-chain test PCB and QFN package

7.2 Solder joint reliability results

NXP experimentally gathers board-level reliability data for a variety of packages. To get results from these experiments (including Weibull plots), contact the NXP sales team.

8 Package thermal characteristics

8.1 General thermal performance

Since the thermal performance of the package in the final application will depend on a number of factors (like board design, power dissipation of other components on the same board, ambient temperature), the thermal package properties provided by NXP should only serve as a reference. In applications where the thermal performance is considered to be critical, NXP recommends running application-specific thermal calculations in the design phase, to confirm the on-board thermal performance. NXP can generate so-called compact thermal models (CTM) of the specific product, that can be used in system level simulations. In order to obtain such a model please contact your NXP sales team.

Exposed pad packages may require the exposed pad to be connected to the PCB for thermal and/or electrical measurement. For optimized thermal performance, it is recommended to form a thermal pass into the PCB, by connecting the exposed pad to the top and/or bottom and/or inner copper layers of the PCB. The PCB copper area and number of thermal vias connected to the exposed pad required to achieve the proper thermal performance on the PCB is application specific, and depends on the package power dissipation and the individual board properties (thermal resistance of the application PCB).

8.2 Package thermal characteristics

Junction temperature is a function of die size, on-chip power dissipation, package characteristics, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal technology.

Additional factors to be considered in PCB design and the thermal rating of the final application (amongst others) are:

- Thermal characteristics of the PCB (metal density, number of thermal vias, thermal conductivity of thermal vias)

- Quality and size of PCB solder joints (effective PCB pad size, potential solder voiding in the thermal path solder joints that may reduce the effective solder area)

The stated values are meant to define the package thermal performance in a standardized environment (one package on a standardized board).

Thermal properties of the individual products are usually given in the NXP product data sheets as appropriate. Product data sheets are available at http://www.nxp.com. For more details on thermal properties, contact NXP.

8.3 Package thermal properties definition

The thermal performance of PwrQFN packages with and without exposed pads is typically specified by thermal properties such as $R_{\theta JA}$, $R_{\theta JC}$ and Ψ_{JT} (in °C/W). Thermal characterization is performed by physical measurement and by running complex simulation models under the following conditions:

- One thermal board type:
  - Four-layer board (2s2p), per JEDEC JESD51-7 and JESD51-5 (exposed pad packages only)
- Two boundary conditions:
  - Natural convection (still air), per JEDEC JESD51-2
  - Cold plate method, per MIL SPEC-883 method 1012.1

8.3.1 RθJA: Theta junction-to-ambient natural convection (still air)

Junction-to-ambient thermal resistance (Theta-JA or $R_{\theta JA}$ per JEDEC JESD51-2) is a one-dimensional value that measures the conduction of heat from the junction (of the hottest temperature on die) to the environment (ambient) near the package in a still air environment. The heat that is generated on the die surface reaches the immediate environment along two paths:

- Convection and radiation off the exposed surface of the package, and
- Conduction into-and-through the test board, followed by convection and radiation off the exposed board surfaces.

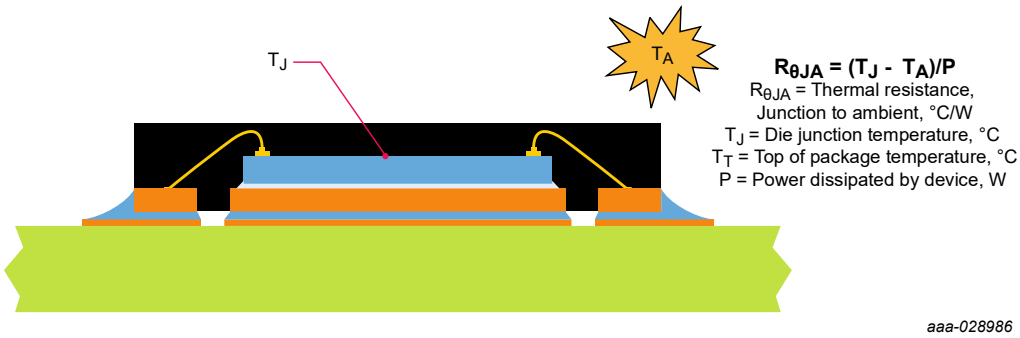


Figure 43. Junction and ambient temperature (still air)

8.3.2 RθJC: Theta junction-to-case

Junction-to-case thermal resistance (Theta-JC or $R_{\theta JC}$ per MIL SPEC-883 Method 1012.1) indicates the average thermal resistance between the die and the case top surface, as measured by the cold plate method per MIL SPEC-883 Method 1012.1, with the cold plate temperature used for the case temperature. The case temperature is defined as

- Either the temperature at the top of the package (for non-exposed pad packages), or
- The temperature at the bottom of the exposed pad surface (for exposed pad packages).

For exposed pad packages where the pad would be expected to be soldered, the junction-to-case thermal resistance is a simulated value from the junction to the exposed pad without contact resistance. $R_{\theta JC}$ can be used to estimate the thermal performance of a package when the board is adhered to a metal housing or heat sink, or when a complete thermal analysis is done.

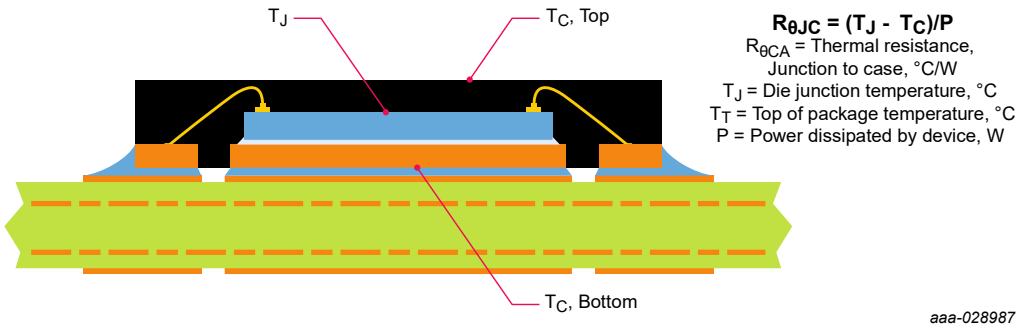


Figure 44. Junction and case temperatures (top and bottom side)

8.3.3 ΨJT (Psi JT): Junction-to-package top

Junction-to-package top (Psi JT or Ψ_{JT}) indicates the temperature difference between the package top and the junction temperature, optionally measured in a still air condition (per JEDEC JESD51-2) or in a forced convection environment (per JEDEC JESD51-6). Ψ_{JT} must not be confused with the parameter $R_{\theta JC}$: $R_{\theta JC}$ is the thermal resistance from the device junction to the external surface of the package, with the package surface held at

a constant temperature, while Ψ_{JT} is the value of the temperature difference between the package surface and the junction temperature, usually in natural convection.

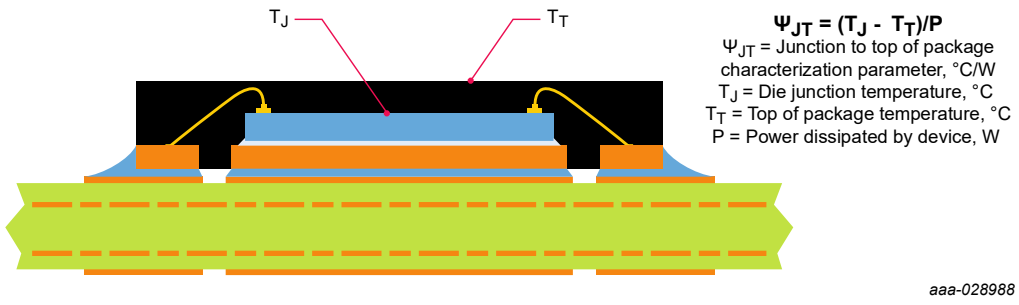


Figure 45. Junction and package top temperatures

8.4 Example of package thermal properties

Table 5 shows an example of the thermal characteristics typically shown in a NXP product data sheet. The example applies to a PwrQFN package size 12.0 mm x 12.0 mm x 2.1 mm, ~5.0 mm x 7.5 mm exposed pad, pitch 0.9 mm, die size ~ 4.5 mm x 7.0 mm.

NOTE

NXP gathers all thermal data for a variety of packages. To obtain thermal properties (such as $R_{\theta JA}$, $R_{\theta JC}$, and Ψ_{JT}) for a specific package, contact the NXP sales team.

Table 5. Thermal parameters of a PwrQFN 12 x 12 package

Rating	Board type	Parameter	Value	Unit	Notes
Junction-to-ambient (natural convection)	Four-layer board (2s2p)	RθJA	24.5	°C/W	1 2
Junction-to-Board		RθJB	4.0	°C/W	3
Junction-to-case (bottom/ exposed pad)		RθJC	0.13	°C/W	4

Table continues on the next page...

Table 5. Thermal parameters of a PwrQFN 12 x 12 package (continued)

Rating	Board type	Parameter	Value	Unit	Notes
Junction to Case (Top)		RθJC	11.5	°C/W	5
Junction-to-package-top	Natural convection	ΨJT	0.5	°C/W	6

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board temperature) ambient temperature air flow power dissipation of other components on the board, and the thermal resistance.
2. Per JEDEC JESD51-6 with the board (JESD51-7) horizontal.
3. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
4. Thermal resistance between the die and the exposed pad surface as measured by the cold plate method (MIL Spec-883 Method 1012.1).
5. Thermal resistance between the die and the package top surface as measured by the cold plate method (MIL Spec-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

9 Downloading package information from NXP website

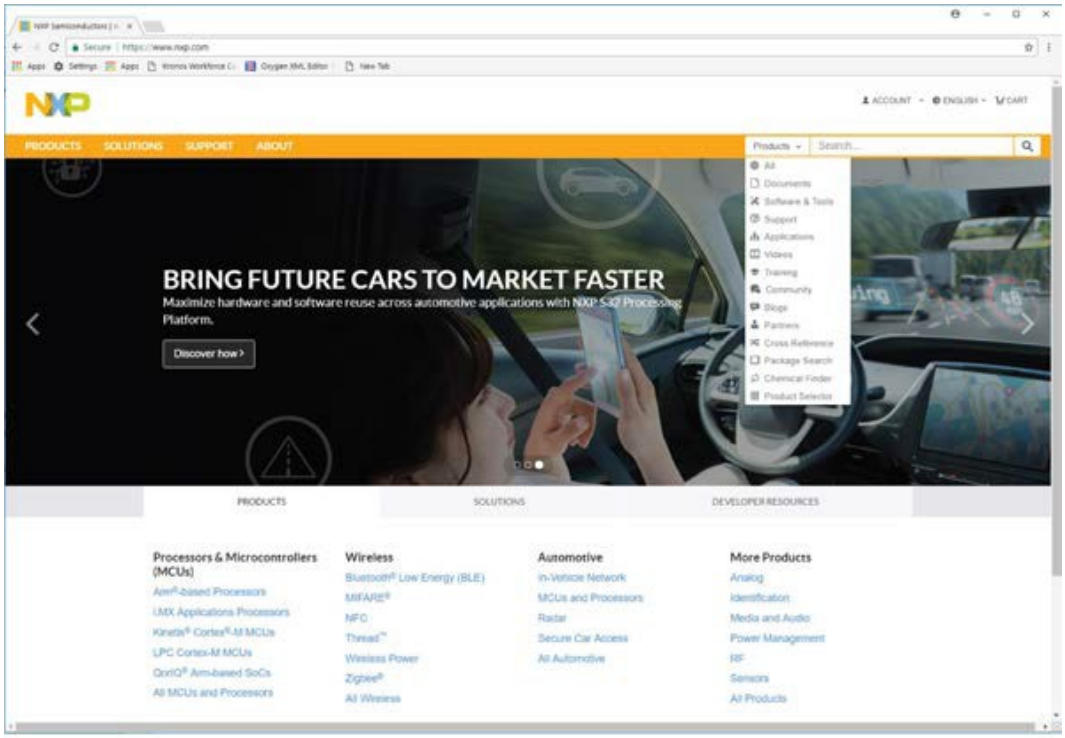
9.1 Performing a product search on NXP website

The package outline drawing and the material composition declaration sheet (MCD, in IPC-1752 reporting format) can be downloaded from the NXP website. Information on product specific moisture sensitivity levels (MSL) is available on the website, too. Note that the website screen appearance is regularly changed and may look different from the one shown in this section. However, the general procedure described should mostly apply.

To download the documents:

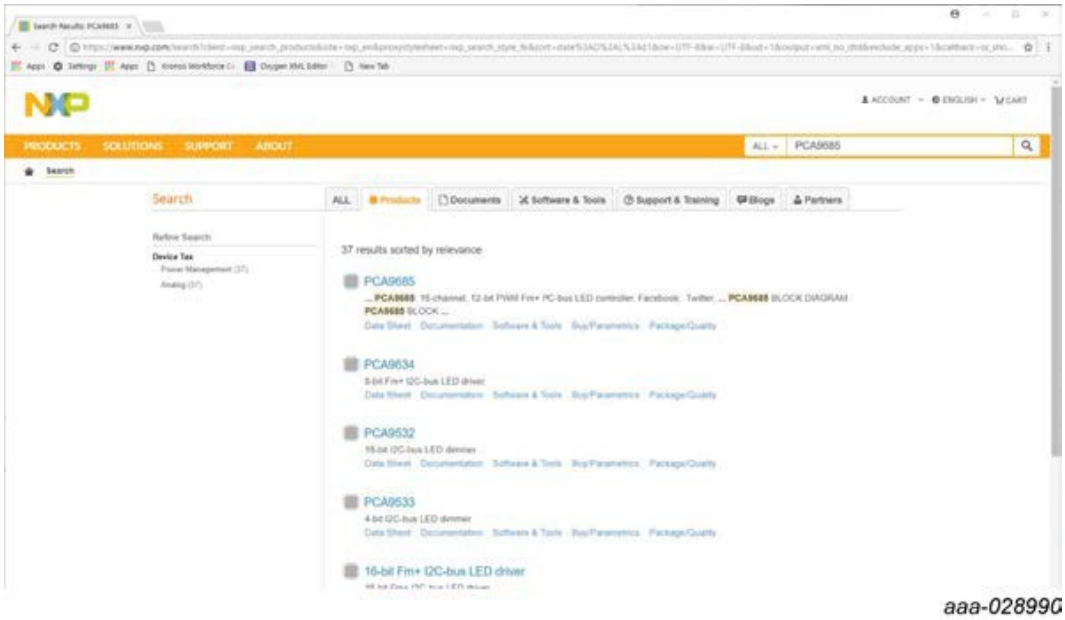
- Go to www.nxp.com.

- In the text box on the upper right of the screen, click and select “Products” from the drop-down menu.



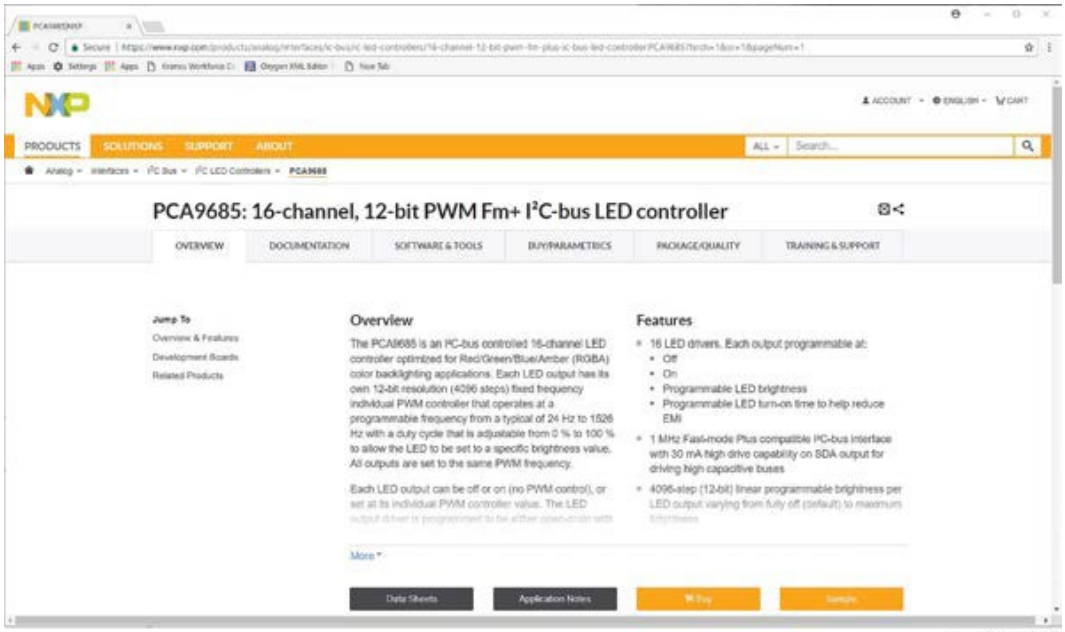
aaa-028989

- Enter the NXP product part number in the “Search …” box.



aaa-028990

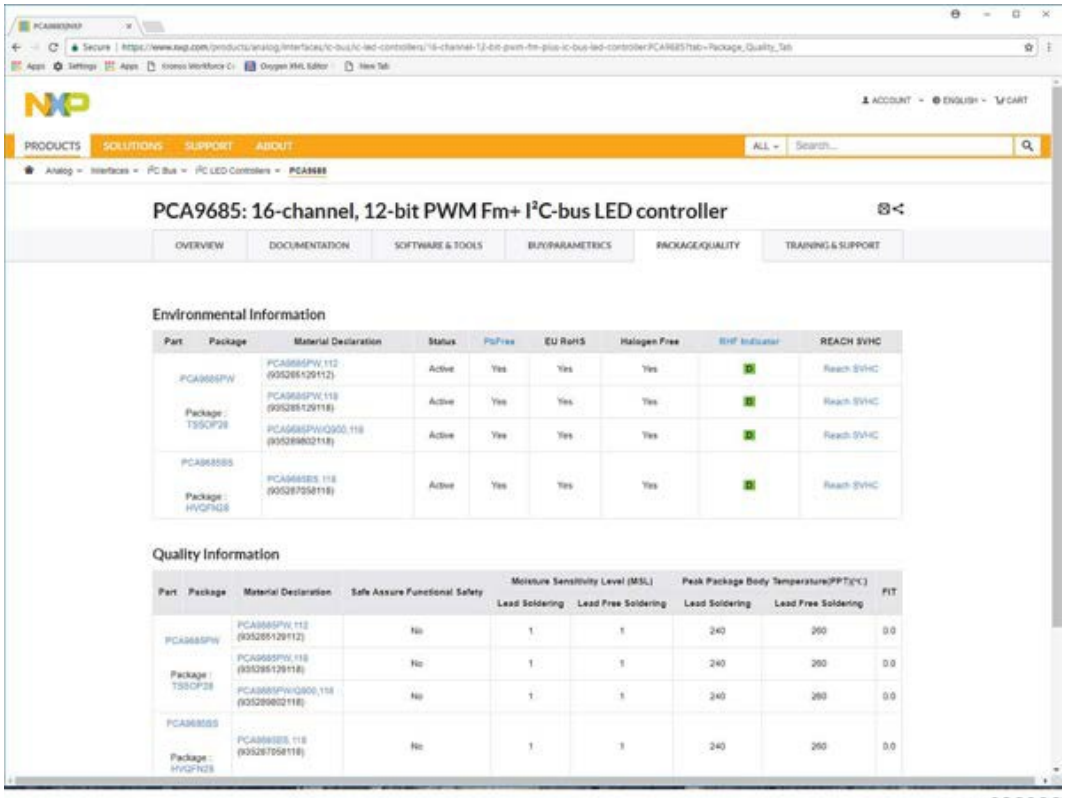
- The next screen returns search results, and lists all part numbers and documents related to the search term.
- On the search results screen, select the desired part number.
- The next screen shows the “Product Overview Page” with information on Product Documentation, Software & Tools, Buy/Parametric, Package/Quality, Training & Support.



aaa-028991

9.2 Retrieving package outline drawing, MCD and MSL rating

- Click on the “Package/Quality” tab to view environmental and quality information



aaa-028992

Environmental Information

Part	Package	Material Declaration	Status	PbFree	EU RoHS	Halogen Free	RHF Indicator	REACH SVHC
PCA9685PW	Package : TSSOP28	PCA9685PW,112 (935285129112)	Active	Yes	Yes	Yes	D	Reach SVHC
		PCA9685PW,118 (935285129118)	Active	Yes	Yes	Yes	D	Reach SVHC
		PCA9685PW/Q900,118 (935289802118)	Active	Yes	Yes	Yes	D	Reach SVHC
PCA9685BS	Package : HVQFN28	PCA9685BS,118 (935287058118)	Active	Yes	Yes	Yes	D	Reach SVHC

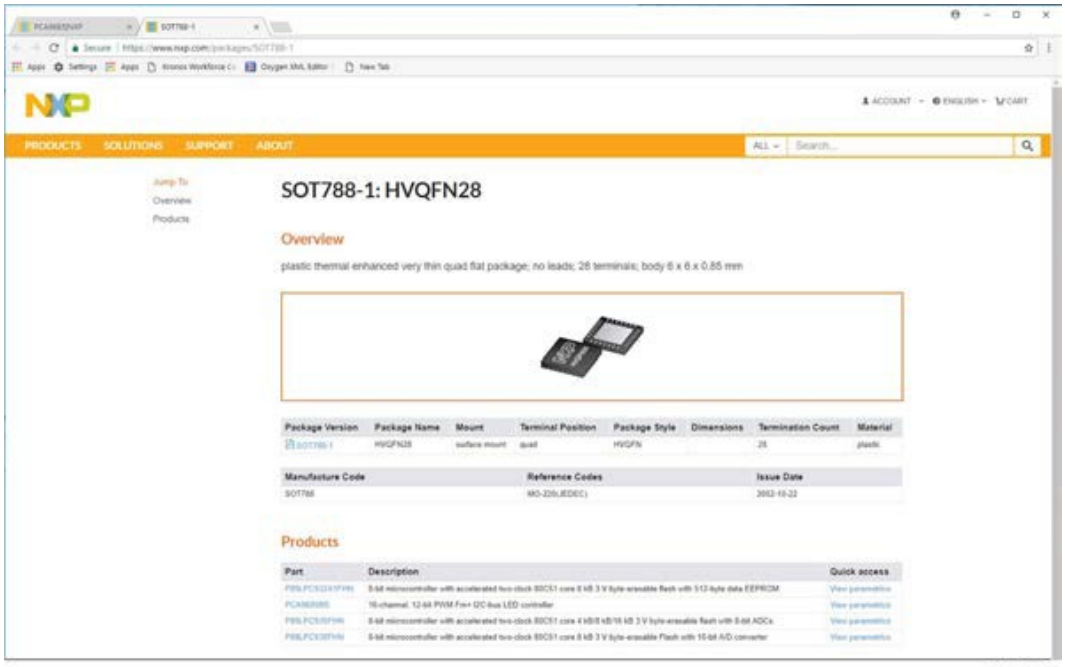
aaa-028993

Quality Information

Part	Package	Material Declaration	Safe Assure Functional Safety	Moisture Sensitivity Level (MSL)		Peak Package Body Temperature(PPT)(℃)		FIT
				Lead Soldering	Lead Free Soldering	Lead Soldering	Lead Free Soldering	
PCA9685PW	Package : TSSOP28	PCA9685PW,112 (935285129112)	No	1	1	240	260	0.0
		PCA9685PW,118 (935285129118)	No	1	1	240	260	0.0
		PCA9685PW/Q900,118 (935289802118)	No	1	1	240	260	0.0
PCA9685BS	Package : HVQFN28	PCA9685BS,118 (935287058118)	No	1	1	240	260	0.0

aaa-028994

- Click on the “Material Declaration” link to go to the “Chemical Content” site. Material information is displayed. MCD sheet can be downloaded in XLS, XLM, and PDF format.

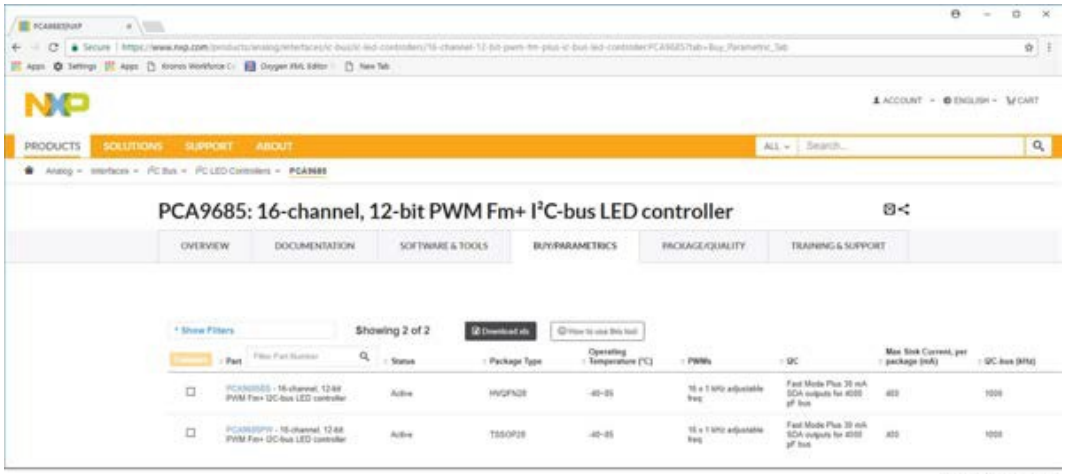


aaa-028995

- Click the “Package” link to go to the “Package Overview” site. Package information is displayed. PDF file with package outline drawing can be downloaded.

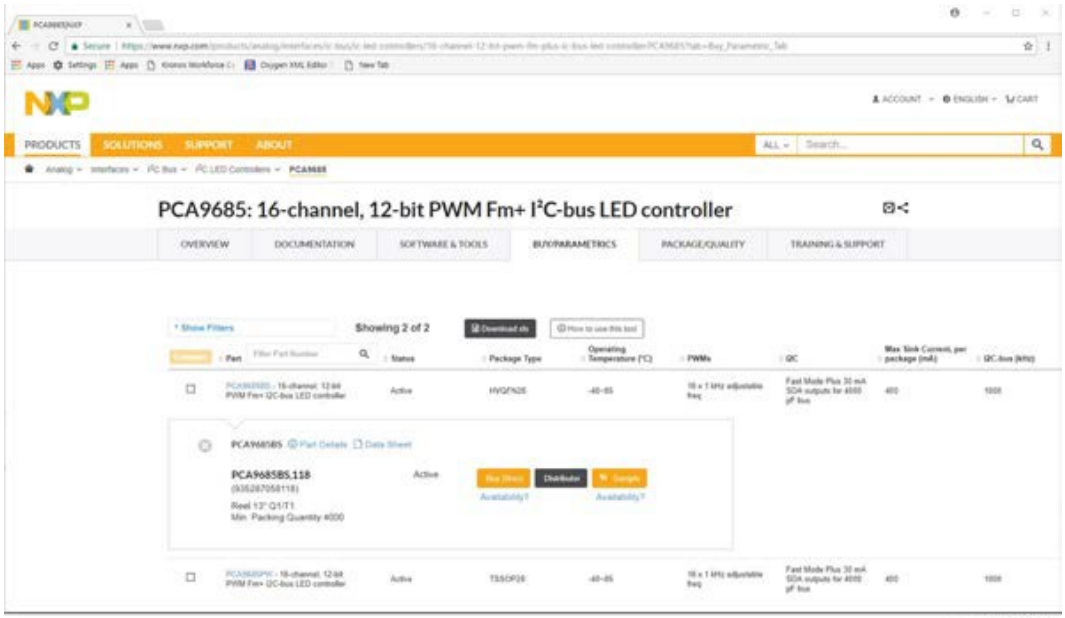
9.3 Retrieving the packing information for the product

- Click on the “Buy/Parametrics” tab on the “Product Overview Page” to view available product options



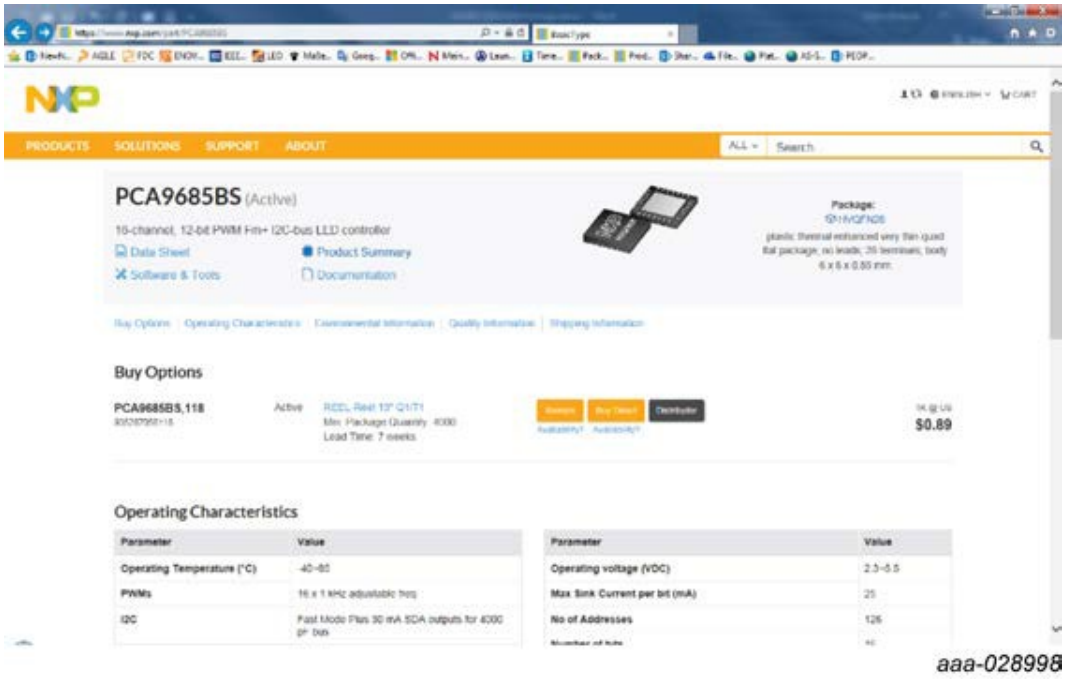
aaa-028996

- Select the preferred part number from the list and click on the link to view details of the part number.



aaa-028997

- Click on the “Parts Detail” link to show the product details view.



- Find the link to the Packing Information next to the product number and download the PDF file.

10 Package handling

10.1 Handling of ESD sensitive devices

Semiconductor integrated circuits (ICs) and components are electrostatic discharge sensitive (ESDS) devices, so proper precautions are required for handling and processing them. Electrostatic discharge (ESD) is one of the significant factors leading to damage and failure of semiconductor ICs and components, and comprehensive ESD controls to protect ESDS devices during handling and processing should be considered.

The following industry standards describe detailed requirements of proper ESD controls; NXP recommends meeting the standards before handling and processing ESDS devices. Detailed ESD specifications of devices are available in each device data sheet.

- JEDEC JESD625: Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices
- IEC-61340-5-1: Protection of electronic devices from electrostatic phenomena - General requirements

10.2 Handling of moisture-sensitive surface mount devices

Some SON/QFN packages are moisture sensitive surface mount devices (SMD) and proper precautions are required for handling, packing, shipping and use.

Moisture from atmospheric humidity enters permeable plastic package materials by diffusion. When the package is exposed to rapid temperature rise and high temperature during reflow solder process, moisture expansion, materials mismatch, and material interface degradation can result in package cracking and/or de-lamination of critical interfaces (“popcorn” effect).

Therefore, moisture-sensitive components are dried and sealed in a moisture barrier bags (MBB) before shipping per IPC/JEDEC J-STD-033. The components are stored together with a desiccant and a moisture indicator card in the vacuum sealed bag. Only remove the moisture-sensitive components immediately prior to assembly onto the PCB. If partial lots are used, the remaining SMD packages must be resealed or placed in safe storage within one hour of bag opening.

A label on the moisture barrier bag (MBB) indicates that it contains moisture sensitive components (Figure 46). The “Moisture Sensitivity Caution Label” contains information about the moisture sensitivity level (MSL) and maximum allowed peak body temperature of the products. Same information is shown on the barcode labels of the shipping box and reels.

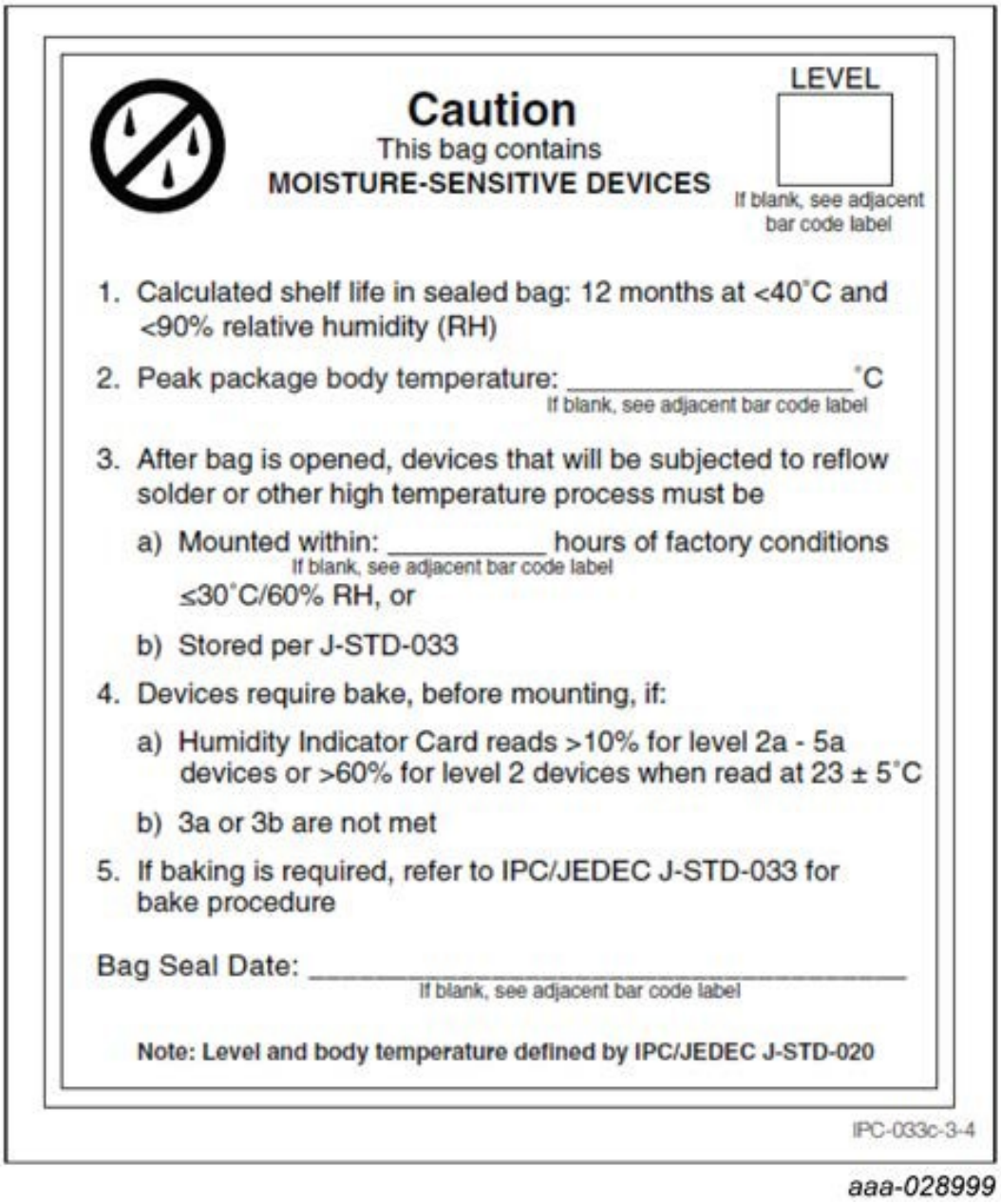


Figure 46. Example of moisture-sensitive caution label (IPC/JEDEC J-STD-033)

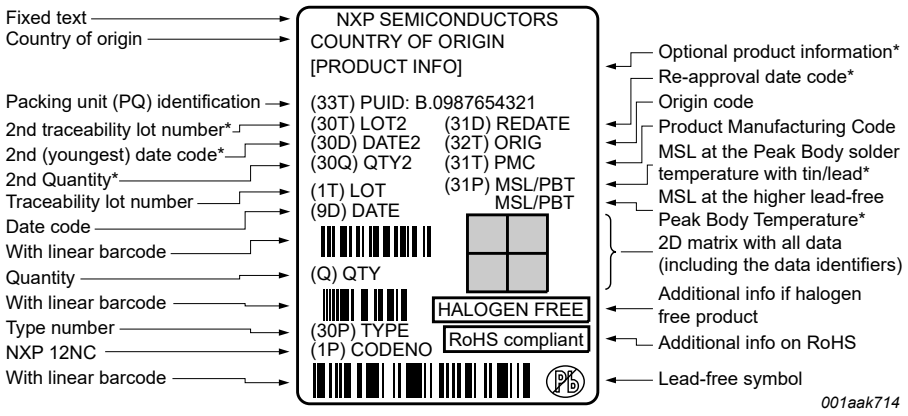


Figure 47. Example of typical box and reel information barcode label

The MSL indicates the floor life of the component, its storage conditions, and handling precautions after the original container has been opened. The permissible time, from opening the moisture barrier bag until the final solder reflow process, that a component can remain outside the moisture barrier bag is a measure of the sensitivity of the component to ambient humidity.

Table 6 presents the floor life definitions per IPC/JEDEC J-STD-033. Components must be mounted and reflowed within the allowable period of time (floor life out of the bag), and component temperature must not exceed the maximum peak body temperature during reflow process at the customer's facility.

Table 6. Moisture classification level of floor live (IPC/JEDEC J-STD-033)

Moisture sensitivity level	Floor life (out of bag) at factory ambient ≤ 30 °C/60 % RH or as stated
1	Unlimited at ≤ 30 °C/85 % RH
2	1 Year
2a	4 Weeks
3	168 Hours
4	72 Hours
5	48 Hours
5a	24 Hours
6	Mandatory bake before use. After bake, must be reflowed within the limit specified on the label.

Upon opening the MBB, the floor-life clock starts. If components have been exposed to ambient air for longer than the specified time, or if the humidity indicator card indicates too much moisture after opening a moisture barrier bag, then the components are required to be rebaked prior to the assembly process. Refer to IPC/JEDEC J-STD-033 for bake procedure.

10.3 Packing of devices

PwrQFN devices are contained in tray or tape and reel configurations. The packing media are design to protect devices from electrical, mechanical and chemical damages (as well as moisture absorption).

Devices are shipped with dry packing or non-dry packing depending on the MSL level of the device per IPC/JEDEC J-STD-033 (Table 7). Moisture sensitive devices are dry packed for transportation and storage with a vacuum sealed moisture barrier bag, including a desiccant and a moisture indicator card (refer to Section Handling of moisture-sensitive surface mount devices). MSL1

components do not require dry packing, but for devices with Sulphur sensitive Au/Ag plating alloy NXP is using a Sulphur barrier pack to protect the device also from airborne Sulphur contamination.

Proper handling and storage of dry packs are recommended. Improper handling and storage (dropping dry packs, storage exceeding 40 °C/90 % RH environment, excessive stacking of dry packs, etc.) will increase various quality and reliability risks.

Table 7. Dry packing requirements (IPC/JEDEC J-STD-033)

MSL level	Dry before bag	MBB with HIC	Desiccant	MSID label	Caution label
1	Optional	Optional	Optional	Not Required	Not required if classified at 220 to 225 °C Required if classified at other than 220 to 225 °C
2	Optional	Required	Required	Required	Required
2a to 5a	Required	Required	Required	Required	Required
6	Optional	Optional	Optional	Required	Required

- MBB: Moisture barrier bag
- HIC: Humidity indicator card
- MSID: Moisture sensitive identification

The packing method, product orientation, dimensions, and labels are described in the Packing Information document. This document can be downloaded from NXP's website at the Buy Options for each device. The different packing methods are also indicated by the ending of either the orderable part number (3-digit number or single letter), or the ending of the ordering code (3-digit number).

NOTE

Packing information can be found on NXP's website following the steps described in Section Retrieving the packing information for the product

NXP complies with following environmental standards conformance guidelines/directives:

- ISPM 15, Guidelines for Regulating Wood Packaging Material in International Trade.
- European Parliament and Council Directive 94/62/EC of 20 December 1994, packaging and packaging waste.

10.3.1 Trays

- NXP complies with standard JEDEC tray design configuration (see Figure 48).
- Devices will be oriented with pin 1 toward the chamfered corner of the tray.
- Trays are designed to be baked for moisture-sensitive SMDs, but the temperature rating of tray should NOT be exceeded when the devices are baked. The temperature rating can be found on the end-tab of the tray. The recommended baking temperature of trays is 125 °C.
- Trays are typically banded together with 5 + 1 (five fully-loaded trays and one cover tray) stacking, and dry packed in a moisture barrier bag (MBB). Partial stacking (1 + 1, 2 + 1, etc.) is also available, depending on individual requirements.

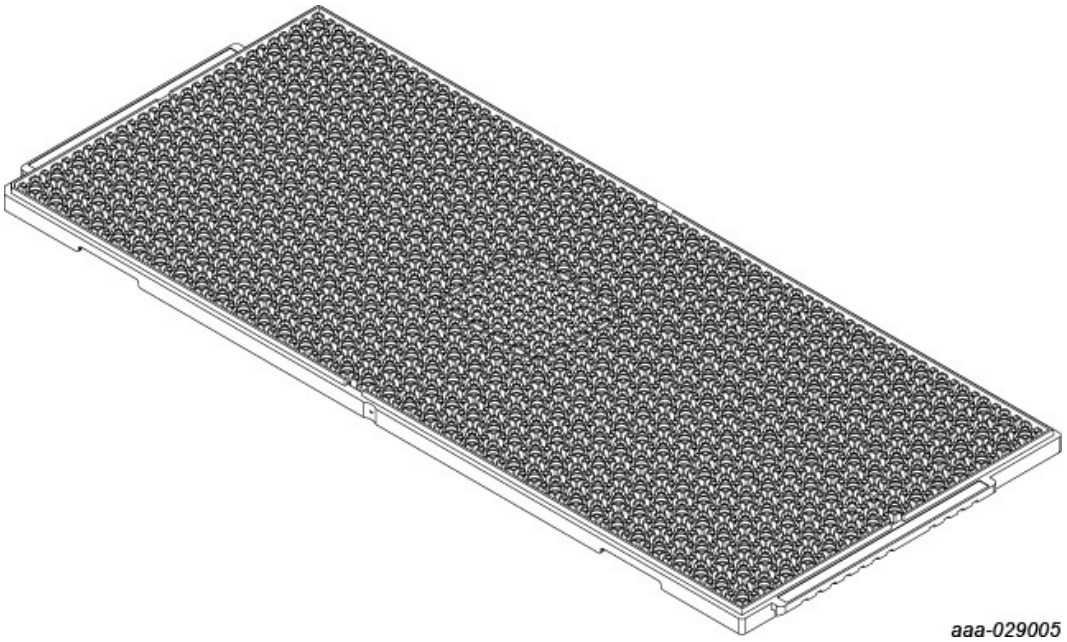


Figure 48. JEDEC tray example

10.3.2 Tape and reel

- NXP tape and reel carriers are in accordance with ANSI/EIA-481 (Figure 49).
- The packing information document (which can be either in PDF format or Excel table format) provides detail information on:
  - Packing method
  - Reel dimensions (Figure 52 and Table 9).
  - Packing quantity
  - Product pin 1 orientation
  - Carrier tape dimensions and tolerances (Figure 51 and Table 8)
- The product pin 1 orientation in the carrier tape (Figure 50) follows the orientation guide of ANSI/EIA-481 standard, but exceptions are possible depending on the product characteristics. Refer to the Buy Options on NXP's website to confirm the individual product orientation.
- Tape and reels are NOT designed to be baked at high temperatures.
- Each tape and reel is typically dry packed in a moisture barrier bag.

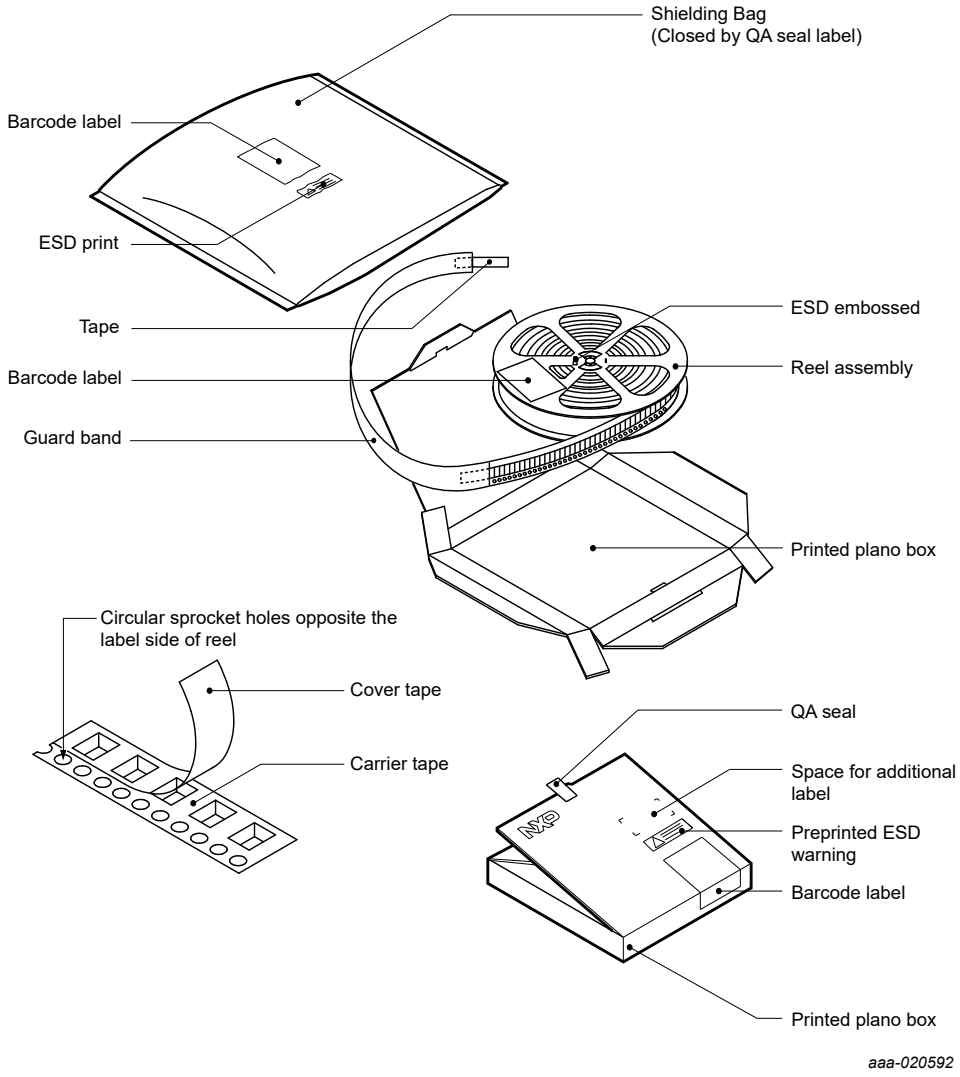


Figure 49. Typical reel pack for SMD: Guard band, ESD shielding bag

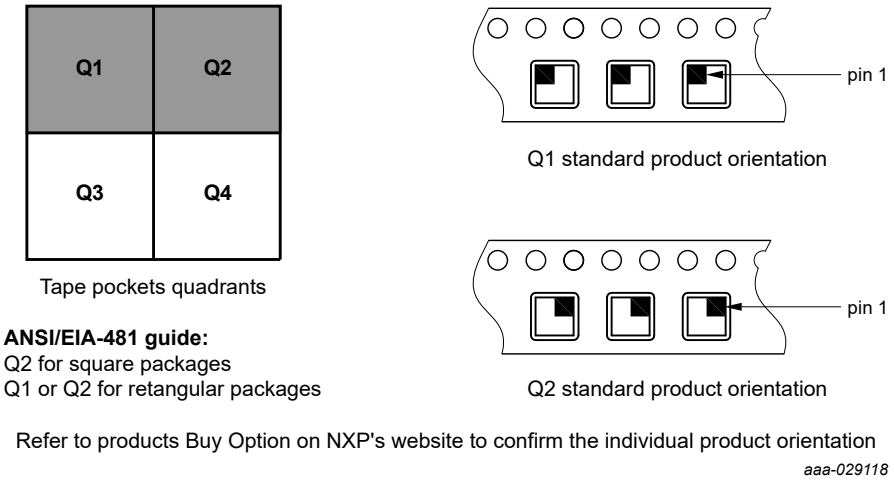


Figure 50. Product orientation in carrier tape

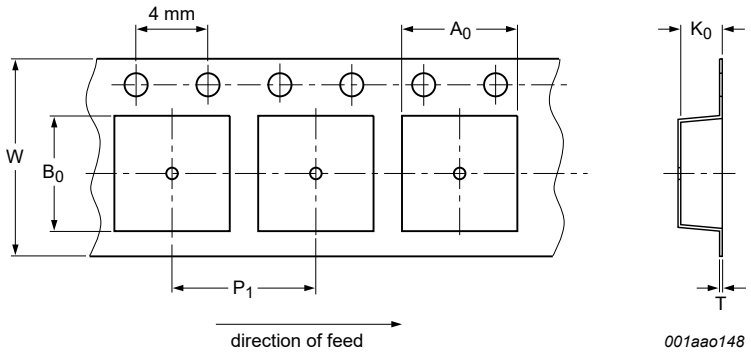


Figure 51. Example of carrier tape dimensions (in accordance with IEC 60286-3)

Table 8. Example of carrier tape dimensions

A_g (mm)	B_g (mm)	K_g (mm)	T (mm)	P_1 (mm)	W (mm)
2.30 ± 0.10	2.30 ± 0.10	0.75 ± 0.10	0.30 ± 0.05	4.0 ± 0.1	0.80 ± 0.3

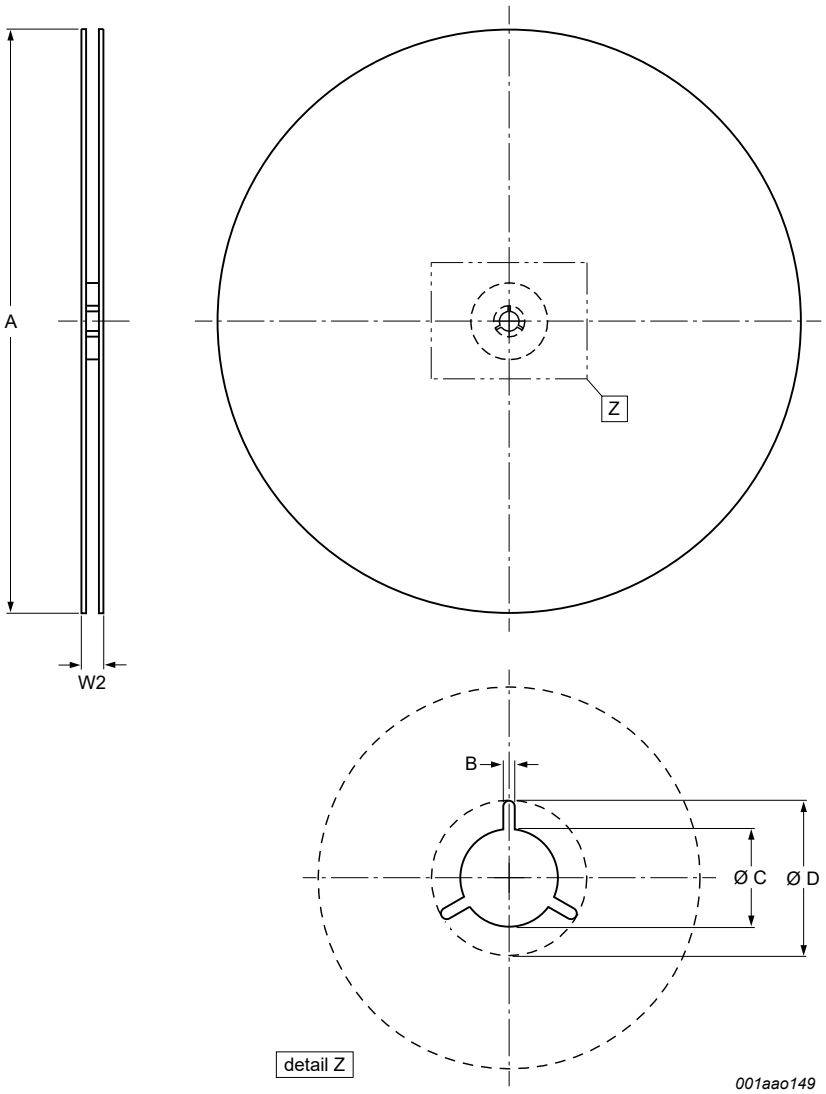


Figure 52. Schematic view of reel

Table 9. Reel dimensions (in accordance with IEC 60286-3)

A [nom] (mm)	W2 (mm)	B [min] (mm)	C [min] (mm)	D [min] (mm)
180 (7”)	Depending on tape width	1.5	12.8	20.2
330 (13”)				

11 References

1. JEDEC MO-220, Thermally Enhanced Plastic Very Thin and Very Very Thin Fine Pitch Quad Flat No Lead Package
2. JEDEC MO-229, Thermally Enhanced Plastic Very Thin, Very Very Thin and Ultra Thin Fine Pitch Small Outline No Lead Package
3. IEC 60286-3, Packaging of components for automatic handling. Part 3: Packaging of surface mount components on continuous tapes

4. JESD51-2, Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air)
5. JESD51-3, Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
6. JESD51-5, Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms
7. JESD 51-6, Integrated Circuits Thermal Test Method Environment Conditions – Forced Convection (Moving Air)
8. JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages, February 1999
9. JESD51-7, High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages
10. JESD51-8, Integrated Circuit Thermal Test Method Environmental Conditions – Junction-to-Board, October 1999
11. IPC/JEDEC J-STD-020, Moisture/reflow sensitivity classification for nonhermetic surface mount devices
12. IPC/JEDEC J-STD-033, Handling, packing, shipping, and use of moisture/reflow sensitive surface-mount devices
13. MIL-STD-883, Method 1012.1 Thermal Characteristics
14. IPC-7351B, Generic Requirements for Surface Mount Design and Land Pattern Standards
15. IPC-7093, Design and Assembly Process Implementation for Bottom Termination SMT Components
16. IPC, J-STD-004, Requirements for Soldering Fluxes
17. IPC, J-STD-005, Requirements for Soldering Pastes
18. IPC, J-STD-006, Requirements for Electronic Grade Solder Alloys
19. ANSI/EIA-481, 8 mm Through 200 mm Embossed Carrier Taping and 8 mm & 12 mm Punched Carrier Taping of Surface Mount Components for Automatic Handling

12 Revision history

Table 10. Revision history

Rev	Date	Description
v.6	20200120	Rewrote and transform to new format AN2467 and revise to NXP name.

How To Reach Us

Home Page:

nxp.com

Web Support:

nxp.com/support

Limited warranty and liability — Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. “Typical” parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including “typicals,” must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: nxp.com/SalesTermsandConditions.

Right to make changes - NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Security — Customer understands that all NXP products may be subject to unidentified or documented vulnerabilities. Customer is responsible for the design and operation of its applications and products throughout their lifecycles to reduce the effect of these vulnerabilities on customer’s applications and products. Customer’s responsibility also extends to other open and/or proprietary technologies supported by NXP products for use in customer’s applications. NXP accepts no liability for any vulnerability. Customer should regularly check security updates from NXP and follow up appropriately. Customer shall select products with security features that best meet rules, regulations, and standards of the intended application and make the ultimate design decisions regarding its products and is solely responsible for compliance with all legal, regulatory, and security related requirements concerning its products, regardless of any information or support that may be provided by NXP. NXP has a Product Security Incident Response Team (PSIRT) (reachable at PSIRT@nxp.com) that manages the investigation, reporting, and solution release to security vulnerabilities of NXP products.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: December 2020
Document identifier: AN2467