Freescale Semiconductor
Application Note

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Hardware and Layout Design Considerations for DDR Memory Interfaces

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Embedded systems that use double data rate memory (DDR) can realize increased performance over traditional single data rate (SDR) memories. As the name implies, DDR enables two data transactions to occur within a single clock cycle without doubling the applied clock or without to doubling the size of the data bus. This increased data bus performance is due to source-synchronous data strobes that permit data to be captured on both the falling and rising edges of the strobe.

Although DDR can bring improved performance to an embedded design, care must be observed in the schematic and layout phases to ensure that desired performance is realized. Smaller setup and hold times, cleaner reference voltages, tighter trace matching, new I/O (SSTL-2) signaling, and the need for proper termination can present the board designer with a new set of challenges that were not present for SDR designs.

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Design challenges confronting the board designer can be summarized as follows:

- Routing requirements
- Power supply and decoupling, which includes the DDR devices and controller, the termination rail generation (V_{TT}), and reference generation (V_{REF})
- Proper termination for a given memory topology

This application note provides several layout considerations within these areas and includes recommendations that can serve as an initial baseline for board designers as they begin specific implementation, which can consist of the following:

- Single or multi-DIMM—registered, unbuffered
- Single or multi SO-DIMM—registered, unbuffered
- Soldered-down discrete implementation
- Mixture—discretes plus DIMM expansion slots

Besides memory, composite memory topologies can also include on-board logic analyzer connections and expansion DIMM cards with analyzer connections.

The design guidelines in this document apply to PowerQUICC™ products that leverage the DDR IP core and are based on a compilation of internal platforms designed by Freescale. These guidelines minimize board-related issues across multiple memory topologies while allowing maximum flexibility for the board designer. Because numerous memory topologies and interface frequencies are possible on the DDR interface, Freescale highly recommends that the board designer verify, through simulation, all aspects (signal integrity, electrical timings, and so on) before PCB fabrication. Also, be sure to consult the latest errata. Any AC timing parameters within this document are for reference purposes only. The designer should consult the official AC specifications for a given product.

1 SSTL-2 and Termination

For DDR-I memories, JEDEC created and adopted a low voltage, high-speed signaling standard called series stub termination logic (SSTL). SSTL leverages an active motherboard termination scheme and overcomes the signal integrity concerns with legacy LVTTL signaling. As the name implies, SSTL is suited for use in mainstream memory interfaces where stubs and connectors are present. The 2.5 V version, named SSTL-2, is prominent with DDR1 memories and is defined within JESD8-9B. The memory controller s drivers and receivers are compatible.with SSTL-2.

The most common SSTL termination is the class II single and parallel termination scheme shown in Figure 1. This scheme involves using one series resistor (R_S) from the controller to the memory and one termination resistor (R_T) attached to the termination rail (V_{TT}). This approach is used in commodity PC motherboard designs. Values for R_S and R_T are system-dependent and should be derived by board simulation. See Section 12, “Simulation,” for a list of potential termination ranges. Use of the mainstream termination in commodity PC motherboards is assumed in this document. Consequently, differing termination techniques can be valid and useful, but the designer should use simulation to validate this determination.

In a typical memory topology, the series damping resistor (R_S), if used, is placed away from the controller. This approach has two distinct advantages. It frees precious board space around the memory controller,

avoiding layout congestion and burdensome fanout. Also, it optimizes the signal integrity for the signals sent from the controller to the memories, where more signals (addr + cmd) must be reliably received by multiple devices.

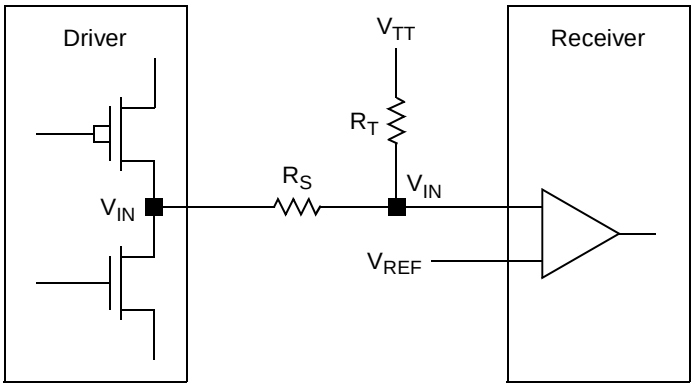

Figure 1. Typical Memory Interface Using Class II Option

To realize the increased signaling frequencies, SSTL leverages high-gain differential receivers that are biased around a reference voltage denoted as V_{REF}. Using these receivers allows a smaller voltage swing, reducing signal reflections, lowering EMI, improving settling time, and yielding higher possible clock rates than with LVTTL signaling. Figure 2 shows the SSTL interface levels. The AC logic levels are the points at the receiver where the AC input timing parameters (setup and hold) must be satisfied. The DC logic levels provide a point of hysteresis. When the input level crosses the DC reference point, the receiver switches to the new logic level and maintains this new state as long as the signal does not cross below the threshold. Consequently, SSTL buses are less susceptible to overshoot, undershoot, and ringing effects.

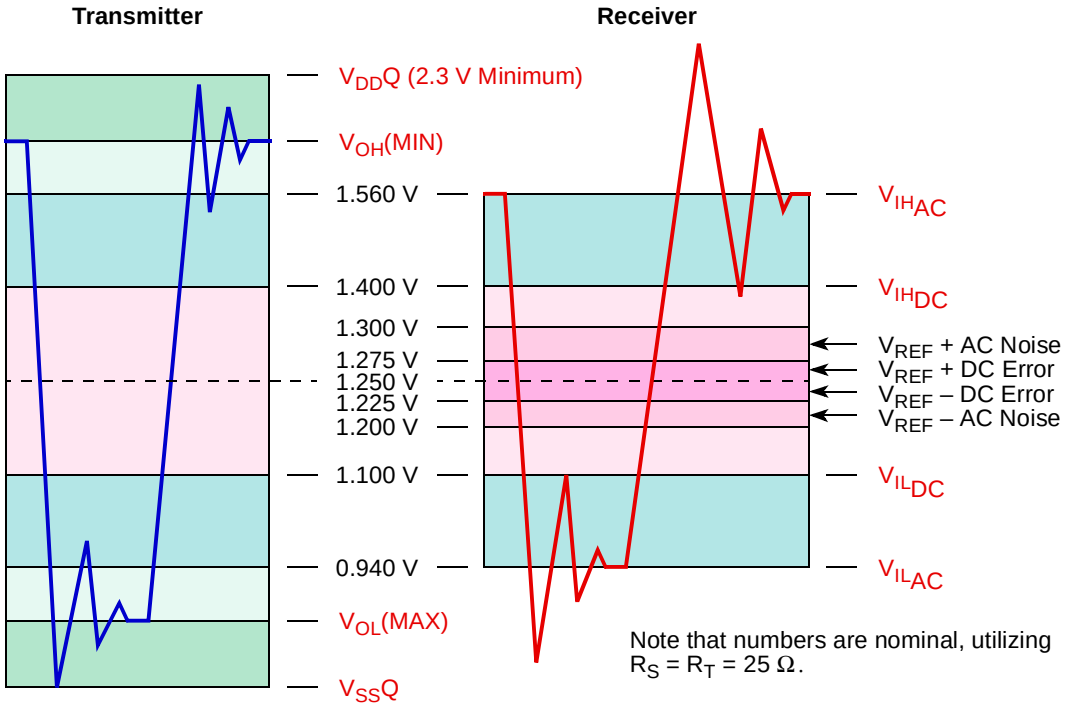

Figure 2. SSTL Signaling

1.1 Termination Dissipation

Sink and source currents flow through R_S and R_T. Assuming worst-case parameters and that the Class II termination scheme of Figure 1 is used, the power dissipation for these resistors is as follows:

$$P_{(RT \text{ and } RS)} = I^2 * R = (26.5 \text{ mA})^2 * (25\ \Omega) = 17.6 \text{ mW}.$$

NOTE

See Section 7.8, "DDR VTT Voltage Rail," for current calculations.

Small compact 4-pin resistor packages (16 mm × 32 mm) that provide dissipation up to 1/16 watt (62.5 mW) are available. Such devices are ideal for the DDR termination.

2 DDR Signal Groupings

The DDR memory controller consists of more than 130 signals and provides a glueless interface for the memory subsystem. These signals can be divided into the following signal groups for the purpose of this design guide:

- Clocks
- Data
- Address/Command
- Control
- Feedback signals

Table 1 depicts signal groupings for the DDR interface. The remaining sections of this document give PCB layout recommendations for each group.

Table 1. DDR Signal Groupings for Routing Purposes

Group	Signal Name	Description	Section
Clocks	MCK[0:5]	DDR differential clock outputs	See Section 7.1, "Clock Signal Group MCK[0:5] and MCK[0:5]"
	$\overline{\text{MCK}}$[0:5]	DDR differential clock outputs (complement)	
Data	MDQ[0:63]	64-bit data bus	See Section 7.2, "Data—MDQ[0:63], MDQS[0:8], MDM[0:8], MECC[0:7]"
	MECC[0:7]	ECC pins	
	MDM[0:8]	Data mask pins	
	MDQS[0:8]	Data strobe pins	
Address/Command	MA[0:14]	Address bus	See Section 7.3, "Address and Command Signal Group"
	MBA[0:1]	Bank address	
	$\overline{\text{MRAS}}$	Row address strobe	
	$\overline{\text{MCAS}}$	Column address strobe	
	$\overline{\text{MWE}}$	Write enable	

Table 1. DDR Signal Groupings for Routing Purposes (continued)

Group	Signal Name	Description	Section
Control	MCKE[0:1]	Clock enable	See Section 7.4, “Control Signal Group”
	$\overline{\text{MCS}}$[0:3]	Chip selects	
Feedback	MSYNC_OUT	DRAM DLL synchronization output	See Section 7.5, “Feedback Signal Group”
	MSYNC_IN	DRAM DLL synchronization input	
Power	V_{REF}	Voltage reference for differential receivers	See Section 7.6, “DDR Power Delivery”
	V_{TT}	Termination voltage	

3 Controller Signal Pinout

The pinout for the DDR interface facilitates ease of routing to a standard JEDEC DIMM connector. For non-DIMM topologies (that is, discretes), DDR devices should be similarly placed to optimize signal fanout. Figure 3 shows general DDR controller pinout flow. The figure shows generic topology if a series damping (R_S) and parallel termination (R_T) scheme is used.

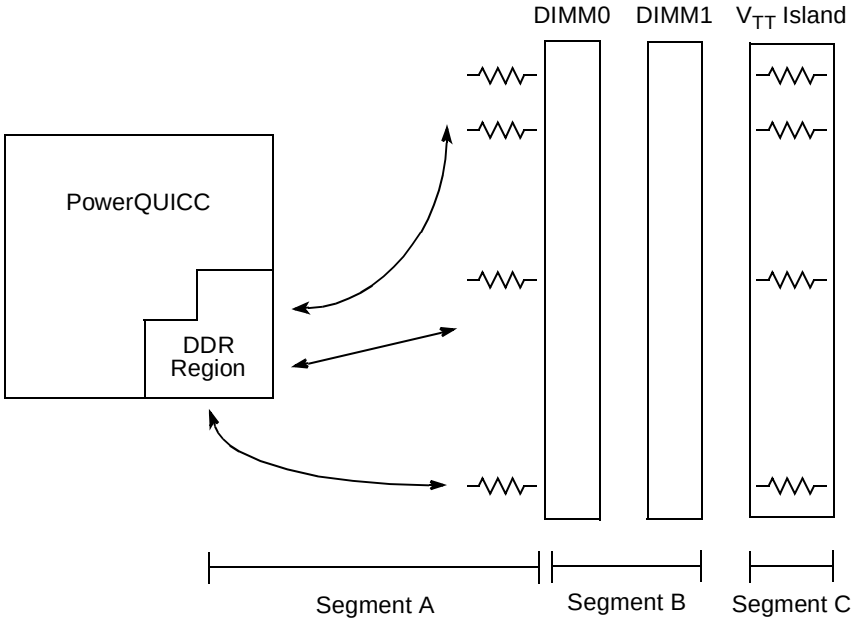

Figure 3. General DDR Controller Pinout Flow

4 Board Stack-Up

Freescale recommends placing all DDR signals on critical layers that are ground-referenced, which ensures the lowest impedance for the return currents and provides improved signal integrity performance. Ground referencing is especially critical for the data group as it operates at the 2x clock rate. If trade-offs must be made, allow the data and clock signal groups to be routed over solid ground planes and other DDR signal groups to be routed over solid power plans.

Each ground or power reference must be solid and continuous from the BGA ball through the end termination. Wherever power plan referencing is used, take care to avoid DDR signal crosses that split power planes, which adversely affect the impedance of the return currents.

5 Layout Order for the DDR Signal Groups

To help ensure that the DDR interface is properly optimized, Freescale recommends the following sequence for routing the DDR memory channel:

1. Power (V_{TT} island with termination resistors, V_{REF})
2. Pin swapping within resistor networks
3. Route data
4. Route address/command
5. Route control
6. Route clocks
7. Route feedback

The data group is listed before the command, address, and control group because it operates at twice the clock speed and its signal integrity is of higher concern. In addition, the data group constitutes the largest portion of the memory bus and consists of the majority of the trace matching requirements, those of the data lanes.

The address/command, control, and the data groups all have a relationship to the routed clock. Therefore, the effective clock lengths used in the system must satisfy multiple relationships. The designer should construct system timing budgets to ensure that all these relationships are properly satisfied. Section 10, “Interface Timing Analysis and Other Considerations,” describes these timing relationships.

6 Length Matching Overview

The following sections discuss considerations for length matching.

6.1 Signal Length Matching

Signal length matching is a two-fold item for the board designer. To ensure a robust interface, the designer must address both components. First, adhere to the absolute routed maximums to prevent signal integrity issues. As the absolute maximums affect component placement, the designer should derive the absolute maximums for each signal group before commencing board placement. Absolute maximums are easily determined by simulation. In most memory implementations, proper component placement easily satisfies the absolute maximums.

Directly or indirectly, all signal groups have some relationship to the clock signal, and the data has an additional relationship with its strobe. The second component of length matching deals with the clock-to-signal group relationship. This item ensures that sufficient timing margins are available on the interface.

Table 2 illustrates the key length relationships that the board designer should be cognizant of when determining the layout rules for the signal groups.

Table 2. Signal Group Length Relationships

Signal Group	Minimum Length	Maximum Length	Comment
Data lane to data strobe	Strobe length minus 25 mils	Strobe length plus 25 mils	See Note (1) and Note (4).
Data lane to data lane	No more than 1 inch delta among all data lane groups		See Note (2) and Note (4). See also Section 10.3.1, "Meeting the 75%–125% Write Data JEDEC Window"
Data strobe to clock	See Section 10.3.1, "Meeting the 75%–125% Write Data JEDEC Window"	See Section 10.3.1, "Meeting the 75%–125% Write Data JEDEC Window"	See Note (2). See also Section 10.3.1, "Meeting the 75%–125% Write Data JEDEC Window"
Address/command/ control to clock	Should be determined through simulation.	Should be determined through simulation.	See Note (3)

1 Based on skew tolerance during read cycles. Takes into account all board and device variances in the skew budget window.

2 This specification is dictated by the write data to the DRAM devices, which must fall within a clock window. JEDEC specifies a fairly wide clock window range (from 75% to 125% of one clock cycle). The WR_DATA_DELAY within the TIMING_CFG_2 registers enables the DDR write data to be positioned properly within the clock window range.

3 Because the loading on the address/command can vary from as little as 15 pF (four x16 devices with no ECC) all the way up to 108 pF (4 physical banks with nine x8 devices/per bank), and because the clock frequency and signal integrity of the specific memory implementation can greatly influence the setup/hold margins, the relationship should be determined through simulation.

4 The given numbers provide the most flexibility across all frequency ranges. If needed, this relationship could be relaxed further based on the frequency of the memory interface.

7 Layout Guidelines for the Signal Groups

The section describes the general layout guidelines for the signal groups noted in Table 1. These general guidelines are mostly independent of the memory system implementation, and can serve as an initial foundation for the board designer. Additional guidelines for specific memory implementations are given in Section 8, "Layout Guidelines for Specific Implementations."

7.1 Clock Signal Group MCK[0:5] and $\overline{\text{MCK}}$[0:5]

The DDR clock signal group consists of six differential clock pairs, labeled as MCK[0:5] and $\overline{\text{MCK}}$[0:5]. These six differential clock pairs enable the system designer to handle a worst case scenario of up to two unbuffered DIMM modules (3 clocks per DIMM), or up to thirty-six x8 discrete devices, if similar motherboard tree topologies are constructed analogous to DIMM modules. Registered DIMM implementations require only a single clock per DIMM. Therefore, for most mainstream memory implementations, no external clock driver/PLL is required on the board.

NOTE

The reference to 36 discrete devices is stated for references purposes only, mainly to illustrate the largest clock tree that can be constructed from the device. Capacitive loading along with signal topologies on the address/command buses in such a scenario would limit the maximum interface speed. The designer must simulate the particular implementation to determine whether the desired interface frequency is achievable.

7.1.1 DDR Layout Recommendations

Table 3 shows the general layout recommendations for the DDR clock control group.

Table 3. General Layout Recommendations for the DDR Clock Group

Item	Recommendation	Comment
Reference plane	Ground-referenced	Maintain a solid ground reference (no splits and so on) for all routed clocks, thereby providing a low-impedance path for the return currents.
Same layer routing	Route all clock pairs on the same critical layer. Avoid switching between layers except where required. See Figure 5 and Figure 6.	Ensures all clocks have the same signal integrity. Swap clock pairs as needed so that signal routing is optimized between the controller and the memory.
Characteristic impedance	= 50–60 Ω single-ended = 100–120 Ω differential	All pairs must be routed differentially from the DDR controller to the end point (DIMM or discrete).
Trace width	Implementation-specific	—
Differential spacing	Implementation-specific	Correct differential spacing must be maintained throughout entire signal route. See Figure 4.
Pair-to-pair spacing	20 mils	Exceptions may be needed at device breakout
Group spacing (clocks to all other signals)	20 mils to any other signal	See Figure 4. Exceptions may be needed at device breakout.
Serpentine isolation spacing	Maintain at least 20 mils	See Figure 4
MCK to $\overline{\text{MCK}}$ trace matching	Matched to within 20 mils	—
Clock pair-to-clock pair matching	All clock pairs to a given memory bank (DIMM or discrete) matched to within 20 mils	—
Series damping resistor value	Range 15–33	Optimal value and location system dependent and should be determined by simulations. For point-to-point connections, placement is optimal at the source. For point-to-multipoint, placement at the loads (DIMM connector or discrete bank) may prove optimal.
Optional–parallel termination to V_{TT} [1]	25–57 Ω ± 1%	Considered to be an optional item based on internal simulation runs and application notes published by Micron (see Section 14, “Useful References”).
Use of resistor networks for damping resistor	Not recommended	—

Table 3. General Layout Recommendations for the DDR Clock Group (continued)

Item	Recommendation	Comment
Differential termination	100–120 Ω	Required only for discrete implementations. DIMM modules provide the differential termination.

1 Values denoted in the table provide a starting-point for the designer and are not intended to be the only acceptable values. For example, if clocks are point-to-multipoint, a lower differential impedance (less than 100) may prove more effective in matching the actual loaded impedance of the system.

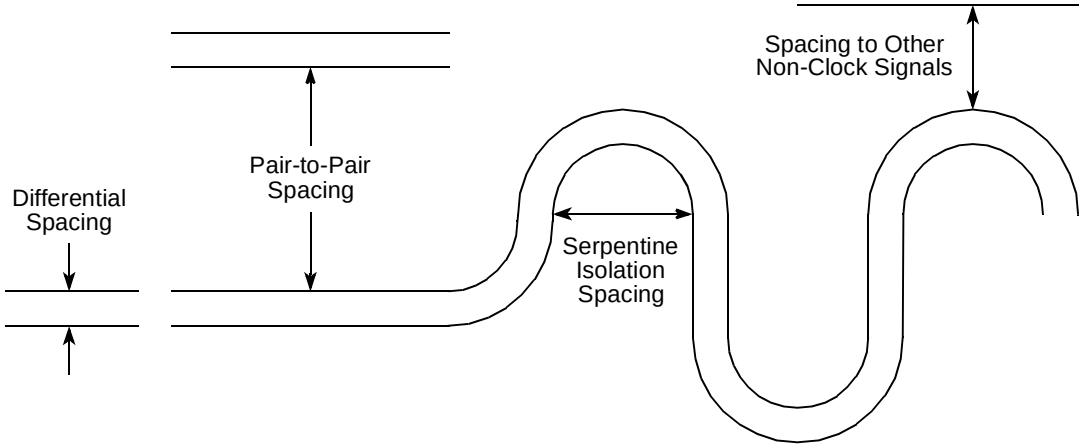

Figure 4. Differential Clock Routing Example

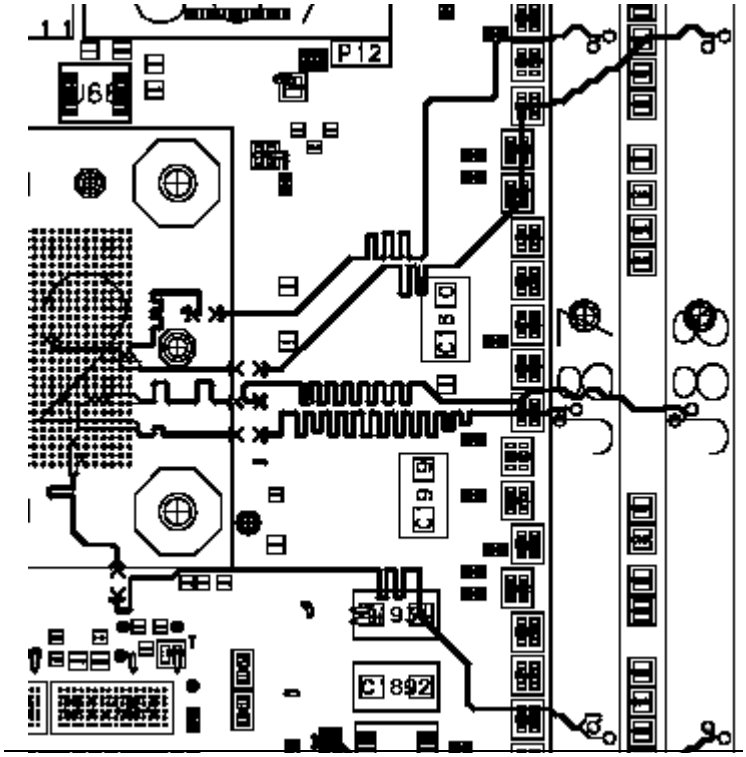

Figure 5. Clock Routing Example—All Clocks Routed on Same Layer (Zoomed-Out View)

Figure 6. Clock Routing Example—All Clocks Routed on Same Layer (Zoomed-In View)

7.2 Data—MDQ[0:63], MDQS[0:8], MDM[0:8], MECC[0:7]

The data signals of the DDR interface are source-synchronous signals whereby the data is captured by the memory and at the controller using the data strobe rather than the clock itself. When transferring data, both edges of the strobe are used to achieve the 2x data rate.

For each data byte lane, an associated data strobe (DQS) and data mask (DM) comprise each byte lane. This 10-bit byte lane relationship is crucial for routing. Table 4 depicts this relationship. When length matching, the critical item is the variance of the signal lengths within a given byte lane. Length matching across all bytes lanes is also important, but is more relaxed than the byte lane itself.

Table 4. Byte Lane to Data Strobe and Data Mask Mapping

Data	Data Strobe	Data Mask	Lane #
MDQ[0:7]	MDQS0	MDM0	Lane #0
MDQ[8:15]	MDQS1	MDM1	Lane #1
MDQ[16:23]	MDQS2	MDM2	Lane #2
MDQ[24:31]	MDQS3	MDM3	Lane #3
MDQ[32:39]	MDQS4	MDM4	Lane #4
MDQ[40:47]	MDQS5	MDM5	Lane #5
MDQ[48:55]]	MDQS6	MDM6	Lane #6
MDQ[56:63]	MDQS7	MDM7	Lane #7
MECC[0:7]	MDQS8	MDM8	Lane #8

NOTE

When routing, each row (that is, 10-bit signal group) must be treated as a trace-matched group.

7.2.1 Data Layout Recommendations

Freescale strongly recommends routing each data lane adjacent to a solid ground reference for the entire route to provide the lowest inductance for the return currents, assisting the overall signal integrity of the data interface. This concern is especially critical in designs that target the top-end interface speed, because the data switches at 2x the applied clock, and can be up to 333 MHz. When routing the byte lanes, signals within a byte lane should be routed on the same critical layer as they traverse the PCB motherboard to the memories and then finally to the V_{TT} termination end of the bus. This consideration helps minimize the number of vias per trace and provides uniform signal characteristics for each of the data lanes.

To facilitate ease of break-out from the controller perspective and to keep the signals within the byte group together, the board designer should alternate the byte lanes on different critical layers (see Figure 7 and Figure 8).

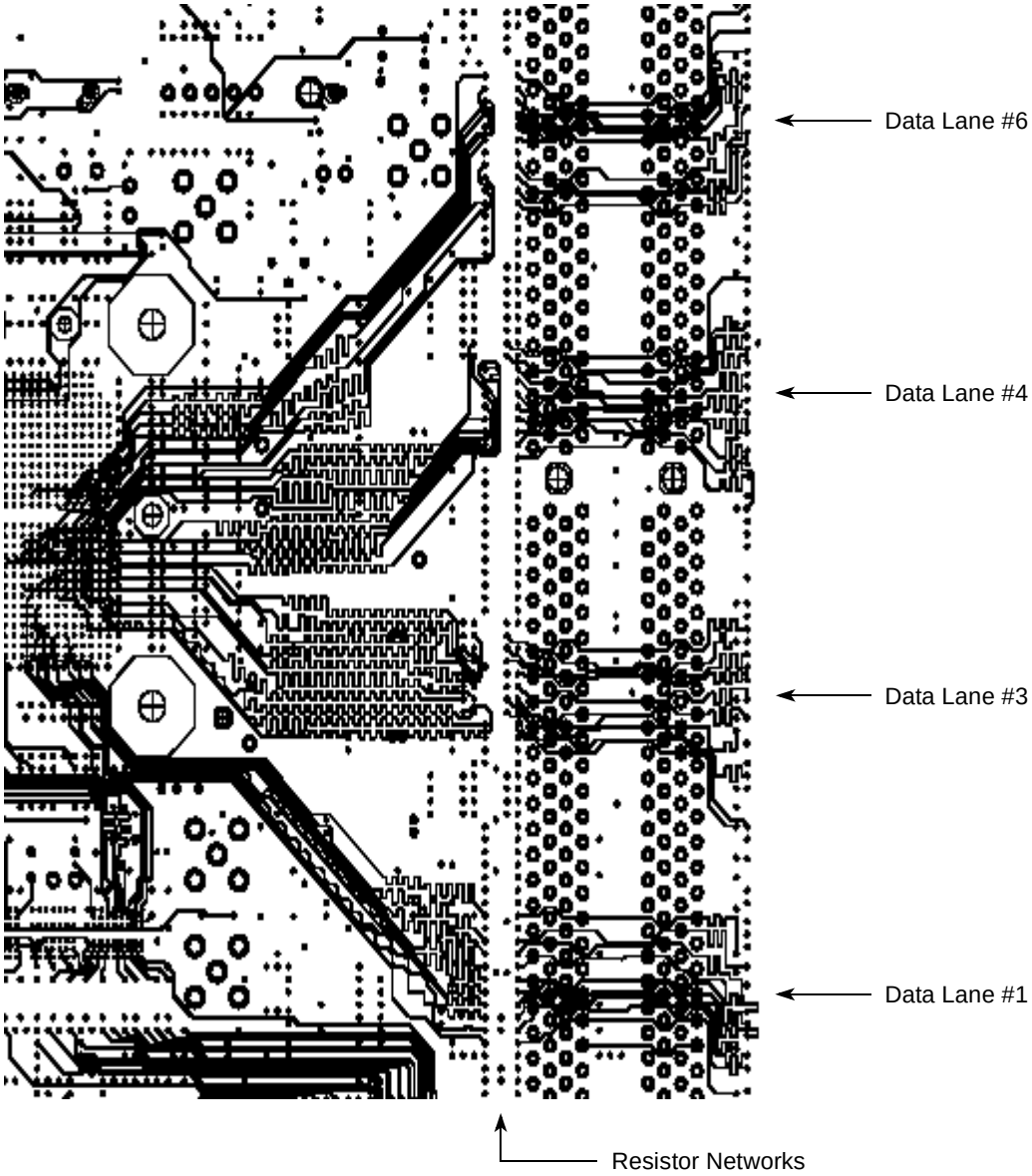

Figure 7. Alternating Data Byte Lanes on Different Critical Layers—Part #1

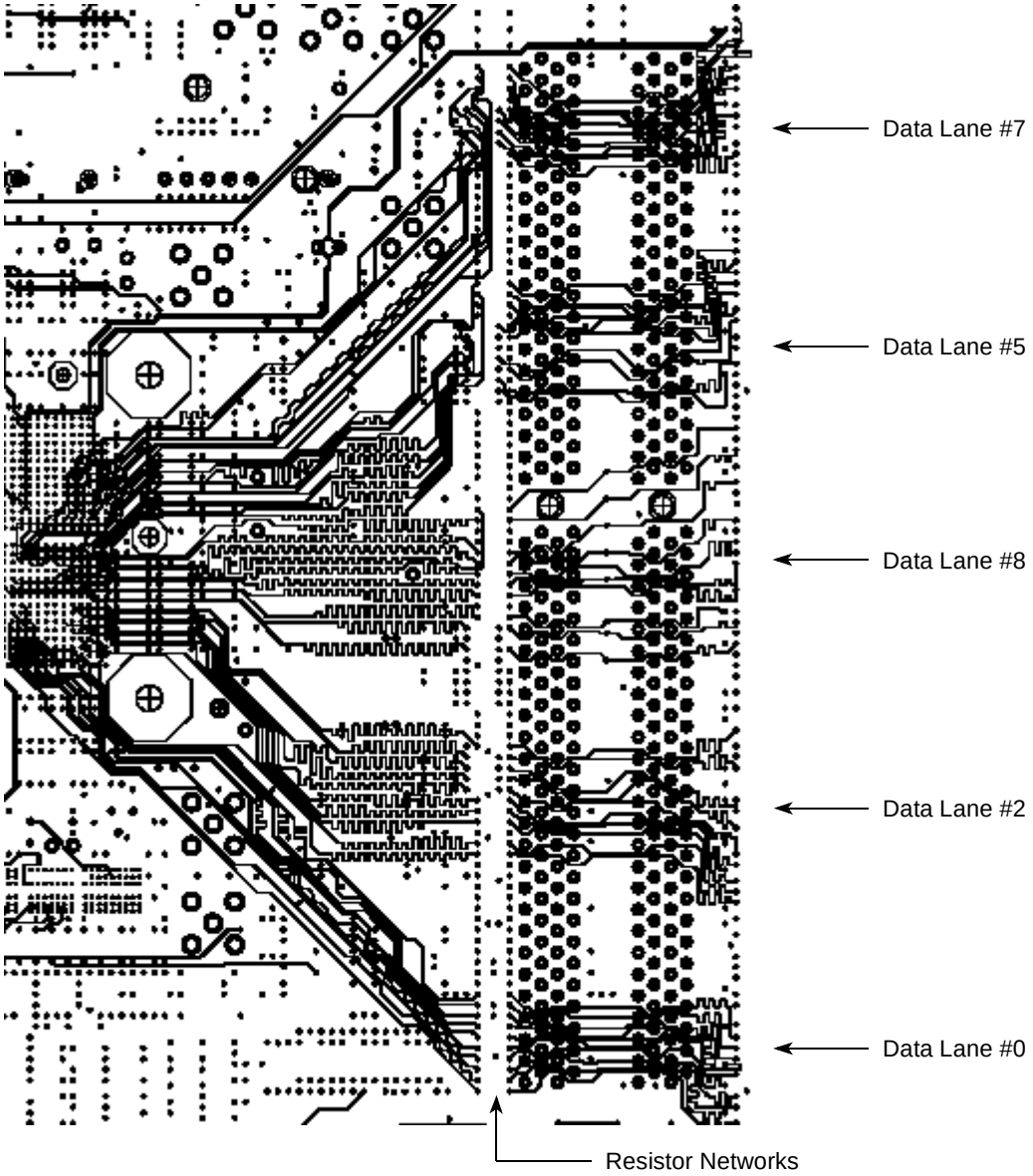

Figure 8. Alternating Data Byte Lanes on Different Critical Layers—Part #2

Because the DQS lines provide ‘data-latching’ function into the controller during reads and into the memory during writes, take care to reduce cross-talk noise from adjacent signal aggressors. Do not place the DQS strobes in the same resistor packs as the command and address if possible. In addition, ensure that at least a 4-W distance is maintained as much as possible between a DQS line and any other non-data group signal.

Table 5 shows the general routing rules for most memory system implementations.

Table 5. General Routing Recommendations for the DDR Data Signal Group

Item	Recommendation	Comment
Topology	Daisy chain	
Reference plane	Ground-referenced	Maintain a solid ground reference (no splits and so on) for all routed clocks, thereby providing a low-impedance path for the return currents.
Characteristic impedance [1]	50–60 Ω	—
Trace width	Implementation-specific	—
DQS spacing	4 W minimum	—
Group spacing	20 mils of isolation from other non-DDR related signals	—
Series resistor [1]	0–33 Ω ± 5%	—
Termination resistor [1]	25–57 Ω ± 5%	—
Length matching within the byte lane	±25 mils from the data strobe	Allows max interface speeds. See Section 7.2.2, “Data Group Matching Requirements”
Length matching byte lane to byte lane [2]	No more than 1 inch delta between all groups	See also Section 10.3.1, “Meeting the 75%–125% Write Data JEDEC Window”
Length matching DQS to clock	See Section 10.3.1, “Meeting the 75%–125% Write Data JEDEC Window”	See Section 10.3.1, “Meeting the 75%–125% Write Data JEDEC Window”
Resistor packs	Use as needed	Do not place the data group in the same RNs as the other DDR signal groups.

1 Values denoted in the table provide a starting place for the designer and are not intended to be the only acceptable values. For example, it may be possible for certain topologies to eliminate R_S and/or to modify the characteristic impedance below 50 Ω in order to more optimally match the actual loaded impedance of the system.

2 This specification is dictated by the write data to the DRAM devices, which must fall within a clock window. JEDEC specifies a fairly wide clock window range (from 75% to 125% of one clock cycle). The numbers given in Table 5 provide the most flexibility across all frequency ranges. If needed, this relationship could be relaxed further based on the frequency of the memory interface.

7.2.2 Data Group Matching Requirements

To achieve the highest performance from the DDR data bus at 333 MHz, pay close attention to trace matching to ensure that the design is robust over temperature, power variations, and other secondary effects. The key relationship for both reads and writes is the relationship between a given data strobe and its DQs and DM signals. See Section 10.3, “Data Group Timing Analysis,” for more information.

7.3 Address and Command Signal Group

The DDR address and command signal group consists of 20 signals. Figure 9 shows these signals.

Address/Command	MA[0:14]	Address bus
	MBA[0:1]	Bank address
	$\overline{\text{MRAS}}$	Row address strobe
	$\overline{\text{MCAS}}$	Column address strobe
	$\overline{\text{MWE}}$	Write enable

Figure 9. DDR Address and Command Signal Group

NOTE

By default, the address and command signals three-state during inactive periods.

7.3.1 Address and Command Layout Recommendations

Table 6 describes the general routing rules for most memory system implementations.

Table 6. General Routing Recommendations for the DDR Address and Command Group

Item	Recommendation	Comment
Reference plane	Ground-referenced or power-referenced	Maintain a solid ground reference or power reference (no splits, and so on) for the entire signal group to provide a low-impedance path for the return currents
Characteristic impedance [1]	= 50 – 60 Ω	—
Trace width	Implementation-specific	—
Group spacing	20 mils	Isolation from control group to other non-DDR signals
Length matching (with respect to clock)	Min <= Addr/Cmd Group <= Max	—
Minimum Addr/Cmd group length [2]	Max clock length – ‘Y’	—
Maximum Addr/Cmd group length [2]	Minimum clock length – ‘Y’ inches	—
Series resistor [1]	0–33 Ω ± 5%	—
Termination resistor [1]	25–57 Ω ± 5%	—
Resistor packs	Use as needed	Do not place the addr/cmd group in the same RN as the data group

1 Values denoted in the table provide a starting place for the designer and are not intended to be the only acceptable values. For example, it may be possible for certain topologies to eliminate R_S and/or to modify the characteristic impedance below 50 Ω to match the actual loaded impedance of the system more optimally.

2 The parameter ‘Y’ is the timing variance around the clock edge that can be tolerated for a specific memory implementation and still ensure that setup and hold times can be satisfied. Because loading, clock frequency and signal integrity of the specific memory implementation greatly influence the ‘Y’ parameter, it is important that the value of ‘Y’ is determined by simulation.

7.4 Control Signal Group

The control group enables the board designer to implement up to 4 physical banks of memory, which allows up to two unbuffered DIMM slots (2 chip selects per slot), 2–4 registered DIMM slots depending on single or dual rank modules, or up to 4 physical memory banks based on discrete populations. The DDR control signal group consists of six signals (see Figure 10).

Control	MCKE[0:1]	Clock enable
	$\overline{\text{MCS}}$[0:3]	Chip selects

Figure 10. DDR Control Signal Group

7.4.1 Memory System Layout Recommendations

Table 7 shows the general routing rules for most memory system implementations.

Table 7. General Routing Recommendations for the DDR Control Group

Item	Recommendation	Comment
Reference plane	Ground-referenced or power-referenced	Maintain a solid ground reference or power reference (no splits and so on.) for the entire signal group thereby providing a low-impedance path for the return currents
Characteristic impedance [1]	= 50–60 Ω	—
Trace width	Implementation-specific	—
Group spacing	20 mils	Isolation from control group to other non-DDR signals
Length matching (with respect to clock)	Min <= control group <= Max	—
Minimum control group length [2]	Max clock length—'Z'	—
Maximum control group length [2]	Minimum clock length—'Z' inches	—
Series resistor [1]	0–33 Ω ± 5%	—
Termination resistor [1]	25–57 Ω ± 5%	—
Resistor packs	Use as needed	Do not place the control signals in the same RN as the data group

[1] Values denoted in the table provide a starting place for the designer and are not intended to be the only acceptable values. For example, it may be possible for certain topologies to eliminate R_S and/or to modify the characteristic impedance below 50 Ω to match the actual loaded impedance of the system more optimally.

[2] The parameter 'Z' is the timing variance around the clock edge that can be tolerated for a specific memory implementation and still ensure that setup and hold times can be satisfied. Because the loading, clock frequency and signal integrity of the specific memory implementation greatly influence the 'Z' parameter, it is important that the value of 'Z' is determined by simulation.

7.5 Feedback Signal Group

The DDR feedback signal group consists of two signals (see Figure 11).

Feedback	MSYNC_OUT	DRAM DLL synchronization output
	MSYNC_IN	DRAM DLL synchronization input

Figure 11. DDR Feedback Signal Group

Table 8 shows the general routing rules that should apply to most memory system implementations.

Table 8. General Routing Recommendations for the DDR Feedback Group

Item	Recommendation	Comment
Reference plane	Ground-referenced	Maintain a solid ground reference (no splits and so on) for the entire signal group to provide a low-impedance path for the return currents
Characteristic impedance [1]	= 50–60 Ω	Use same impedance as differential clocks (single-ended)
Trace width	Implementation-specific	—
Group spacing	20 mils	Isolation from feedback group to all other board signals
Series damping resistor value[1]	25–36	The optimal value system is dependent and should be determined by simulations
Access point for shortening/lengthening the DLL feedback path	0 Ω	Highly recommended that the designer place a 0-Ω resistor at the MSYNC_IN pin. Such flexibility allows the feedback path to be adjusted easily (if needed) during the prototyping phase by removing this resistor and the series damping resistor noted above.
Optional -Parallel termination to V_{TT} [1]	25–57 Ω ± 1%	Considered to be an optional item based on internal simulation runs and based on clock routing rules from Micron (see Section 14, “Useful References”).
Resistor packs	Not recommended	—
Placement of series damping resistor	Place as close to the MSYNC_OUT pin as possible	—
Trace matching of feedback path	The feedback path should be trace matched to within 20 mils of the mid-point of the 6 clock pair lengths.	This recommendation assumes no clock shifting is needed within the designer’s system budget.
Serpentine isolation spacing	Maintain at least 20 mils	See Figure 4

1 Values denoted in the table provide a starting place for the designer and are not intended to be the only acceptable values.

7.6 DDR Power Delivery

The DDR controller and associated memory channel requires a +2.5-V supply, +1.25-V_{TT} rail, and +1.25-V_{REF} supply for proper operation. Table 9 highlights the tolerances permitted on each of the voltages.

Table 9. DDR Voltage Requirements

	Parameter	Min	Typical	Max	Unit
V_{DD}	Device supply voltage	2.3	2.5	2.7	V
V_{REF}(DC)	Input reference voltage	1.13	1.25	1.38	V
V_{TT}	Termination voltage	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04	V
I_{REF}	V_{REF} current	—	—	0.003	A
I_{TT}	V_{TT} supply current [1]	—	—	2.3–3.2	A

[1] Maximum current rating based on specific termination and values used for a specific topology. For this case $R_S = R_T = 25\ \Omega$. Calculated under maximum signal loading (all DDR signals drawing current from V_{TT} plane).

7.7 DDR V_{REF} Voltage

The current requirements for V_{REF} are relatively small, at less than 3 mA. This reference provides a DC bias of 1.25 V (V_{DD}/2) for the differential receivers at both the controller's interface and at the DDR devices. Voltage tolerances are summarized in Table 9.

Noise or deviation in the V_{REF} voltage can lead to potential timing errors, unwanted jitter, and erratic behavior on the memory bus. To avoid these problems, keep V_{REF} noise within the 25 mV specification. As such, V_{REF} and the V_{TT} cannot be the same plane because the DRAM V_{REF} buffers' sensitivity to the termination plane noise. However, both V_{REF} and V_{TT} must share a common source supply to ensure that both are derived from the same voltage plane. Proper decoupling at each V_{REF} pin (at the controller, at each DIMM/discrete, and at the V_{REF} source) along with some simple layout considerations can keep the noise within specification.

Numerous off-the-shelf power solutions can provide both the V_{REF} and V_{TT} from a common circuit. An another alternative is to generate V_{REF} using a simple divider network as shown in Figure 12. If used, the divider network should be placed in the middle of the memory configuration. To minimize voltage deviation, 1% resistor values should be used for the divider network. Additionally, like the common circuit generation method, decoupling is required at each V_{REF} pin in the memory topology, including the controller's V_{REF}, each DIMM or discrete device's V_{REF}, and the divider network itself.

Regardless of the generation technique, common circuit or divider network, V_{REF} can track variations in V_{DDQ} over voltage, temperature, and noise margins as the interface specifications require.

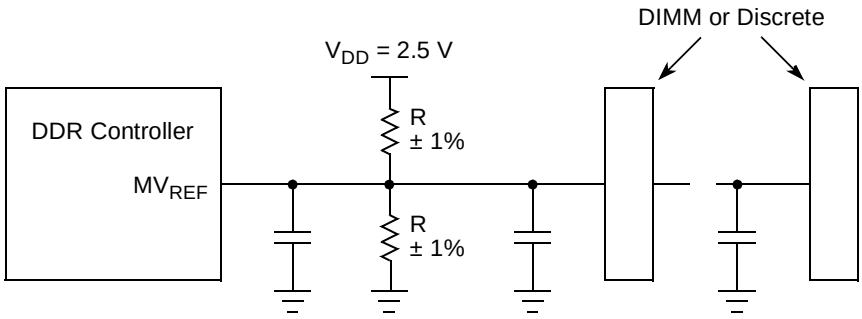

Figure 12. V_{REF} Generation Using a Simple Resistor Divider Circuit

7.7.1 Routing Layout Recommendations

Table 10 shows the general routing rules for most memory system implementations.

Table 10. General Routing Recommendations for V_{REF}

Item	Recommendation	Comment
V_{REF} generation	Use resistor divider network or an off-the-shelf DDR regulator that generates V_{REF}.	Ensures that V_{REF} tracks the midpoint of the voltage swing.
V_{REF} decoupling	Use distributed and balanced decoupling. Specifically, decouple the source and each destination pin using 0.1 or 0.01 bypass caps.	Localizes transient currents and returns. If single IC is used to generate V_{TT} and V_{REF}, add additional decoupling according to the manufacturer's recommendation.
V_{REF} Isolation	Keep a 20–25 mil clearance between V_{REF} and other traces.	If possible, isolate the V_{REF} track as much with adjacent ground trace segments.
V_{REF} trace width	Route V_{REF} with as wide a trace as possible, for example, a minimum of 20–25 mil where feasible.	—
V_{REF} divider resistors (if used)	Ensure the use of 1% resistors. Suggested range 50–150 Ω.	Both resistors must be the same value.

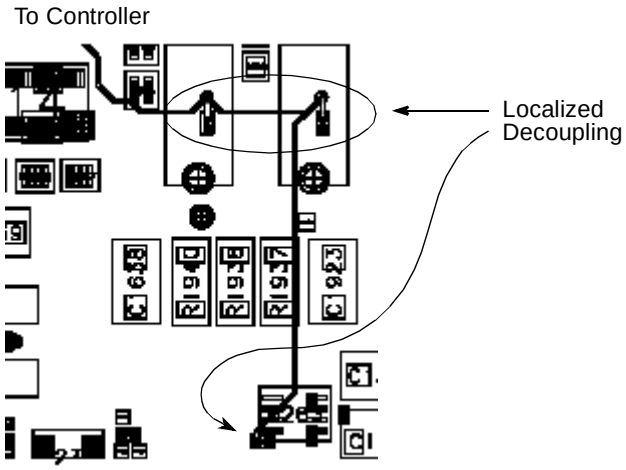

Figure 13. Example V_{REF} Route—DIMM-Based Topology

7.8 DDR V_{TT} Voltage Rail

With the exception of the six DDR clock pairs, the V_{TT} termination rail terminates all DDR signals to 1.25 V using a parallel resistor (R_T). Unlike V_{REF}, V_{TT} must be capable of sinking and sourcing high transient currents in the range of 2.0–3.5 A.

For a given topology, the worst case V_{TT} current should be derived. For example, using the typical circuit given in Figure 1 and the worst case parameters give in Table 11, sink and source currents can be calculated for the memory topology.

Table 11. Worst Case Parameters for V_{TT} Current Calculation

Parameter	Values	Comment
V_{DDQ} (max)	2.7 V	From tolerance table
V_{TT} (max)	1.39 V	From tolerance table
V_{TT} (min)	1.11 V	From tolerance table
R_{DRVR}	10 Ω	Target typical is 17 Ω
R_S	25 Ω	Assumes typical JEDEC scheme
R_T	25 Ω	Assumes typical JEDEC scheme
V_{OL}	0 V	Assumes driver reaches 0 V in the low state. Typically between 0.3–0.8 V.

A driver would source (V_{TT} plane would sink) the following based on this termination scheme:

$$(V_{DD\_max} - V_{TT\_min})/(R_T + R_S + R_{DRVR}) = (2.7\ V - 1.11\ V)/(25 + 25 + 10) = 26.5\ mA$$

The driver would sink (V_{TT} plane would source) the following based on this termination scheme:

$$(V_{TT\_max} - V_{OL} / (R_T + R_S + R_{DRVR}) = (1.39\ V - 0\ V)/(25 + 25 + 10) = 23.2\ mA$$

A bus with balanced number of high and low signals would place no real demand on the V_{TT} supply. However, a bus that had all DDR signals low (+115 signals) would cause a transient current demand of approximately 2.7 A.

In tandem to these high transient peaks, the regulator must be able to provide relatively tight voltage regulation (summarized in Table 9). Besides a tight tolerance, the regulator must also allow V_{TT} along with V_{REF} (if driven from a common IC), to track variations in V_{DDQ} over voltage, temperature, and noise margins.

Freescale recommends that the V_{TT} termination rail is a solid surface island trace at least 150 mils wide and located at the end of the memory channel, just past the last DIMM or discrete memory bank. Figure 14 shows an example surface island implementation. Leveraging a surface island implementation greatly improves the transient switching ability of the bypass scheme (lowering the ESL and ESR of decoupling scheme) while reducing the number of required bypass caps by a factor of three.

Each parallel resistor (R_T), whether discrete or using a resistor network, should be tied directly to the surface island trace. If resistor networks are utilized for the V_{TT} termination, take care to avoid mixing the DDR data groups with the other signal groups.

Figure 14. V_{TT} Surface Island Example—Zoomed-Out View

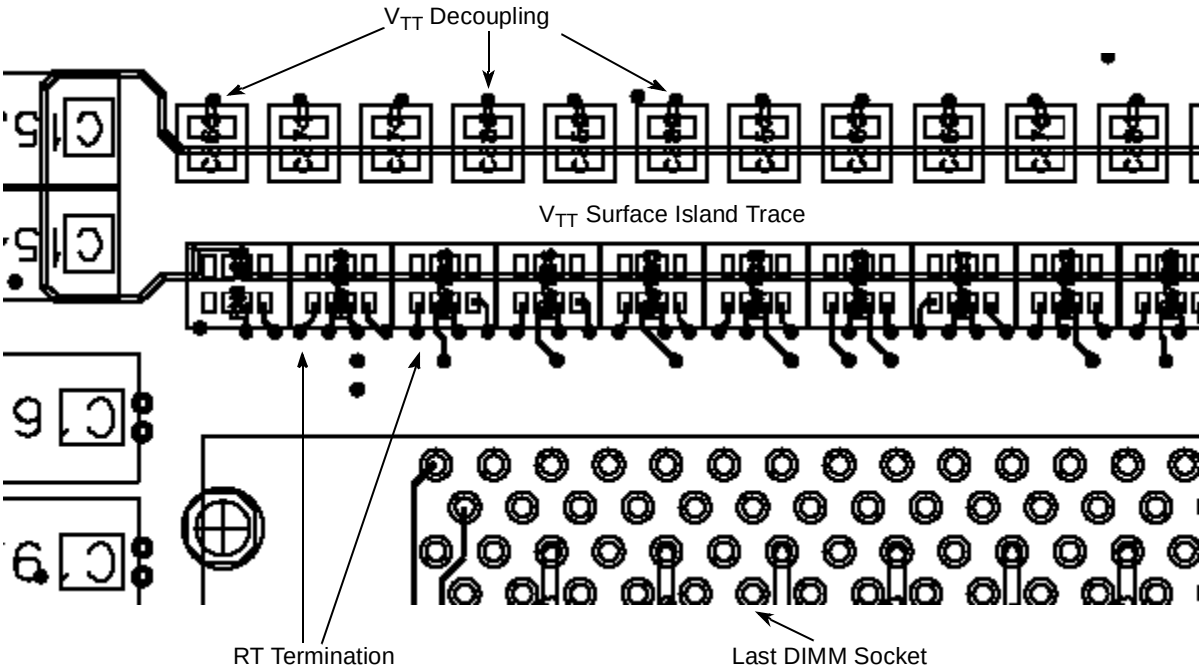

Figure 15. V_{TT} Surface Island Example—Zoomed-In View

7.8.1 V_{TT} Layout Recommendations

Table 12 shows the general routing rules for most memory system implementations. The recommendations listed in Table 12 are based on a V_{TT} surface island implementation. If this is not the case, the hardware designer should significantly increase the number of decoupling capacitors. See the Micron DesignLine publication, Vol 9, Issue 3, 3Q00, article entitled *Decoupling Capacitor Calculation for a DDR Memory Channel* for further information.

Table 12. General Routing Recommendations for V_{TT}

Item	Recommendation	Comment
V_{TT} island placement	Place at end of memory channel. Keep as close to the last DIMM or discrete memory bank as possible (that is, <1 inch).	—
V_{TT} island track width	Utilize a wide surface island trace of at least 150 mils	—

Table 12. General Routing Recommendations for V_{TT} (continued)

Item	Recommendation	Comment
V_{TT}high frequency decoupling	• At least one low ESL cap, or two standard decoupling caps for each 4-pin resistor network used. • At least two additional decoupling caps (4.7 µF) at each end of the V_{TT} island.	Bypass caps should be evenly spread throughout the V_{TT} island, ensuring that all termination resistors are close to a high-speed capacitor. Based on calculations derived from Micron's DesignLine publication, Vol 9, Issue 3, 3Q00, article entitled *Decoupling Capacitor Calculation for a DDR Memory Channel*.
V_{TT} low frequency decoupling	Place a bulk cap (100–220 µF) capacitor at each end of the island.	—
V_{TT} regulator placement	If placement permits, place the V_{TT} generation in the middle of the island or as close to one end of the island as possible.	—
Sense pin for V_{TT} regulator (if available)	Attach in the middle of the island	—
Other decoupling	Ensure sufficient high-speed decoupling and bulk decoupling is provided at the output of the 1.25-V regulator to ensure high stability and responsiveness of the solution.	Vendor-specific. Consult the specific vendor data sheets.
Termination resistor and decoupling placement	Place on the top layer and directly connect V_{TT} island	—

8 Layout Guidelines for Specific Implementations

The following sections discuss additional layout guidelines for specific system implementations.

8.1 Guidelines for Unbuffered DDR

This section contains additional considerations for customers who use two standard 184-pin JEDEC unbuffered DDR DIMM devices within the system. The guidelines are divided into respective signal groups that include data, clock, address/command, control, and feedback. The guidelines in this section apply to systems that use the controller 2T timing feature and run at maximum frequency. If you want to run at the top end frequency with a single cycle address/cmd capture window, see Section 10.2.1, "Single-Cycle Address/Command."

8.1.1 Clock Signal Group MCK[0:5] and $\overline{\text{MCK}}$[0:5]

The DDR interface consists of six differential clock pairs, labeled as MCK[0:5] and $\overline{\text{MCK}}$[0:5]. These six differential clock pairs enable the system designer to handle a worst case scenario of up to two unbuffered DIMM modules (three clocks per DIMM).

8.1.1.1 DDR Clock Pinout

The pinout for the clock signal group was optimized for routing to a standard DIMM based connector. Table 13 shows one potential breakout of the clock group that permits all clock pairs to be routed on a single critical layer. Table 13 is based on the initial 783-pin package layout. If a different package is used, the board designer should re-assign the clock pairs appropriately to allow all clock pairs to be routed on the same critical layer and avoid cross-overs or unnecessary layer switching.

Table 13. Optimized Clock Pair Routing in a Two-DIMM System

Clock Pair	DIMM	DIMM Pin #
MCK[0]	DIMM 0	Pin 137
MCK[0]	DIMM 0	Pin 138
MCK[1]	DIMM 0	Pin 16
MCK[1]	DIMM 0	Pin 17
MCK[2]	DIMM 0	Pin 76
MCK[2]	DIMM 0	Pin 75
MCK[3]$\bar{]}$	DIMM 1	Pin 137
MCK[3	DIMM 1	Pin 138
MCK[4]	DIMM 1	Pin 16
MCK[4]	DIMM 1	Pin 17
MCK[5],	DIMM 1	Pin 76
MCK[5]	DIMM 1	Pin 75

8.1.1.2 Clock Group Topology

All signal groups except the clocks and feedback are length-matched per slot to their respective DIMM clocks. The clocks themselves are matched to within a certain length variance at each DIMM slot. Figure 16 and Figure 17 show an example of clock topology for unbuffered DIMMs. In these side view representations, only one side of the diff pair is represented. Furthermore, the parallel terminator that is housed on the DIMM module is not shown.

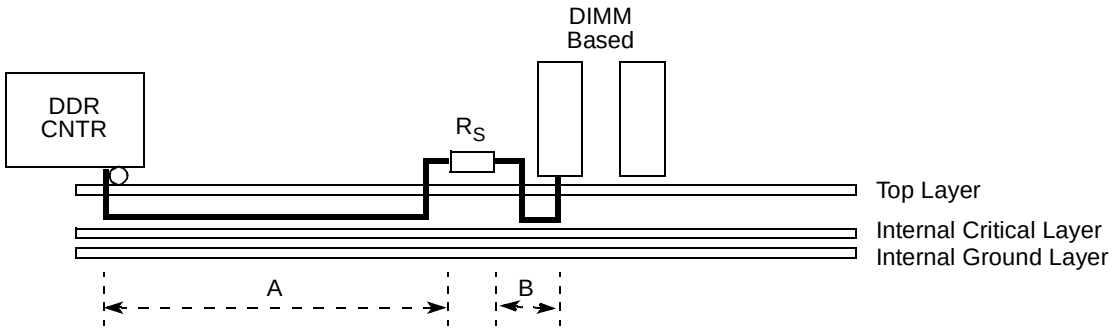

Figure 16. Clock Routing for First DIMM Memory Slot

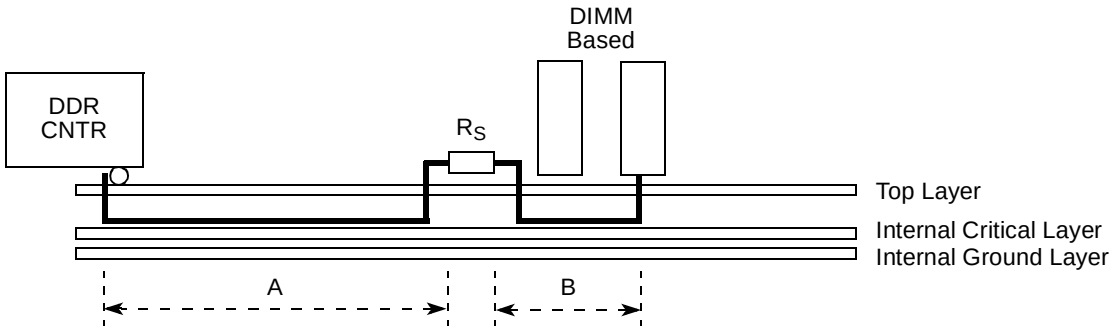

Figure 17. Clock Routing for Second DIMM Memory Slot

NOTE

Because each clock pair can drive up to six loads on an unbuffered DIMM module, the signal net is not a true point-to-point topology from the driver's perspective. The series damping resistor is placed close to the first DIMM module. Besides improving overshoot and undershoot, this arrangement frees precious board real estate at the DDR controller.

8.1.1.3 Additional Guidelines for the Clock Signal Group

Table 14. Additional Guidelines for the Clock Signal Group—Unbuffered DIMM Example

Item	Recommendation	Comment
Topology [1]	Point-to-point on motherboard for DIMM based module	—
Series damping resistor placement [2]	As close to the first DIMM as possible	Provides an 'RC-like' clock edge with no overshoot/undershoot
Trace segments A and B	Determined using simulation, as clock lengths must maintain a certain relationship to the other DDR signal groups	—

1 Table 14 describes the additional guidelines for unbuffered DIMM topologies. This table, used with Table 3, provides a composite list of recommendations for the DDR clock group when unbuffered DIMMs are being considered in a design.

2 If registered DIMMs are also being considered, placement of R_S is more optimal at the driver. In such topology, the system experiences more overshoot/undershoot when unbuffered DIMMs are present.

8.1.2 Data—MDQ[0:63], MDQS[0:8], MDM[0:8], MECC[0:7]

The following sections discuss data group typology and guidelines.

8.1.2.1 Data Group Topology

Figure 18 shows an example topology for the data signal group when unbuffered DIMMs are used. Table 15 provides some additional guidelines for this topology.

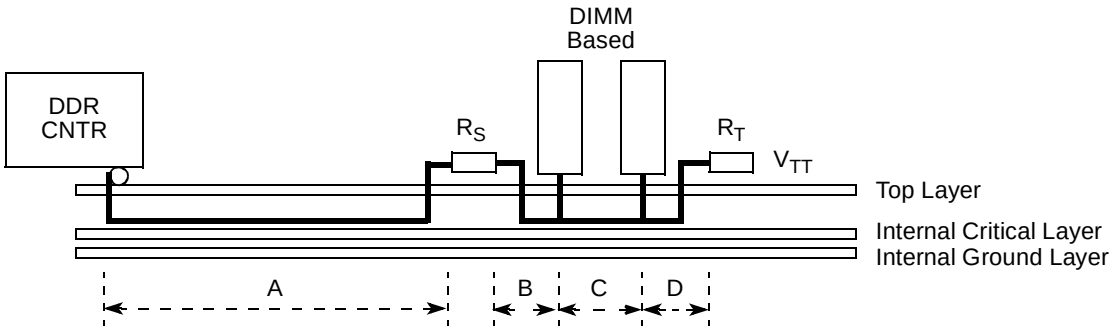

Figure 18. Data Group Routing Topology

8.1.2.2 Additional Guidelines for the Data Signal Group

Table 15 describes the additional guidelines for unbuffered DIMM topologies.

Table 15. Additional Guidelines for the Data Signal Group—Unbuffered DIMM Example

Item	Recommendation	Comment
Topology [1]	Daisy chain	—
Series damping resistor placement	As close to the first DIMM as possible	—
Trace Segments A, B, C, D	Determined using simulation, as clock lengths must maintain a certain relationship to the other DDR signal groups	—

1 Table 15 describes the additional guidelines for unbuffered DIMM topologies. This table, used withTable 5, together provide a composite list of recommendations for the DDR data group when unbuffered DIMMs are being considered in a design.

8.1.3 Address and Command Signal Group

The following sections discuss address and command group topology and guidelines.

8.1.3.1 Address and Command Group Topology

Figure 19 shows an example topology for the address and command signal group when unbuffered DIMMs are used. Table 16 provides some additional guidelines for this topology.

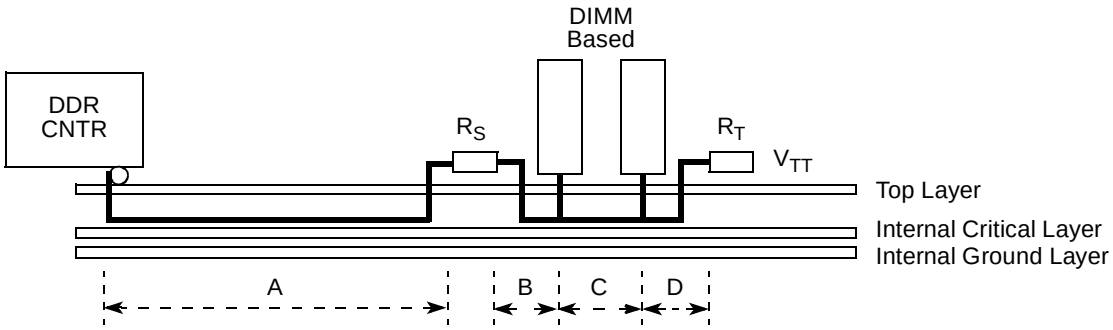

Figure 19. Address and Command Group Routing Topology

8.1.3.2 Additional Guidelines for the Address and Command Signal Group

Table 16 describes the additional guidelines for unbuffered DIMM topologies.

Table 16. Additional Guidelines for the Address/Cmd Signal Group—Unbuffered DIMM

Item	Recommendation
Topology [1]	Daisy chain
Series damping resistor placement	As close to the first DIMM as possible
Trace Segments A, B, C, D	Determined using simulation, as clock lengths must maintain a certain relationship to the other DDR signal groups

[1] Table 16 describes the additional guidelines for unbuffered DIMM topologies. This table, used with Table 6, provides a composite list of recommendations for the DDR addr/cmd group when unbuffered DIMMs are being considered in a design.

8.1.4 Control Group Topology

The following sections discuss control signal group topology and guidelines. Figure 20 and Figure 21 show the example topologies for the control signal group when unbuffered DIMMs are used. Table 17 provides some additional guidelines for this topology.

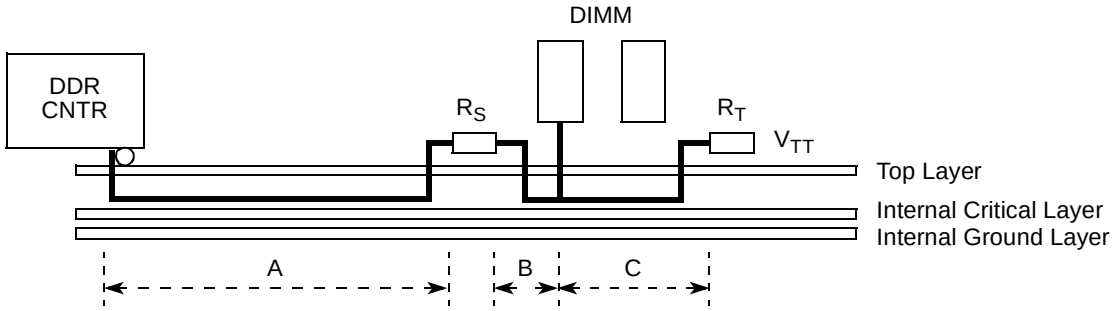

Figure 20. Control Group Routing for Unbuffered DIMM Topology—First DIMM Slot

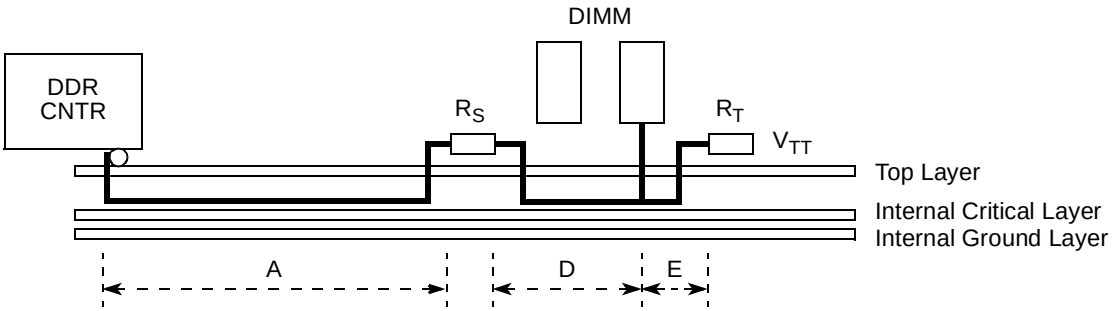

Figure 21. Control Group Routing for Unbuffered DIMM Topology—Second DIMM Slot

NOTE

Though not immediately obvious from Figure 20 and Figure 21, each CKE signal routes to two adjacent pins at the DIMM connector. The CKE signal has a slightly larger load than its chip select counterpart because each CKE must drive both physical banks on a given DIMM slot.

8.1.4.1 Additional Guidelines for the Control Signal Group

Table 17. Additional Guidelines for the Control Signal Group—Unbuffered DIMM

Item	Recommendation
Topology [1]	Daisy chain
Series Damping Resistor Placement	As close to the first DIMM as possible
Trace segments A, B, C, D, E	Determined using simulation, as clock lengths must maintain a certain relationship to the other DDR signal groups

1 Table 17 describes the additional guidelines for unbuffered DIMM topologies. This table, used with Table 7, provides a composite list of recommendations for the DDR control group when unbuffered DIMMs are being considered in a design.

8.1.5 Feedback Signal Group

No additional guidelines other than those specified in Section 7.5, “Feedback Signal Group,” are relevant for the feedback signal group.

8.1.6 DDR DIMM Decoupling Capacitor Guidelines

Freescale recommends a minimum of 10 high-frequency decoupling caps (0.1 µF) between the two DIMMs to help minimize the signal return path discontinuities that occur as the signals transition from the main PCB to the DIMM modules. These bypass capacitors should connect between 2.5 V and ground, and should use wide traces where possible. Bulk decoupling should be present around the DDR DIMMs. At minimum four 100-µF capacitors should be used on the outer edges of the DIMM connector (2 per DIMM). The power end of the capacitor should connect to 2.5 V and the ground side to the internal ground plane. Figure 22 shows the general placement for DIMM decoupling.

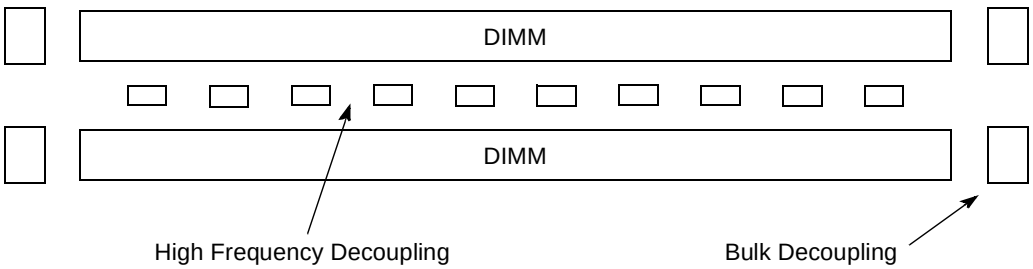

Figure 22. DDR-DIMM Decoupling Placement

8.2 Layout Guidelines for Discrete Memories Scenarios

For discrete memory subsystems, if the memory subsystem is constructed like that of a DIMM-based system, in terms of specific signal topology, relative component placement, minimum/maximum signal routes, and so on, the majority of recommendations given in this document should be applicable for discrete memory subsystems. The following guidelines can be made for discrete memory topologies:

1. Leverage the V_{TT} and V_{REF} layout guidelines noted in Section 7.7, "DDR V_{REF} Voltage," and Section 7.8, "DDR VTT Voltage Rail."
2. Construct the signal routing topologies for the groups like those found on unbuffered DIMM modules.
   — Trade-off: Placement of the series damping resistor (R_S) the data group is left to the board designer. This trade-off comes in the form of achieving optimal signal integrity for both reads/writes (R_S in middle) vs. ease of layout routing (R_S placed closer to memory devices).
3. As a initial starting place for simulation, leverage the general guidelines given in Section 7, "Layout Guidelines for the Signal Groups."
4. When placing components, optimize placement of the discretes to favor the data bus (analogous to DIMM topologies).
   — Optional: Pin-swap within a given byte lane to optimize the data bus routes further. Caution: Do not swap individual data bits across different byte lanes.
      • If multiple physical banks are needed, double stack (top and bottom) the banks to prevent lengthy and undesirable address/cmd topologies.
5. If a single bank of x16 devices is used, make the DDR clocks point-to-point. Place the series damping resistor (R_S) close to the source and the differential terminator (R_{DIFF}) at the input pins of the discretes.
   — If more than four discretes are used, construct the clocks like those found on unbuffered DIMM modules.
   — Alternatively, place an external PLL between the controller and the memory to generate the additional clocks.
6. Properly decouple the DDR chips per manufacturer recommendations. Typically, five low ESL capacitors per device are sufficient. For further information, see the article entitled, *Decoupling Capacitor Calculation for a DDR Memory Channel*, located on Micron's web site.
7. To allow expansion into larger devices, ensure that extra NC pins (future address pins) are connected.

9 Logic Analyzer Support Packages

Both Tektronix and Agilent have various DDR support and probing packages for their analyzers. The support can vary from simple bus transaction capture to full code disassembly. In addition, the analyzer visibility can be leveraged either directly on the motherboard or indirectly in certain instances using an adapter card plugged into an DIMM/SO-DIMM socket, assuming a DIMM-based memory topology, and offers the board designer the advantage of more available board real estate.

If visibility is leveraged on the motherboard, the board designer should leverage the existing probing footprint per the specific vendor of interest to permit quick and easy access to the memory interface during card debug.

NOTE

A designer who intends to use an off-the-shelf visibility module should avoid pin-swapping between the controller and DIMM connector.

10 Interface Timing Analysis and Other Considerations

10.1 Source Clock versus DLL

Various end-product offerings may support different operational modes on the DDR interface. This may include (1) DLL method only, (2) source clock only, or in certain instances, (3) both options.

Ideally, for products supporting the source clock method this option is typically the preferred method, especially for designs operating at the max memory interface speed. For new designs, and products supporting the source clocked option, Freescale recommends using this option.

The key advantage in using source clock is that the designer does not have to include worst case I/O output timings (that is, tco_min, tco_max) as part of the overall timing analysis. In source clock operation, memory clocks, address, command, and control signals are all launched by similar output gates. As such, over process, voltage and temperature, all signals are subject to the same degradation effects. For example, the clock-to-outs for the clock and the other signals, with no external load, will be nearly identical when examined at the pins of the controller. The only addition item needing to be considered by the board designer is the worst case skew parameters between the signal groups and the clock group. These skew parameters are documented within the electrical specification for a given product. Based on difference in loading between the clock group and the address, command, and control groups, the DDR controller allows programmable offsets of 0, 1/4, 1/2, 3/4, and 1 full clock to be added. If needed, any further positioning of the clock within the eye can be achieved by PCB trace differences. Figure 23 shows a relative example of source clock versus DLL by comparing margins within the eye budget.

NOTE

For the rest of this document any unique timing considerations between the DLL and source clock modes are noted as needed. In instances where no distinction is made, it is assumed the section applies to both the DLL and the source clock modes.

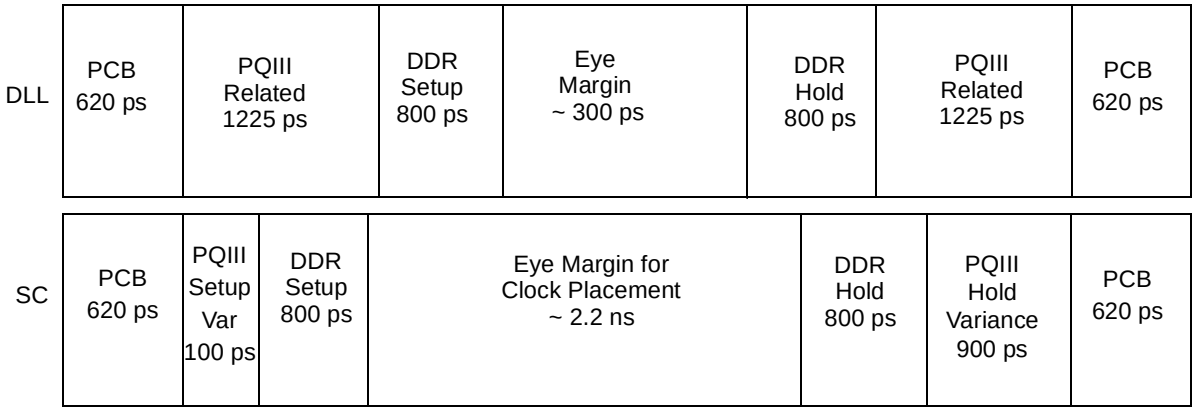

Figure 23. DLL versus Source Clock Method—Address Eye Margin Example

NOTE

PCB consumption varies from board to board (based on loading, SSO, cross-talk, etc.). See the interconnect parameter field in Table 18 for the breakdown.

10.2 Address, Command, and Control Design Considerations

This section covers the single-cycle address/command, eye diagrams, setup and hold timing analysis, the 2T timing option, and the extrapolated eye margin.

10.2.1 Single-Cycle Address/Command

Capacitive loading on the address/command bus can severely degrade the effective eye opening for the designer system timing budget. Caution should be taken during the simulation phase to ensure that the memory loading does not violate the overall budget. This concern is especially crucial for memory interfaces operating in the 266–333 MHz, but is not necessarily limited to this specific range. In achieving a single-cycle address/cmd window, two design aspects are of key interest to the board designer:

- Wide enough address/command/control eye to account for worst case interface parameters
- Positive margin for setup and hold timing budgets

These topics are discussed in the following sections.

10.2.2 Address/Cmd/Control Eye Diagram Analysis

Systems running at the higher frequencies experience a reduced eye diagram for the address/command signals as a direct result of smaller clock period, loading and reflections. Reflections are caused by impedance mismatches inherent in the address/command tree branches present on unbuffered DIMM module (or discrete) designs. The most prominent impedance mismatch occurs on the bus segment between the controller and that of the loaded memory area where the tree structure routes exists.

To account for all the board parameters properly, the designer must construct an eye diagram budget. Having such a budget enables the designer to determine whether a given implementation will provide positive margin over all worst case constraints.

Table 18 and Table 19 enumerate the specific break-downs for the example eye diagrams given in Figure 23 based on the DLL and source clock methods. Such a budget is updated by the board designer based on simulation runs of his/her specific system implementation. Using simulation, the designer can update key parameters such as the ISSI, crosstalk, and loading in tandem with fine-tuning the termination values needed to maximize the eye diagram.

Table 18. Eye Diagram Budget for Address, Command, Control—DLL Method

Skew Contributor	Skew Item	Value	Unit	Comment
Total budget	Nominal clock period description	6000	ps	Ideal Eye. Applied clock rate of 167 MHz, data rate = 333 MHz.
DDR-related	Setup/hold time requirements at memory	1600	ps	Directly from DDR data sheet
Interconnect related	ISSI, crosstalk, loading degradation	950	ps	Based on a single bank of memory with five (x16) chips
	Clock skew in system	50	ps	Ideally could be smaller if clock rules are followed
	Capacitive mismatch on inputs	25	ps	—
	V_{REF} reduction	50	ps	—
Interconnect related (continued)	Termination mismatch	15	ps	—
	Trace matching with group	150	ps	Assumes max trace delta within group of 0.75 inches * 180 ps/in
85xx related	Eye movement [1]	300	ps	Nominal amount. DLL in normal operation.
	Clock skew	150	ps	Amount of clock skew on-chip
	Clock to out spread	2000	ps	Assumes tco_min = 1 ns Assumes tco_max = 3 ns Operation: DLL method used
eye_margin	Extra margin on the eye diagram after all worst case parameters are included [2]	710	ps	—

1 Amount of time delta that does not track between the address/cmd bus and that of the DDR clocks.

2 Eye margin calculated as follows: eye_margin= Total_budget – DDR_related – Interconnect – 85xx_related.

Note: Specific product AC timing parameters used within this document are used for reference purposes only. The designer should consult the official AC specifications for their given product.

Note: For multi-bank scenarios, separate budgets need to be created between the control group and the address and command signals to account for loading differences.

Table 19. Eye Diagram Budget for Address, Command, Control— Source Clocked Method

Skew Contributor	Skew Item	Value	Unit	Comment
Total budget	Nominal clock period description	6000	ps	Ideal eye. Applied clock rate of 167 MHz, data rate = 333 MHz.
DDR-related	Setup/hold time requirements at memory	1600	ps	Directly from DDR data sheet

Table 19. Eye Diagram Budget for Address, Command, Control— Source Clocked Method (continued)

Skew Contributor	Skew Item	Value	Unit	Comment
Interconnect related	ISSI, crosstalk, loading degradation	950	ps	Based on a single bank of memory with five (x16) chips
	Clock skew in system	50	ps	Ideally could be smaller if clock rules are followed
	Capacitive mismatch on inputs	25	ps	—
	V_{REF} reduction	50	ps	—
	Termination mismatch	15	ps	—
	Trace matching with group	150	ps	Assumes max trace delta within group of 0.75 inches * 180 ps/in
85xx related	Skew delta between clock and signal group	1000	ps	Operation: source clocked method used Tperiod – (output setup with respect to MCK + output hold with respect to MCK)
eye_margin	Extra margin on the eye diagram after all worst case parameters are included [1]	~ 2160	ps	

[1] Eye margin calculated as follows: eye_margin= Total_budget – DDR_related – interconnect – 85xx_related.

Note: Specific product AC timing parameters used within this document are used for reference purposes only. The designer should consult the official AC specifications for their given product.

Note: For multi-bank scenarios, separate budgets need to be created between the control group and the address and command signals to account for loading differences.

10.2.3 Address/Command/Control Setup and Hold Timing Analysis

At 333 MHz, the applied clock that captures the address and command bus is 167 MHz, yielding a clock period of 6 ns. A key concern for board designers at this speed is meeting the single clock timing requirements for the specific memory implementation (termination, loading, PCB items, and so on).

Table 20 depicts the single clock timing issue confronting board designers at the top-end frequency. For this example, a single back of discretes is assumed with x16 components and source clock mode is used. Assuming worst case parameters, positive margin is realized.

Table 20. 1T Setup/Hold Timing for Address, Command, Control—Source Clocked Mode

Item	Description	Setup	Hold	Unit	Comment
Total budget	Nominal clock period description	3000	3000	ps	Applied clock rate of 167 MHz with for addr/cmd bus. Data rate = 333 MHz. This is the ideal eye. Assumes 1/2 clock shift setting is used between clock and signal groups.
DDR related	DDR setup requirement	800	800	ps	Directly from DDR data sheet
85xx related	Controller skew	100	900	ps	Operation: Source clocked mode

Table 20. 1T Setup/Hold Timing for Address, Command, Control—Source Clocked Mode (continued)

Item	Description	Setup	Hold	Unit	Comment
Interconnect related	ISSI, crosstalk, loading degradation	475	475	ps	Based on a single bank of memory with five (x16) chips
	Clock skew in system	25	25	ps	If discrete parts are used, clock skew <20 ps assuming clock group routing is followed.
	Capacitive mismatch on inputs	13	13	ps	—
	V_{REF} reduction	25	25	ps	—
	Termination mismatch	8	8	ps	—
	Trace matching with group	75	75	ps	Assumes max trace delta of 0.75 inches * 180 ps/in
	Time of flight delta between clock and signal group [1]	350	350	ps	Flight time delta due to loading differences and PCB trace deltas between clock and other signal groups. This is the amount not compensated for with extra PCB trace length. This number is subtracted in setup column and added in the hold margin.
Interconnect Total		971	271	ps	
Margin	Extra margin on the setup/hold [2]	1129	1029	ps	—

1 This delta along with the controller's clock shift offset can be used by the board designer to achieve the desired clock centering within the eye margin.

2 Setup_margin/Hold_margin = Total_Budget – DDR_related -Interconnect Total – 85xx_related.

Table 21 depicts the setup timing budget when using the DLL mode.

Table 21. 1T Setup Timing Analysis for Address, Command, Control—DLL Mode

Item	Description	Value	Unit	Comment
Total budget	Nominal clock period description	6000	ps	Applied clock rate of 167 MHz for addr/cmd bus. Data rate = 333 MHz. This is the ideal eye.
DDR related	DDR setup requirement	800	ps	Directly from DDR data sheet
Interconnect related	ISSI, crosstalk, loading degradation	475	ps	Based on a single bank of memory with five (x16) chips
	Clock skew in system	25	ps	If discrete parts are used, clock skew <20 ps assuming clock group routing is followed.
	Capacitive mismatch on inputs	13	ps	—
	V_{REF} reduction	25	ps	—
	Termination mismatch	8	ps	—
	Trace matching with group	75	ps	Assumes max trace delta of 0.75 inches * 180 ps/in
	Propagation delay	950	ps	—
Clock shift	Clock shifting via DLL feedback path	0	ps	Operation: DLL method used. Assumes DLL feedback path is matched to the DDR clocks

Table 21. 1T Setup Timing Analysis for Address, Command, Control—DLL Mode (continued)

Item	Description	Value	Unit	Comment
85xx related	Eye movement [1]	150	ps	Nominal amount. DLL in normal operation.
	Clock skew	150	ps	Amount of clock skew/2 on-chip
	Clock to out (max)	3000	ps	Operation: DLL method used
Setup margin	Extra margin on the setup [2]	404	ps	—

1 Amount of time delta that does not track between the address/cmd bus and that of the DDR clocks.

2 Setup_margin = Total_Budget – DDR_related – interconnect – 85xx_related ± clock shift.

Table 22 depicts the hold timing budget in the DLL mode.

Table 22. I1T Hold Timing Analysis for Address, Command, Control—DLL Mode

Item	Description	Value	Unit	Comment
DDR related	DDR hold requirement	800	ps	Directly from DDR data sheet
Interconnect related	ISSI, crosstalk, loading degradation	475	ps	Based on a single bank of memory with five (x16) chips
	Clock skew in system	25	ps	If discrete parts are used, clock skew <20 ps assuming clock group routing is followed.
	Capacitive mismatch on inputs	13	ps	—
	V_{REF} reduction	25	ps	—
	Termination mismatch	8	ps	—
	Trace matching with group	75	ps	Assumes max trace delta of 0.75 inches * 180 ps/in
	Propagation delay	950	ps	—
Clock shift	Clock shifting via DLL feedback path	0	ps	Operation: DLL method used. Assumes DLL feedback path is matched to the DDR clocks
85xx related	Eye movement [1]	150	ps	Nominal amount. DLL in normal operation.
	Clock skew	75	ps	Amount of clock skew/2 on-chip
	Hold time (Clock to out—min)	1000	ps	Operation: DLL method used
Hold margin	Extra margin on the hold [2]	304	ps	—

1 Amount of time delta that does not track between the address/cmd bus and that of the DDR clocks.

2 Hold_margin = 85xx hold_time + prop_delay ± clk_shift – (all other parameters).

10.2.4 2T Timing Option

The DDR controller supports a 2T clock timing feature for the address and command signals. This option affords the designer an extra clock cycle, allowing more heavily loaded buses to reach their valid levels. The 2T clock timing affects only the following signals: MA[14:0], BA[1:0], RAS, CAS, WE. CS, CKE, and the data bus are not affected by the double clock option. Memory termination is still present.

Table 23 depicts a timing analysis for a 2T example when in DLL mode. The large margin shows that timing is not an issue because the eye is given sufficient time to open by the second clock edge. Though not tabulated, the hold time (800 ps) is easily achieved by the minimum clock-to-out of the controller and the large capacitive load of the bus.

Table 23. 2T Setup Timing Analysis—DLL Mode

Item	Description	Value	Unit	Comment
Total budget	Nominal clock period description	12000	ps	Applied clock rate of 167 MHz with 2T for addr/cmd bus. Data rate = 333 MHz.
DDR related	DDR setup requirement	800	ps	Directly from DDR data sheet
Interconnect related	ISSI, crosstalk, loading degradation	2250	ps	Based on a dual bank of memory with x8 chips
	Clock skew in system	50	ps	Assumes DIMM module. Majority of this introduced by the DIMM module. If discrete parts are used, clock skew <20 ps assuming clock group routing is followed.
	Capacitive mismatch on inputs	50	ps	—
	V_{REF} reduction	25	ps	—
	Termination mismatch	8	ps	—
	Trace matching with group	75	ps	Assumes max trace delta of 0.75 inches * 180 ps/in
	Propagation delay	1800	ps	—
Clock shift	Clock shifting via DLL feedback path	0	ps	Operation: DLL method used. Assumes DLL feedback path is matched to the DDR clocks
85xx related	Eye movement [1]	150	ps	Nominal amount. DLL in normal operation. See Note (1).
	Clock skew	75	ps	Amount of clock skew/2 on-chip
	Clock to out (max)	3000	ps	Operation: DLL method used
Setup margin	Extra margin on the setup [2]	3792	ps	—

1 Amount of time delta that does not track between the address/cmd bus and that of the DDR clocks.

2 Setup_margin = Total_Budget -DDR_related – interconnect – 85xx_related + clock shift.

Neither the chip select, clock enable, nor the data signals are affected by the 2T option. Because MCS[0:3] and MCKE[0:1] are referenced to the interface clock, they must still meet a single clock cycle. Because both signal types are less loaded than the other DDR groups, 1T timing is more achievable for these signals. To ensure these signals meet 1T timing, the designer should construct a separate budget and simulate these signals accordingly so that proper termination and routing constraints are applied to them.

10.2.5 Extrapolated Eye Margin

This section covers eye margin for both 1T and 2T mode.

10.2.5.1 Eye Margin—1T Mode

The graph in Figure 24 extrapolates the expected worst case eye margin for various frequencies and memory configurations the address, command and control groups are run in a single cycle mode. The graph is no guarantee of final margin, but it can be used to estimate key hot spots for a given frequency

and memory configuration prior to simulation. The first column represents the option of running the controller in DLL mode with standard DDR termination techniques (R_S and R_T). The second and third columns represent the option of running the controller in source clock mode, one with standard DDR termination, and the latter using the Micron compensation method (Section 11, “Improving Eye Diagrams”). Ultimately, all interface margins must be validated through a timing budget and exhaustive board simulation.

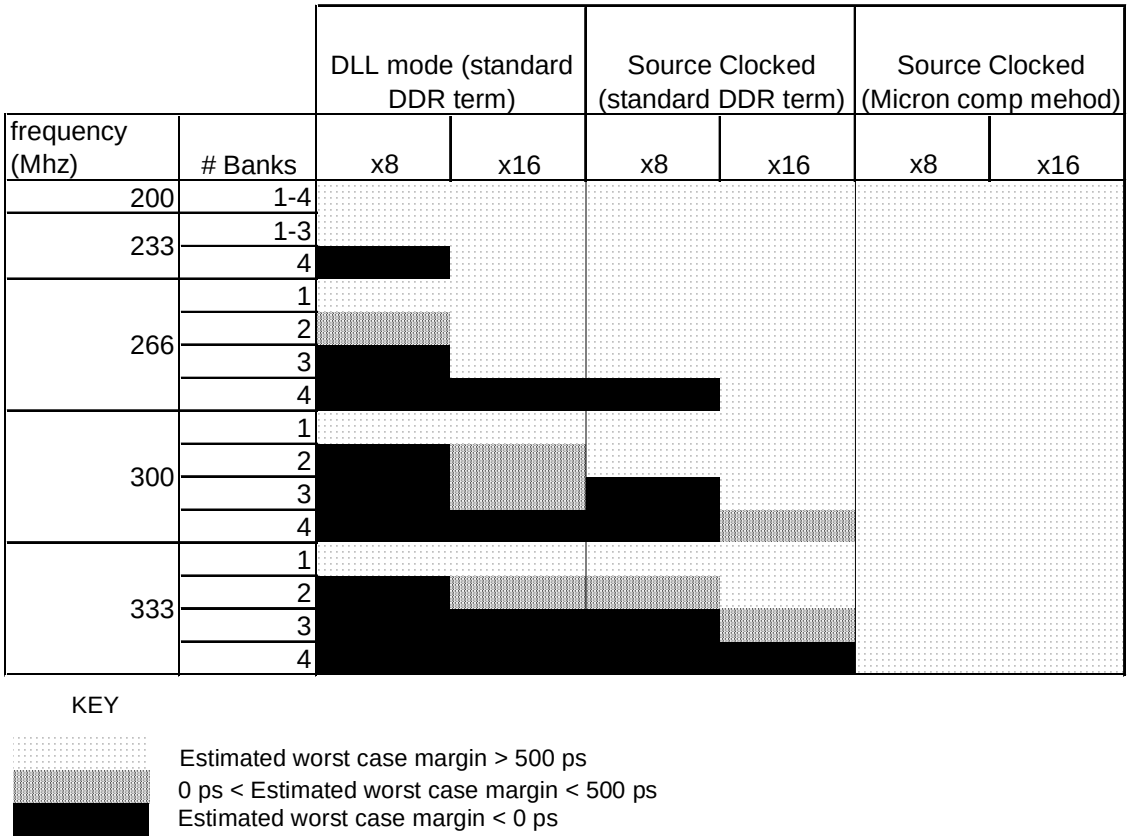

Figure 24. Extrapolated Worst Case Eye Margin Over Frequency and Loading

10.2.5.2 Eye Margin—2T Mode

An extra clock period is given for all the address and command signals, so plenty of eye margin is available across all frequencies and memory configurations. Note that neither the chip select, clock enable, nor the data signals are affected by the 2T option. Because MCS[0:3] and MCKE[0:1] are referenced to the interface clock, they must still meet a single clock cycle. Because both signal types are less loaded than the other DDR groups, 1T timing is more achievable for these signals. To ensure that these signals meet 1T timing, construct a separate budget and simulate these signals accordingly so that proper termination and routing constraints are applied to them.

10.3 Data Group Timing Analysis

For DDR timing, the read path is the limiting case in determining the signal length variance. Figure 25 shows the input timing at the DDR controller, and Table 24 enumerates the read skew timing budget for a system interface operating at 333 MHz.

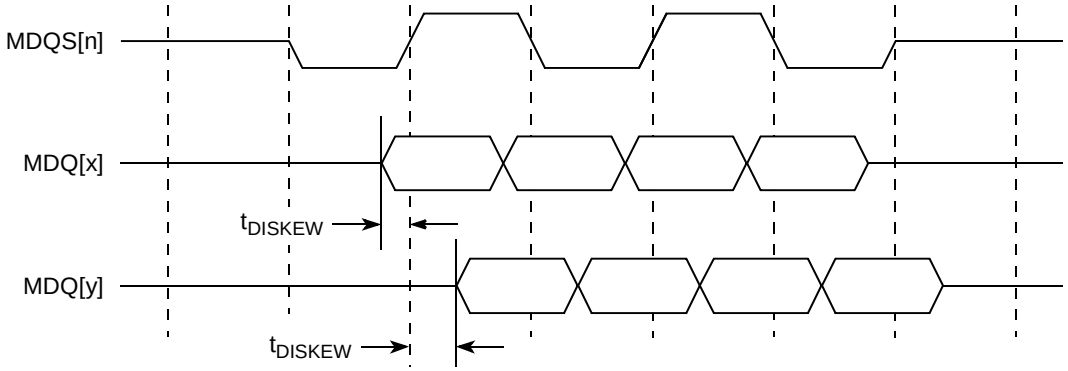

Figure 25. Input Timing Diagram at the DDR Controller—Read Case

Table 24. Read Timing Budget—Assuming 333-MHz Interface

PCB/Interconnect Skew Component	Setup	Hold	Unit	Comment
Crosstalk	100	100	ps	—
Data group trace mismatch [1]	10	10	ps	—
ISI (Intersymbol interference)	25	25	ps	—
Termination mismatch (V_{OH}/V_{OL})	15	15	ps	Termination mismatch error that reduces the input eye.
Eye reduction	100	100	ps	V_{REF} mismatch error, termination error, and eye reduction due to slew rate differences between DQS and DQ
Total Board Skew	250	250	ps	—
DRAM output skew (t_{DQSQ})	450	450	ps	From DDR data sheet.
DDR controller input skew requirement (t_{DISKEW})	750	750	ps	Assumes a 6-ns clock period is used
Read Timing Margin	50	50	ps	Margin = controller requirement – DRAM – board skew

1 The key factor that drives the tight trace matching within a byte lane is the interface frequency, which in turn drives the input skew requirements at the DDR controller. Designs operating at a slower interface can potentially relax the trace matching somewhat if all other skew components are held in tolerance.

Figure 26 shows the output timing from the DDR controller, and Table 25 enumerates the write skew timing budget for a system interface operating at 333 MHz.

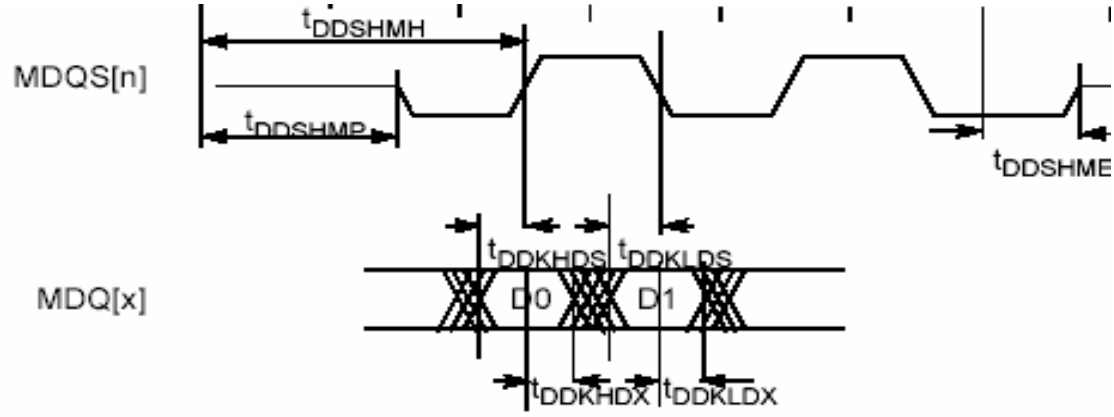

Figure 26. Output Timing Diagram from the DDR Controller—Write Case

Table 25. Write Timing Budget—Assuming 333-MHz Interface

PCB/Interconnect Skew Component	Setup	Hold	Unit	Comment
Crosstalk	100	100	ps	—
Data group trace mismatch [1]	10	10	ps	—
ISI (Intersymbol interference)	25	25	ps	—
Termination mismatch (V_{OH}/V_{OL})	15	15	ps	Termination mismatch error that reduces the input eye
Eye reduction	100	100	ps	V_{REF} mismatch error, termination error, and eye reduction due to slew rate differences between DQS and DQ
Total Board Skew	250	250	ps	—
DRAM setup/hold (t_{DS}/t_{DH})	450	450	ps	From DDR data sheet
DDR controller setup/hold	900	900	ps	Assumes a 333-MHz DDR interface is used
Write Timing Margin	200	200	ps	Margin = DDR controller – DRAM requirement – board skew

1 The key factor that drives the tight trace matching within a byte lane is the interface frequency and the read system timing budget (see Table 24). Designs operating at a slower interface can potentially relax the trace matching somewhat if all other skew components are held in tolerance.

10.3.1 Meeting the 75%–125% Write Data JEDEC Window

Besides the timing constraints noted in Section 10.3, "Data Group Timing Analysis," JEDEC also defines a fairly loose relationship between the data strobes and the applied DDR clock at the memory device. Specifically, the time between the WRITE command and the first corresponding rising edge of the DQS (t_{DQSS}) is specified with a relatively wide range (from 75% to 125% of 1 clock cycle). This relationship is illustrated in Figure 27.

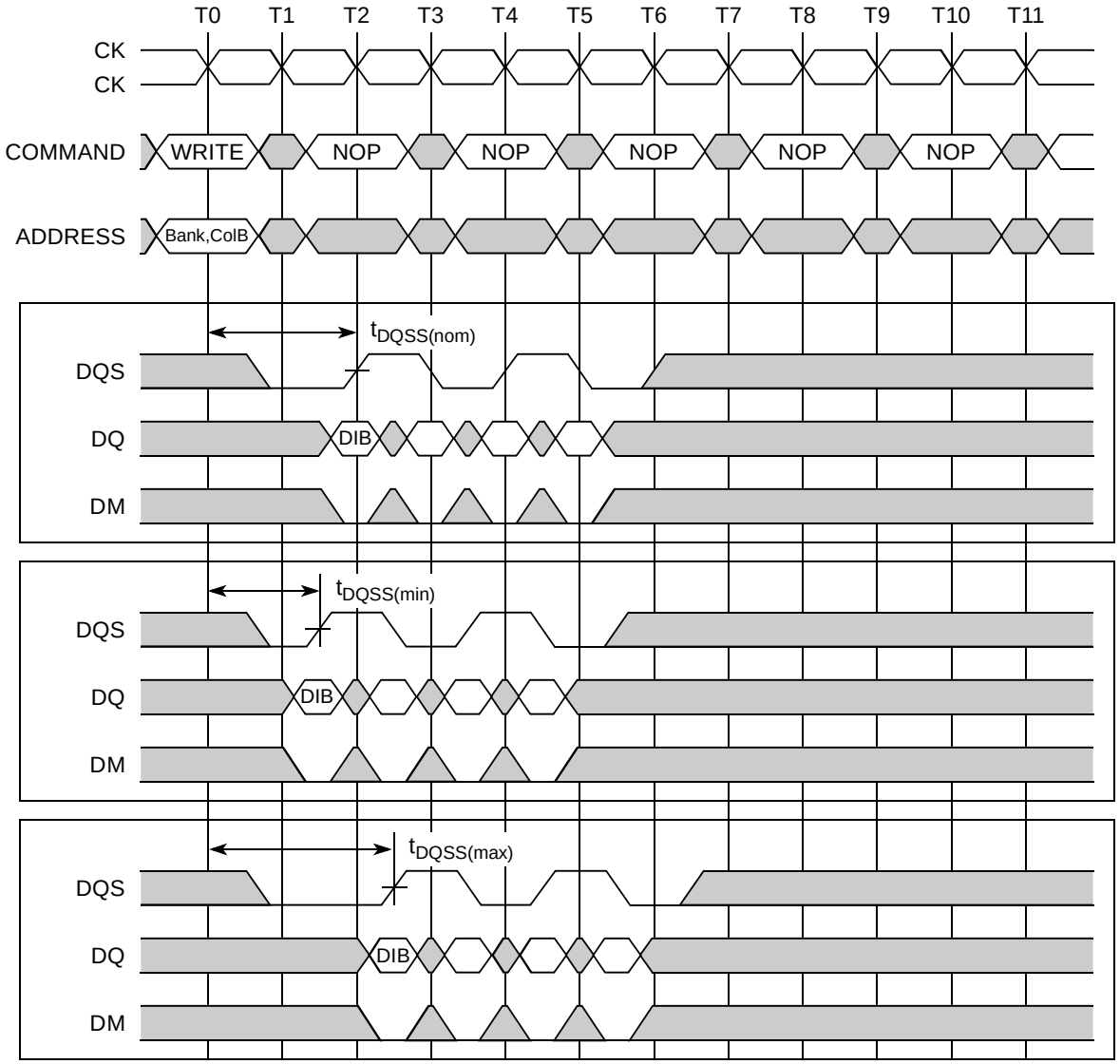

Figure 27. DDR JEDEC Write Window 75%–125%

The minimum shown above refers to the 75% window and the maximum above refers to the 125% window. To help the designer meet the JEDEC window requirement, the DDR controller has a write data delay configuration (WR_DATA_DELAY) option as part of the TIMING_CFG_2 register. This delay option allows the write command to write data strobe timing to be adjusted in increments of 1/4, 1/2, 3/4, and 1 full clock cycle. This option provides the designer with a course adjustment, and is used in both the DLL and source clocked modes.

10.3.2 Meeting the JEDEC Write Window—DLL Mode

For systems using the DLL option the WR_DATA_DELAY option will typically need to be set between 1/2 and 3/4 depending on the interface frequency, capacitive loading delta, and trace skew deltas between the clock and the data group.

Besides the course adjustment mentioned above, the designer may also need to have some additional skew between the clock group and that of the DQS[0:8]. The DQS output timing is the minimum/maximum time for the DQS strobes to become active after a rising edge of the clock. This output timing relationship is specified within the device's data sheet. For reference, Table 26 provides several different interface examples that show how the JEDEC window can be met using a combination of different write delay settings and group skewing. In creating the table it is assumed that all DQS strobes to the memory subsystem are perfectly matched. Secondly, the DDR memory clocks are assumed to be perfectly matched with no DLL offset (that is, DLL feedback path is the same length as the MCKs). In cases where this is not true, these additional factors should be incorporated into the analysis.

Table 26. Meeting the JEDEC Write Data Window in DLL Mode—Write Data Delay + PCB Skew

Col. A Period (ns)	Col. B JEDEC 75% (ns)	Col. C JEDEC 125% (ns)	Col. D DQS Min (ns)	Col. E DQS Max (ns)	Col. F Write Delay	Col. G Additional Skew (ps) (clk-to-DQS)	Col. H Design 75% A*F+D+G (ns)	Col. I Design 125% A*F+E+G (ns)
10.0 (200 MHz)	7.50	12.50	1.5	4.0	3/4	0	9.0	11.5
8.7 (230 MHz)	6.52	10.87	1.5	4.0	3/4	0	8.0	10.5
7.5 (266 MHz)	5.63	9.40	1.5	4.0	1/2	450	5.7	8.2
6.6 (300 MHz)	5.00	8.33	1.5	4.0	1/2	300	5.1	7.6
6.0 (333 MHz)	4.50	7.50	1.5	4.0	1/2	0	4.5	7.0

All time references for the JEDEC window in Table 26 pertain to the T0 clock edge shown in Figure 27. Columns B and C show the design requirement per the JEDEC specification. Columns D and E represent the DQS min/max numbers directly from the device data sheet. The example shown above is for the MPC8540/8560. Refer to the device electrical specifications for the most accurate DQS_min/max timings. Column G is the extra skew achieved by the PCB trace delta between the clock and data groups. Columns H and I represent the implemented window that is achieved based on the write delay register setting (column F) and PCB group skewing.

10.3.3 Meeting the JEDEC Write Window—Source Clocked Mode

For systems using the source clocked option, the WR_DATA_DELAY option will typically be set between 1/2 and 3/4 depending on the interface frequency, capacitive loading delta, and trace skew deltas between the clock and the data group. For the majority of settings, the WR_DATA_DELAY setting will be set to the same value as the clock adjust in the CLK_CNTL register.

To ensure that the write data window is always satisfied, the data group must maintain a certain relationship to the clocks in the memory system. This relationship translates to a the amount of skew that is permitted between the data group and the memory clocks. For reference, Table 27 provides several different interface examples that show how the JEDEC window can be met. In creating the table, it is assumed that all DQS strobes to the memory subsystem are perfectly matched. If this is not the case, then the max DQS skew delta should be incorporated into the table.

Table 27. Meeting the JEDEC Write Data Window in Source Clocked Mode

Col. A Period (ns)	Col. B JEDEC 75% (ns)	Col. C JEDEC 125% (ns)	Col. D DQS Min Skew to clk (ns)	Col. E DQS Max Skew to clk (ns)	Col. F Delta Time Between Col. B and Col. D (ns)	Col. G Delta Time Between Col. C and Col. E (ns)	Col. H Maximum Clk-to-DQS Trace Skew Permitted Min (F, G) (ps)
10.0 (200 MHz)	2.50	2.50	0.9	0.3	1.6	2.2	1600
8.7 (230 MHz)	2.175	2.175	0.9	0.3	1.275	1.875	1275
7.5 (266 MHz)	1.875	1.875	0.9	0.3	.975	1.575	900
6.6 (300 MHz)	1.66	1.66	0.9	0.3	0.76	1.36	760
6.0 (333 MHz)	1.50	1.50	0.9	0.3	0.6	1.2	600

All time references for the JEDEC window inTable 27 pertain to the T2 clock edge shown in Figure 27. Columns B and C show the design requirement per the JEDEC specification. Columns D and E represent the DQS min/max skew numbers with reference to the memory clocks. This is taken directly from the device data sheet. The example shown above is for the MPC8540/8560. Refer to the device electrical specifications for the most accurate DQS skew timings. Columns F and G represents the skew on other side of the T2 clock which is allowable. Column H gives the worst case skew permissible between all DQS strobes and the memory clocks, by taking the minimum of columns F and G. It, therefore, represents the worst case skew allowed for trace differences, loading deltas, etc., between the clock and the DQS strobes.

10.4 Max Clock Trace Length Guidelines for Source Clock Mode

Besides the external timing constraints outlined above, when using source clock mode there are other non-apparent timing relationships that must also be met. An example of such would be meeting the controller's input enable timing window during read transactions, which is a non-visible window to the board designer. Such non-apparent timing relationships can be easily satisfied by limiting the max clock trace length used when constructing the memory topologies. This is possible because the all other DDR signal groups will maintain a certain relationship to the clock group when running in source clock mode. See Table 28 for guidelines on max clock lengths when using source clock mode.

Table 28. Max Trace Lengths for the DDR Memory Clocks—Source Clock Mode

Col. A Period (ns)	Max Clock Length in Inches Assuming 150–200 ps/in.
10.0 (200 MHz)	<= 12
8.7 (230 MHz)	<= 12
7.5 (266 MHz)	<= 10
6.6 (300 MHz)	<= 10
6.0 (333 MHz)	<= 10

11 Improving Eye Diagrams

Micron has developed a modified termination technique called a ‘compensated bus topology.’ The overall approach is described in Volume 11, Issue 2 of their DesignLine publication titled, *DDR333 Memory Design Guide for Two-DIMM Unbuffered Systems*.

To summarize the approach: the series damping resistor (R_S) is replaced with a capacitor tied to ground in the compensated bus topology. The capacitor’s use allows the effective impedance of the transmission line to be more closely matched to the tree topology used at the memories. Without R_S present, the inherent RC slew effects of the signal are improved. Both effects, a better matched transmission line coupled with a better slew rate, enable the signal eye diagram to be greatly enhanced. This specific topology is illustrated in Figure 28.

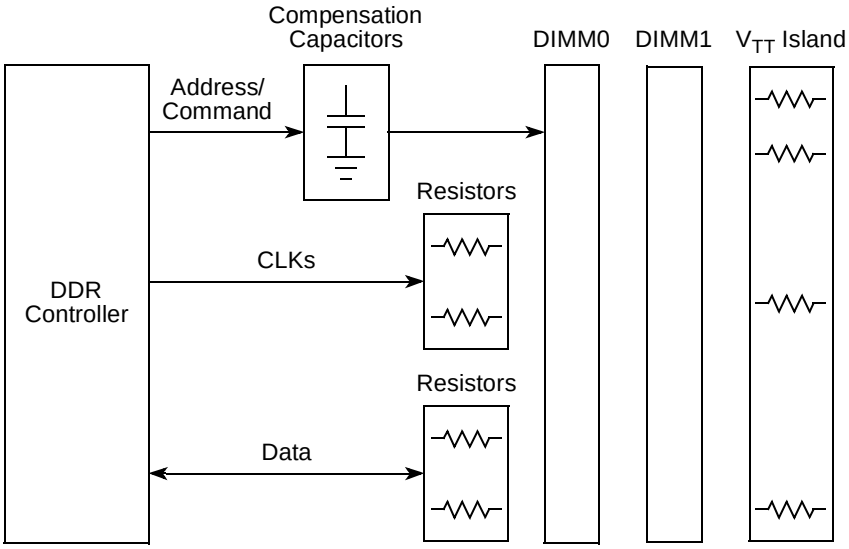

Figure 28. Memory Block Diagram using the Compensated Bus Technique

11.0.1 Layout Guidelines for Using the Compensation Method

Figure 29 shows the modified group topology for systems leveraging the compensation method. Figure 29 is a simple side view representation for the address/command bus, and it does not show the tree structure on the DIMM modules, nor does it show the tree structure routes that would be required on the PCB motherboard for the discrete memory scenario.

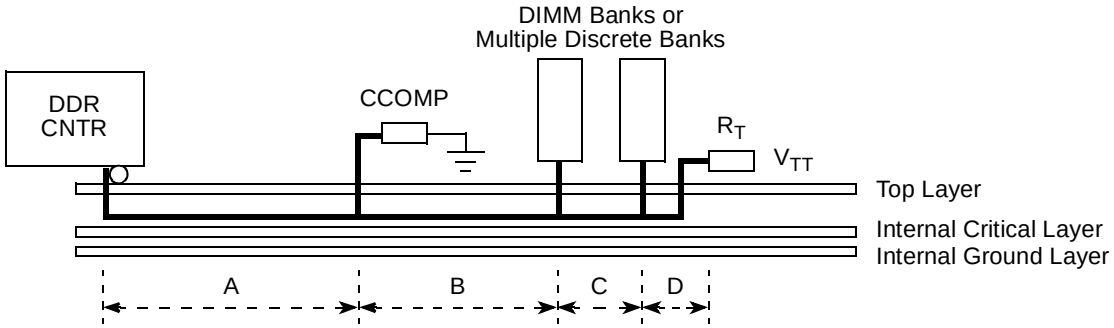

Figure 29. DDR Address/Command Routing Topology with Compensation Capacitor

All previous design guidelines enumerated in this document for the address and command bus remain the same with the exception of the following items:

1. The series damping resistor (R_S) is removed.
2. A compensation cap is added to the address/cmd trace segments between the controller and the first memory bank. Placement of the cap should split the difference between the controller and the first memory bank.
3. The exact value for the compensation cap should be determined by means of board level simulations. A general range that Micron suggests is 45–82 pF.
4. The designer should ensure that this new capacitive element is properly incorporated into the system budget.

12 Simulation

This application note provides general hardware and layout considerations for hardware engineers implementing a DDR memory subsystem.The rules and recommendations in this document can serve as an initial baseline for board designers who begin their specific implementation. Numerous memory topologies and interface frequencies are possible on the DDR interface, so Freescale highly recommends that the board designer, through simulation, verify that all aspects (signal integrity, electrical timings, and so on) are addressed before board fabrication.

In tandem with memory vendors, Freescale provides IBIS models for simulation. The board designer can realize a key advantage during simulation, which is the ability to gain extra noise and timing margins by optimizing the termination values on the interface. Because SSTL-2 noise margins are extremely small, the extra time spent optimizing the termination scheme is well worth it.

During board simulation, the board designer should verify that all aspects of the signal eye are satisfied (see Figure 30), which includes at a minimum the following:

- A sufficient signal eye opening meeting both timing and AC input voltage levels
- Vswing max not exceeded (or alternatively max overshoot/max undershoot)
- Signal slew rate within spec

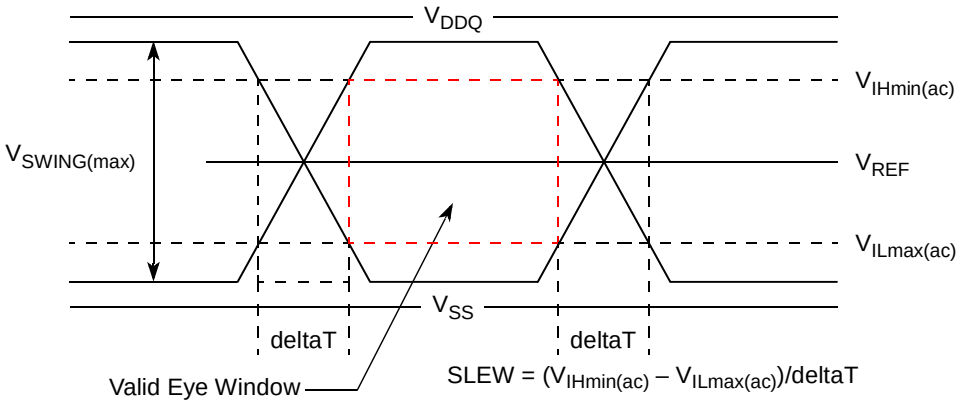

Figure 30. SSTL Signal Wave Form

As a starting place for the board designer, Table 29 provides some typical ranges for the various termination elements.

Table 29. Simulation Ranges for the DDR Signal Groups

Group	Series Resistor (R_S) in Ω	Parallel Resistor (R_T) in Ω	Compensation Capacitor (C_{COMP})
Clocks	22–36	Optional—25–57	N/A
Data	0–33	25–57	N/A
Address/command	0–36	25–57	N/A
Address/command (compensation method)	—	25–57	30–80 pF
Control	0–36	25–57	—
Feedback	15–33	Optional—25–57	N/A

NOTE

R_S and C_{COMP} are mutually exclusive. The compensation technique can be employed for improving the effective eye diagram. See Section 11, "Improving Eye Diagrams."

13 DDR Designer Checklist

Freescale recommends that designers use this document and the latest errata for additional items that may need consideration.

Table 30. DDR Designer Checklist

Item #	Description	Yes/No
	Simulation	
1.	Using simulation, have optimal termination values, signal topology, along with trace lengths been determined for each signal group in the specific memory implementation?	
2.	Does the selected termination scheme meet the AC signaling parameters (voltage levels, slew rate, overshoot/undershoot) across all memory chips in the design?	
	Termination Resistors Note that within the context of this document, it is assumed that the designer is using the mainstream termination approach as found in commodity PC motherboards. Consequently, differing termination techniques may also prove valid and useful, but are left to the designer to validate using simulation.	
3.	Is the worst case power dissipation for the termination resistors within the manufacturer's rating for the selected devices?	
4.	If resistor packs are used, have data lanes been isolated from the other DDR signal groups?	
5.	Have resistor packs been properly placed? The R_T terminators should directly tie into the V_{TT} island at the end of the memory bus. DIMM based systems— If R_S terminators are used, were they placed close to the first memory bank? Discrete based systems—Placement of the series damping resistor (R_S) for the data group is left to the board designer. This trade-off comes in the form of achieving optimal signal integrity for both reads/writes (R_S in middle) vs. ease of layout routing (R_S placed closer to memory devices).	

Table 30. DDR Designer Checklist (continued)

Item #	Description	Yes/No
6.	Is the differential terminator present on the clock lines for discrete memory populations? (DIMM modules contain this terminator.) Dependent on target impedance (typically between 100–120 Ω).	
7.	Is a series damping resistor present on the DLL feedback path (MSYNC_OUT to MSYNC_IN)? Resistor should be placed close to the source pin (MSYNC_OUT). Typically, a resistor of 33 Ω serves as a good value. If available, it is recommended to do this even if the designer plans to use the source clock mode.	
8.	Highly suggested/recommended that the designer place a resistor of 0 Ω at the MSYNC_IN pin. Such flexibility allows the feedback path to be easily adjusted (if needed) during the prototyping phase by removing this resistor and the series damping resistor noted item 7. If available, it is recommended to do this even if the designer plans to use the source clock mode.	
9.	Optional—Parallel terminators (to V_{TT}) for the DDR clock group and the DLL feedback path.	
V_{TT} Related Items		
10.	Has worst case current for the V_{TT} plane been calculated based on the design's termination scheme?	
11.	Is the V_{TT} regulator capable of supporting the steady state and transient current needs of the design?	
12.	Has the V_{TT} island been properly decoupled with high frequency decoupling? At least one low ESL cap, or two standard decoupling caps for each 4-pack resistor networks (or every 4 discrete resistors) should be used. In addition, at least two 4.7 µF caps should be at each end of the V_{TT} island.	
13.	Has the V_{TT} island been properly decoupled with bulk decoupling? At least one bulk cap (100–220 µF) capacitor should be at each end of the island.	
14.	Has the V_{TT} island been placed at the end of memory channel and kept as close as possible to the last memory bank?	
15.	Has a wide surface trace (~150 mils) been used for the V_{TT} island trace?	
16.	If sense pin is present on the V_{TT} regulator, attach it in the middle of the island.	
V_{REF}		
17.	Has V_{REF} been routed with a wide trace? (minimum of 20–25 mil recommended)	
18.	Has V_{REF} been isolated from noisy aggressors? In addition, maintain at least a 20–25 mil clearance from V_{REF} to other traces. If possible, isolate V_{REF} with adjacent ground traces.	
19.	Has V_{REF} been proper decoupled? Specifically decouple the source and each destination pin.	
20.	If a resistor divider network is used to generate V_{REF}, are both resistors the same value and 1% tolerance?	
Routing		
21.	Have the clock pair assignments been optimized to allow break-out of all pairs on a single critical layer?	
22.	To facilitate fan-out of the DDR data lanes, are alternate adjacent data lanes on different critical layers?	
23.	Have all the DDR signal groups been properly referenced to a solid ground plane? Trade-offs can be made for the non-data signal groups that can be referenced to a solid power plane (without splits under the DDR track).	
24.	Has each byte lane + data mask been properly trace matched to its respective data strobe? (±25 mils recommended for highest frequency operation)	
25.	Have all the data lanes been tuned to the clock reference? (±0.5 inches for highest frequency operation)	

Table 30. DDR Designer Checklist (continued)

Item #	Description	Yes/No
26.	Have all other DDR signal groups been tuned to the clock reference? As this is loading and topology dependent, the variance around the clock should be determined by means of simulation.	
27.	Have the differential clocks been properly routed? For example, the correct differential spacing, serpentine isolation, and group spacing have been met? Was the series resistor placed properly?	
28.	Have all clock pairs been routed on the same critical layer?	
29.	Have MCK to $\overline{\text{MCK}}$ been properly trace matched to within 20 mils?	
30.	Have all clock pairs to a given memory bank (discrete or DIMM) been properly trace matched?	
31.	Has the feedback clock for the DLL (MSYNC_OUT to MYSNC_IN) been properly trace matched to the clock length of the DDR clocks? If available, it is recommended to do this even if the designer plans to use the source clock mode.	
32.	If using the source clock option, has the maximum clock lengths been observed from Table 28.	
Miscellaneous Items		
33.	Keep the memory channel (area between controller and the memory) free of noisy and high frequency components (ideal case is to place only memory terminators and decoupling within this area).	
Registered DIMM Topologies (All Items Above Still Apply)		
34.	For memory implementations that plan to utilize registered DIMM modules, the board designer should attach a reset signal to the DIMM sockets. This reset signal should be derived from a ‘power good’ monitor status circuit.	
35.	Though registered DIMMs only require a single clock per bank, all DDR clock pairs at the DIMM connector should be attached (analogous to unbuffered DIMMs). Potentially allows the design to support unbuffered DIMMs (at slower speeds).	
Discrete Memory Topologies (All Items Above Still Apply With Exception of Registered DIMM Items)		
36.	Construct the signal routing topologies for the groups like those found on unbuffered DIMM modules.	
37.	As an initial starting place for simulation, leverage the general guidelines given in Section 7, “Layout Guidelines for the Signal Groups.”	
38.	If a single bank of x16 devices are used, let the DDR clocks be point-to-point. Place the series damping resistor (R_S) close to the source and the differential terminator (R_{DIFF}) at the input pins of the discretes. • If more than four discretes are used, construct the clocks like those found on unbuffered DIMM modules. • Alternatively, place an external PLL between the controller and the memory to generate the additional clocks.	
39.	When placing components, optimize placement of the discretes to favor the data bus (analogous to DIMM topologies). Optional: Pin-swap within a given byte lane so as to further optimize the data bus routes. **Caution:** Do not swap individual data bits across different byte lanes.	
40.	If multiple physical banks are needed, double stack (top and bottom) the banks to prevent lengthy and undesirable address/cmd topologies.	
41.	Properly decouple the DDR chips per manufacturer recommendations. Typically, five low ESL capacitors per device are sufficient. For further information, see article entitled, *Decoupling Capacitor Calculation for a DDR Memory Channel*, located on Micron’s web site.	
42.	To support expandability into larger devices, ensure that extra NC pins (future address pins) are connected.	

14 Useful References

1. DDR chapter of the *MPC8560 PowerQUICC III Integrated Communications Processor Reference Manual*
2. Micron web site: http://www.micron.com. Lots of good application notes and DDR publications. Examples include:
   - *Calculating Memory System Power for DDR SDRAM*
   - *DDR333 Memory Design for Two-DIMM Unbuffered Systems*
   - *Decoupling Capacitor Calculation for a DDR Memory Channel*
3. JEDEC web site: http://www.jedec.com
   - DDR SDRAM Registered DIMM Specification
   - DDR SDRAM Unbuffered DIMM Specification
   - JESD79—DDR SDRAM Specification Release 2 (Feb. 2/00)
   - JESD8-9 SSTL2 Specification
4. Tektronix
   - TLA700 System User's Manual; Logic Analyzer User's Manual
   - *TMS568 Support Guide: Local Bus and DDR Support*
   - *P6810, P6860, and P680 Logic Analyzer Probes Manual*
5. MOSAID Technologies Inc.
   - *DDR SDRAM—An Interpretation of the JEDEC Specification*
6. *NEX-DDRHS User's Manual* (New Wave Technologies)
   - Manufacturer of DDR adapter cards http://www.busboards.com

15 Revision History

Table 31 provides a revision history for this document.

Table 31. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release for internal review.
1	Updated from internal feedback.
1.1	Nontechnical reformatting. Initial release to external customers.
2	• Created more comprehensive eye and timing budgets, including a new write data timing budget, an updated read data budget, and eye and timing budgets for the address/cmd bus. • Revamped Section 10 into two modified Sections, 10 and 11. Section 10 discusses the key concerns associated with meeting single-cycle access on the address/cmd bus versus system loading. Section 11 now incorporates all the additional design considerations not specifically covered elsewhere. • Added recommendation to include a resistor of 0 Ω at pin of MSYNC_IN to facilitate adjusting the DLL feedback path during board prototyping and debug. • Added Section 10.3.2, "Meeting the 75%–125% Write Data JEDEC Window." • Added information about the hold timing budget. • Nontechnical reformatting.

Table 31. Document Revision History (continued)

Rev. No.	Substantive Change(s)
3	• Moved all timing interface related items to Section 10, “Interface Timing Analysis and Other Considerations.” • Added interface considerations needed for using the DDR controller’s new source clock mode—new timing budgets, clock length constraints, and JEDEC write window. • Comments added regarding DLL versus source clock. • Added an extrapolated address/command margin graph.
4	• Updated Motorola references to Freescale and put in new template. • Deleted Section 6.1. • Removed NOTE from Section 6.2. • Deleted Section 16.
5	• Corrected values in Table 2 for strobe length, maximum clock length, and minimum clock length.
6	• Removed section 7.8.2 - List of potential VTT regulators. • Updated note (3) of Table 2.

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