Using the MPC5200 for High-Speed Video-Detection Applications in a Vehicle

Automotive OEMs are relying increasingly on processing high-speed video images captured both within the interior and exterior of the vehicle. For example, cameras mounted within the vehicle may be used to determine an occupant's position in the vehicle to optimally deploy airbags and avoid passenger injury. Cameras mounted in various positions of the vehicle may also be used for lane-departure detection, pre-crash warning, collision avoidance, rear backup warning, vehicle-distance calculation, etc. Many of these applications require the capture of video images at very high rates. In turn, the video images must be processed by sophisticated algorithms in real time to provide feedback to safety control systems within the vehicle. This is an especially daunting task in the timeframe required to avoid a crash or make a decision on an occupant's position in the vehicle during a crash. Moreover, this technology must endure temperatures of up to 85 C within the driver's side of the engine firewall and up to 105 C elsewhere in the vehicle.

The challenge facing automotive OEMs is securing a cost-effective technology that supplies the following characteristics:

- Support of a standardized high-speed interface to CMOS video sensors
- Sufficient processing power
  — Ample MIPS to execute video detection algorithms in required time
  — Double Precision Floating Point Unit (FPU) to boost algorithm execution speed
- DMA capability to read complete pictures
  — Reduce the amount of interrupts and boost overall data throughput
  — Accelerate access to fast memory systems
  — Offload processor core from handling routine data movement functions

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- Next generation Double Data Rate (DDR) memory support for fast data storage and retrieval
- Cost-effective, high-speed connection to safety devices (airbags, etc.)
  — Integrated CAN and J1850 BDLC to reduce latency of data transmission and overall system cost
  — Expansion to next generation automotive networks such as Media Oriented Systems Transport (MOST®)
- Ability to operate at 85 C and 105 C degree Ta, depending on the location of the imaging sensor
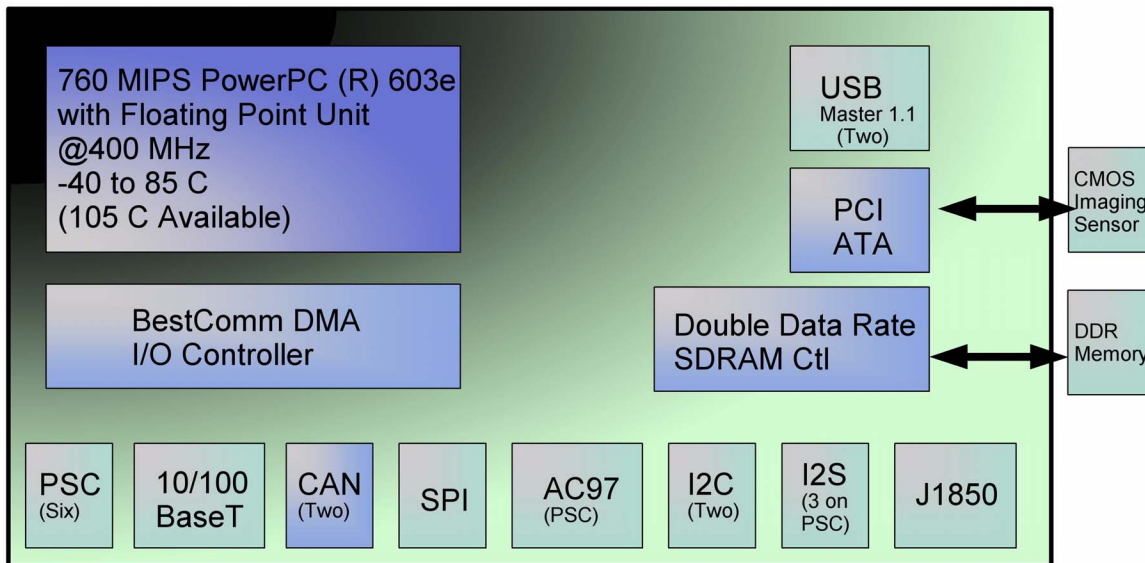- Potential requirement for low-power operation

Figure 1. Block Diagram

The MPC5200 high-performance embedded processor from Freescale Semiconductor, Inc. (formerly Motorola) specifically meets all of these design challenges in one compact, low-power device.

Specifically, the MPC5200 integrates a high performance MPC603e core capable of processing 760 Dhrystone 2.1 MIPS at 400 MHz at a temperature range of –40 to 85 C. The PowerPC® core also utilizes a high-performance, double-precision Floating Point Unit (FPU) to accelerate complex math operations in parallel with other critical tasks. A 105 C version operating at 264 MHz (500 MIPS) is also available for use outside of the driver compartment where higher-temperature ratings may be required.

The MPC5200 processing power, aided by the FPU, provides ample horsepower for most video-detection algorithms. An integrated PCI interface provides a standardized high-speed interface to CMOS image sensors, capable of bringing image data into the MPC5200 at the rate of 80–100 frames per second, depending on the PCI clock and the picture resolution.

The BestComm intelligent DMA controller accelerates the transfer of camera data to memory for algorithmic processing, with minimum taxation on the main MPC603e processor core, leaving it free to process video-detection algorithms and other tasks. The use of the BestComm controller also minimizes the overall interrupt load placed on the main core, thereby speeding overall throughput. An integrated

CAN and J1850 controller in addition to external MOST® support provides for cost-effective integration to the rest of the car's safety systems, while reducing latency in communications to those networks.

The remainder of this article describes how to design a basic high-speed camera-interface circuit to the MPC5200 via its PCI interface. In this example, a Freescale (formerly Motorola) MCM20014 CMOS sensor is used, but other sensors will use nearly identical interface schemes.

The interface is straightforward and requires only a small amount of interface logic to complete the connection.

1 Clock Assumptions Using the MPC5200

The maximum possible XLB release-target frequency is 132 MHz; IPBus is 66 MHz; PCIclk (external bus clock) is 66 MHz. The expected XTAL input frequency is 33 MHz.

For this application, the maximum PCI frequency is 33 MHz.

The clock selection represents a hierarchy of possible 4-1, 2-1, or 1-1 divide ratios as follows: XLB->IPBus, IPBus->PCIclk. At 132 MHz XLB, IPBus must be set to 4:1 or 2:1 (for 33 MHz or 66 MHz IPBus respectively). PCIclk may be 1:1 or 2:1, which is enabled, depending on the IPBus (33 MHz, 16.5 MHz working with a 33 MHz IPBus, or 33 MHz working with a 66 MHz IPBus). A 66 MHz PCIclk from the processor side is possible, but the image sensors available at the time of this writing are simply not that fast.

- PWM outputs to generate HCLK can only be even-integer divisions of the IPBus clock if a 50-percent duty cycle is required.

NOTE

Burst transactions from BestComm to XLB are performed at the XLB frequency, but data from Peripheral is fetched by BestComm at the IPBus frequency.

- Examples of possible clock relationships:

  XTAL: 27 MHz, XLB: 108 MHz, IPB: 54 MHz, PCI: 27 MHz, HCLK: 13.5 MHz (PWM at 4/1 divide ratio from the IPBus clock)

  XTAL: 33 MHz, XLB: 132 MHz, IPB: 66 MHz, PCI:33 MHz, HCLK:8.25 MHz (PWM at 8/1 divide ratio from the IPBus clock)

The XTAL input can be varied to produce different operating frequencies, but the HCLK of 8.25 MHz should be suitable for the camera; it also provides a 4:1 difference between the DMA clock and the sensor data rate (PCIclk to HCLK). This helps with potential bandwidth problems that may occur.

The approach is to provide interface logic between the sensor data bus and the PCI data bus. Sample circuits are provided for the 2:1 and 4:1 cases. The interface logic is quite simple with the MPC5200. However, there are a few system-application issues which must be considered.

One consideration is whether the PCI bus will be used for anything other than camera data transfers. If the PCI bus is to be shared with other devices, the interface logic must co-exist with other PCI targets, and this will require additional circuitry. If the PCI bus is not shared with any other device, the interface logic can assume any PCI transaction is meant for it, and the logic becomes quite simple.

Below is a block diagram showing the MPC5200 PCI signals connected to either the necessary interface logic or directly to the sensor.

Bold lines in Figure 2 represent a tri-state condition. The bus requires external pull-up resistors, so that the interface logic sees a logical "1" at its inputs.

The sensor indicates over its frame valid period that a frame on the sensor is ready to be transmitted. This signal will be connected to the MPC5200 over an IRQ line. The frame transfer needs to be driven from the MPC5200 PCI controller.

- MPC5200 PCI drives Frame_b low to start the transaction. The AD lines are driven by MPC5200 with Address information. The Interface Logic can ignore this phase.

- MPC5200 PCI drives Irdy_b low to start the data phase. The AD lines remain driven by MPC5200 until Target (Interface Logic) asserts Devsel_b to "claim" the transaction.
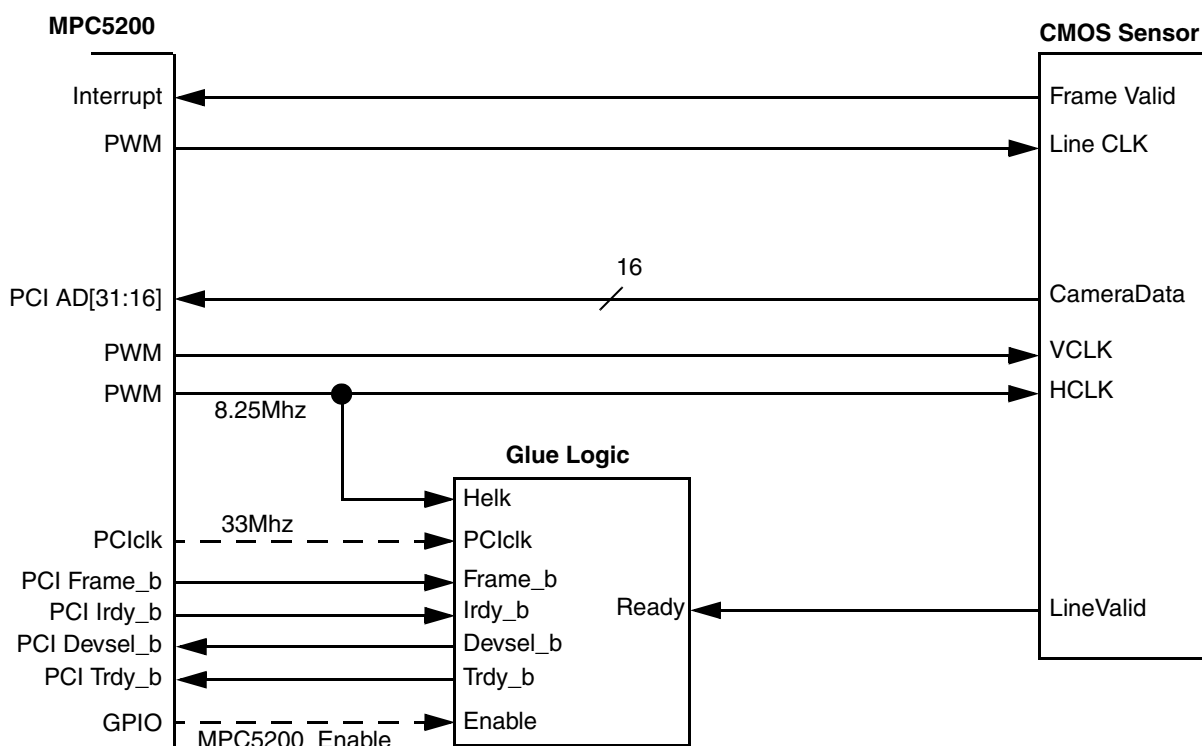
Figure 2. Connecting diagram MPC5200–Interface–CMOS Sensor

NOTE

The PCIclk connection to the Interface Logic would not be necessary if HCLK was 2:1 PCIclk. (The logic would become entirely combinatorial.) For a 4:1 PCIclk-HCLK ratio (Which is much more desirable), one flip-flop is needed to delay and shorten the assertion of the PCI signal Trdy_b.
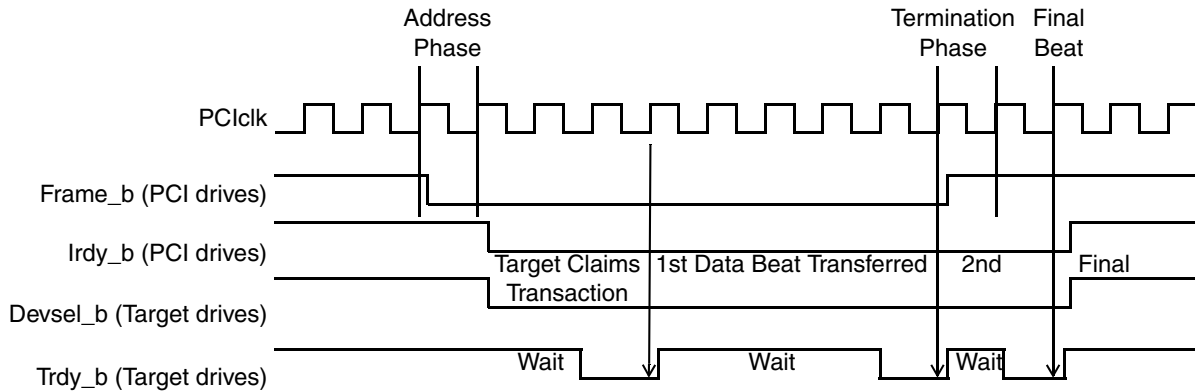
Figure 3. PCI Standard Interface

- MPC5200 PCI then tri-states the AD bus and remains in a Wait State as long as Target is keeping Trdy_b high.

- At any rising PCIclk edge where Trdy_b is detected as low, PCI captures the data and considers one data beat to be transferred.

- At the completion of next-to-last data beat, MPC5200 PCI negates Frame_b, which signals that the last data beat is being requested.

- When Target transfers this final data beat (signified by Trdy_b being low), MPC5200 PCI negates Irdy_b, and the transaction is completed.

- There are other signals associated with PCI transactions; however, they are for error cases in PCI transfers and are not required in this application.

When the 3.3 volt compatible CMOS camera sensor tri-states its data bus, the sensor's data lines are effectively connected directly to the PCI AD bus. Otherwise, data transceivers will be required in the design. The sensor should only drive data lines when its LineValid signal is asserted.
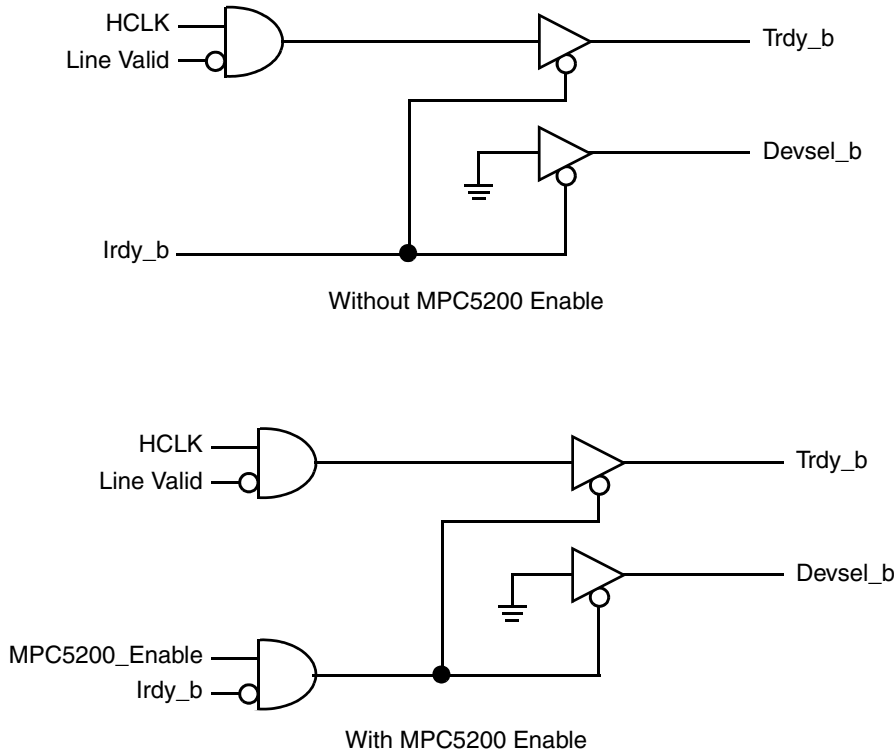
Figure 4. Logic for 2-1 case PCIclk at 27 MHz, HCLK at 13.5MHz (or similar frequency)

This example interface will only work when no other real PCI target device is connected to the PCI-interface. Otherwise, some type of an enable will be needed to inform the Interface Logic to respond to the upcoming PCI transaction.

- In the 2:1 case, the sensor data is valid when HCLK is low, and the next PCIclk rising edge captures the data as HCLK rises again to present the next data beat.

NOTE

PCI transaction must begin prior to the LineValid asserting. The PCI transaction is wait-stated by Trdy_b until LineValid goes high. Additional circuitry may be needed to shut off this circuit at the end of the PCI transaction since 5200Enable requires several cycles to be negated. During this period, a non-camera PCI transaction may wish to commence (to which this Interface Logic must NOT respond).
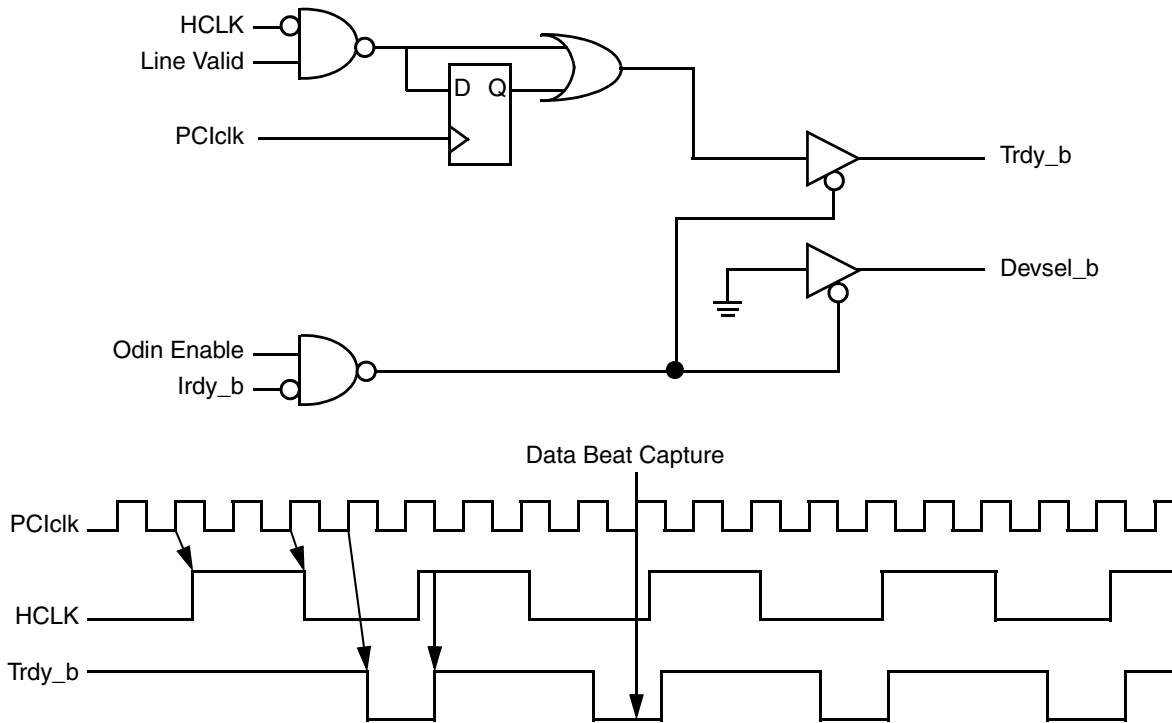
Figure 5. Logic for 4-1 case PCIclk at 33, HCLK at 8.25 (or similar)

- Since HCLK is derived from the MPC5200 PWM, HCLK, transitions occur after the PCIclk edge. (PCIclk is designed to arrive early on the bus.)
- When HCLK falls, the assertion of Trdy_b is delayed by one PCIclk.
- When HCLK rises, Trdy_b immediately goes high.
- This creates the PCI data beat capture at the PCIclk edge, which then creates the rising HCLK (where Pixel Data advances).

A BestComm task, which controls the reading of the sensor data, is flexible enough to be adapted to different sensor sizes.

In this example based on a Freescale (formerly Motorola) CMOS sensor, 640 * 480 pixels are utilized with 10 bits per pixel. After each line, the burst is terminated, and the BestComm task automatically starts the read of the next line until the picture is complete.

This method provides for a very high frame rate. Per line, there is an overhead of 15 clks.

> 640 clocks for the pixel data + 15 clocks overhead = 655 clock
> 655 clocks * 480 lines = 314.4k clocks for a frame
> 33 MHz PCI clock -> 9,52 ms per frame, which gives 105 frames/s

The Frame rate depends on the clock and the resolution of the sensor.

The burst length and the amount of the lines which are read for a complete picture are BestComm parameters which can also be adjusted for each sensor type.

The frame throughput that can be achieved with the interface is much higher than the frame rate of the application. The limiting factor is the calculation power needed for the algorithms. This is very application dependent. Freescale (formerly Motorola) offers an MPC603e core at 400 MHz with 760 MIPS with an integrated FPU.

The burst length and the amount of the line which are read for a complete picture are BestComm parameters, which can be adjusted for each sensor type.

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