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Application Note

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MPC8560 PowerQUICC™ III Compact Flash Interface Design

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This document describes the implementation of a Compact Flash memory controller and interface on the local bus of a PowerQUICC™ MPC8560 processor. This implementation uses a user-programmable machine (UPM) to generate the required control signals and timing for the compact flash memory device. The hardware connection between the local bus and the Compact Flash device is described, and required register settings and UPM RAM array contents are provided.

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1 Compact Flash Overview

Compact Flash is a PCMCIA-compatible small, removable 16-bit storage or I/O device initially introduced in 1994 by SanDisk Corporation. The Compact Flash Association (CFA) (http://www.compactflash.org), which was started in 1995, defines the standards for Compact Flash devices. Because Compact Flash devices have only 50 pins and 11-bit address space, they are smaller than PCMCIA devices; however Compact Flash devices still conform to the PCMCIA PC Card ATA (AT attached) specifications. Additionally, Compact Flash storage devices can be designed to operate in conformance with the ATA-4 (AT attached) specification for IDE drives. Compact Flash storage devices are essentially solid-state ATA disk drives

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that are controlled through ATA task file registers defined by the ANSI T13 committee (http://www.t13.org).

Compact Flash storage cards are typically designed with Flash technology, a non-volatile storage solution that does not require an active power source to retain data. Compact Flash I/O cards are available as modems, Ethernet, serial, BlueTooth wireless, IEEE® 802.11b™ WiFi LAN, and so on. Applications that use Compact Flash devices include digital cameras, digital audio and music devices, portable data collection devices, PDAs, home entertainment set-top services, laptop and desktop computers, networking equipment, and embedded systems.

1.1 CF Classes

The Compact Flash Association developed the CF+ specification to expand the CF concept beyond flash data storage and include I/O devices and magnetic disk data storage. CF classes are:

- Type I (3.3 mm thick) card and newer type II (5 mm thick) cards.
- Type II (5 mm thick) cards enable higher capacity CompactFlash cards, magnetic disk cards, and many additional I/O cards.

Note that CF+ and Compact Flash cards can be used with passive adapters in a PC-card type II or type III socket. The CompactFlash storage cards on-card intelligent controller manages interface protocols, data storage and retrieval, error-correcting code (ECC), defect handling and diagnostics, power management, and clock control. When the host has configured the Compact Flash storage card, it appears to the host as a standard ATA (IDE) disk drive (see Figure 1).

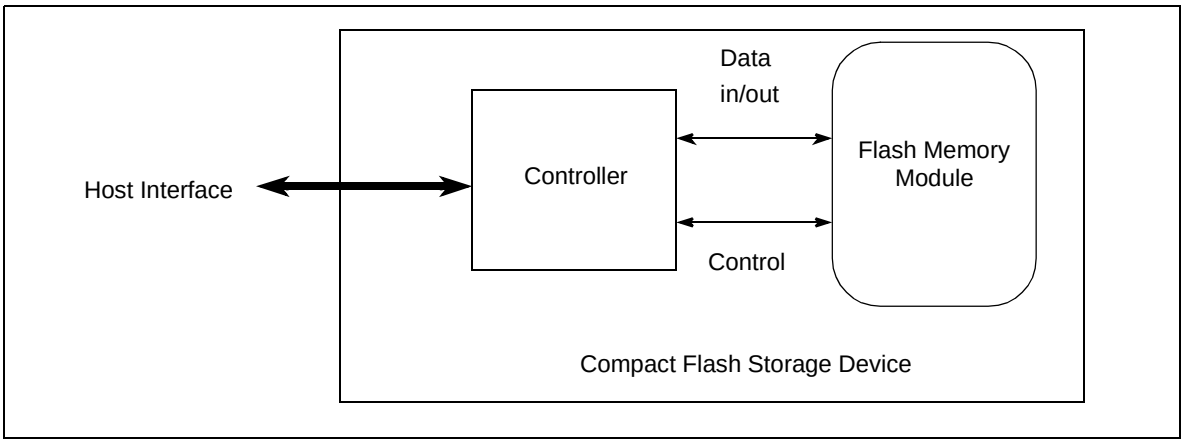


Figure 1. Configured Compact Flash Storage Card

1.2 Electrical Interface

According to the CF+ and CompactFlash Specification, Revision 1.4, the host is connected to the Compact Flash Storage Card or CF+ Card using a standard 50-pin connector. The connector in the host consists of two rows of 25 male contacts, each on 50 mil (1.27 mm) centers. Table 1 lists the signals of the CF interface for the various modes of operation.

Table 1. CF Interface Signals

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode [4]			
Pin No.	Signal Name	Pin Type	In, Out Type	Pin No.	Signal Name	Pin Type	In, Out Type	Pin No.	Signal Name	Pin Type	In, Out Type
1	GND		Ground	1	GND		Ground	1	GND		Ground
2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3	2	D03	I/O	I1Z,OZ3
3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3	3	D04	I/O	I1Z,OZ3
4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3	4	D05	I/O	I1Z,OZ3
5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3	5	D06	I/O	I1Z,OZ3
6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3	6	D07	I/O	I1Z,OZ3
7	-CE1	I	I3U	7	-CE1	I	I3U	7	-CS0	I	I3Z
8	A10	I	I1Z	8	A10	I	I1Z	8	A10	I	I1Z
9	-OE	I	I3U	9	-OE	I	I3U	9	-ATA SEL	I	I3U
10	A09	I	I1Z	10	A09	I	I1Z	10	A09	I	I1Z
11	A08	I	I1Z	11	A08	I	I1Z	11	A08	I	I1Z
12	A07	I	I1Z	12	A07	I	I1Z	12	A07	I	I1Z
13	VCC		Power	13	VCC		Power	13	VCC		Power
14	A06	I	I1Z	14	A06	I	I1Z	14	A06	I	I1Z
15	A05	I	I1Z	15	A05	I	I1Z	15	A05	I	I1Z
16	A04	I	I1Z	16	A04	I	I1Z	16	A04	I	I1Z
17	A03	I	I1Z	17	A03	I	I1Z	17	A03	I	I1Z
18	A02	I	I1Z	18	A02	I	I1Z	18	A02	I	I1Z
19	A01	I	I1Z	19	A01	I	I1Z	19	A01	I	I1Z
20	A00	I	I1Z	20	A00	I	I1Z	20	A00	I	I1Z
21	D00	I/O	I1Z,OZ3	21	D00	I/O	I1Z,OZ3	21	D00	I/O	I1Z,OZ3
22	D01	I/O	I1Z,OZ3	22	D01	I/O	I1Z,OZ3	22	D01	I/O	I1Z,OZ3
23	D02	I/O	I1Z,OZ3	23	D02	I/O	I1Z,OZ3	23	D02	I/O	I1Z,OZ3
24	WP	O	OT3	24	-IOIS16	O	OT3	24	-IOIS16	O	ON3
25	-CD2	O	Ground	25	-CD2	O	Ground	25	-CD2	O	Ground
26	-CD1	O	Ground	26	-CD2	O	Ground	26	-CD2	O	Ground
27	D11	I/O	I1Z,OZ3	27	D11	I/O	I1Z,OZ3	27	D11	I/O	I1Z,OZ3
28	D12	I/O	I1Z,OZ3	28	D12	I/O	I1Z,OZ3	28	D12	I/O	I1Z,OZ3
29	D13	I/O	I1Z,OZ3	29	D13	I/O	I1Z,OZ3	29	D13	I/O	I1Z,OZ3
30	D14	I/O	I1Z,OZ3	30	D14	I/O	I1Z,OZ3	30	D14	I/O	I1Z,OZ3
31	D15	I/O	I1Z,OZ3	31	D15	I/O	I1Z,OZ3	31	D15	I/O	I1Z,OZ3

Table 1. CF Interface Signals (continued)

PC Card Memory Mode				PC Card I/O Mode				True IDE Mode [4]			
Pin No.	Signal Name	Pin Type	In, Out Type	Pin No.	Signal Name	Pin Type	In, Out Type	Pin No.	Signal Name	Pin Type	In, Out Type
32	-CE2	I	I3U	32	-CE2	I	I3U	32	-CS1	I	I1Z
33	-VS1	O	Ground	33	-VS1	O	Ground	33	-VS1	O	Ground
34	-IORD	I	I3U	34	-IORD	I	I3U	34	-IORD	I	I3Z
35	-IOWR	I	I3U	35	-IOWR	I	I3U	35	-IOWR	I	I3Z
36	-WE	I	I3U	36	-WE	I	I3U	36	-WE	I	I3U
37	RDY/BSY	O	OT1	37	IREQ	O	OT1	37	INTRQ	O	OZ1
38	VCC		Power	38	VCC		Power	38	VCC		Power
39	-CSEL	I	I2Z	39	-CSEL	I	I2Z	39	-CSEL	I	I2U
40	-VS2	O	OPEN	40	-VS2	O	OPEN	40	-VS2	O	OPEN
41	RESET	I	I2Z	41	RESET	I	I2Z	41	-RESET	I	I2Z
42	-WAIT	O	OT1	42	-WAIT	O	OT1	42	IORDY	O	ON1
43	-INPACK	O	OT1	43	-INPACK	O	OT1	43	-INPACK	O	OZ1
44	-REG	I	I3U	44	-REG		I3U	44	-REG	I	I3U
45	BVD2	I/O	I1Z,OZ3	45	-SPKR	I/O	I1Z,OZ3	45	-DASP	I/O	I1U,ON1
46	BVD1	I/O	I1Z,OZ3	46	-STSCHG	I/O	I1Z,OZ3	46	-PDIAG	I/O	I1U,ON1
47	D08	I/O	I1Z,OZ3	47	D08	I/O	I1Z,OZ3	47	D08	I/O	I1Z,OZ3
48	D09	I/O	I1Z,OZ3	48	D09	I/O	I1Z,OZ3	48	D09	I/O	I1Z,OZ3
49	D10	I/O	I1Z,OZ3	49	D10	I/O	I1Z,OZ3	49	D10	I/O	I1Z,OZ3
50	GND		Ground	50	GND		Ground	50	GND		Ground

1.3 Operating Modes

Compact Flash storage devices operate in three basic modes:

- PCMCIA-compatible PC card ATA using memory mode
- PCMCIA-compatible PC card ATA using I/O Mode
- IDE disk drive-compatible true IDE mode that is electrically compatible with IDE disk drive

Although Compact Flash devices must support operation in all three modes, they operate only in a single mode at any given time. The operating mode is configured using either the standard PCMCIA configuration registers for PCMCIA-compatible modes or grounding pin 9 for true IDE mode.

1.4 Compact Flash ATA Register Mapping Configuration

The Compact Flash ATA task file registers can be mapped in one of four possible ways:

- Memory-mapped using addresses 0h-Fh and 400h-7FFh; corresponds to general memory space
- I/O-mapped 16 contiguous registers using addresses XX0h-XXFh; corresponds to a system-decoded 16 byte I/O block
- Primary I/O-mapped using addresses 1F0h-1F7h and 3F6h-3F7h
- Secondary I/O-mapped using addresses 170h-177h and 376h-377h; primary and secondary I/O mappings correspond to the standard PC-AT disk I/O address spaces

1.4.1 PC Card ATA using Memory Mode

Compact Flash storage devices operating in memory mode have two distinct memory spaces:

- Attribute (configuration) memory, which includes both the card configuration registers and the card information structure (CIS) that contains information about the card and is typically used by the system and Compact Flash card controller to configure the device properly. Attribute memory accesses are limited to 8 bits only at even addresses. Attribute memory space is accessed when the -REG signal is low.
- Common memory, which includes all the other storage in the card. The ATA task file registers are mapped into common memory space. Common memory accesses can be either 8 or 16 bits wide. Common memory space is accessed when the -REG signal is high.

1.4.2 PC Card ATA using I/O Mode

Compact Flash storage devices operating in I/O mode have three distinct I/O address mappings:

- Contiguous I/O (XX0h-XXFh)
- Primary I/O - IDE (1F0h-1F7h and 3F6h-3F7h)
- Secondary I/O - IDE (170h-177h and 376h-377h)

Although the Compact Flash storage device can operate in this mode, it still contains attribute memory that allows it to be configured properly. Information in the card configuration option register, typically located at address 0x200h in the attribute memory space, determines whether the task file registers are mapped to common memory space or one of the three I/O ranges.

1.4.3 True IDE Mode

Compact Flash storage devices can operate in true integrated drive electronics (IDE) mode if the -ATA_SEL input signal (pin 9) is grounded when the Compact Flash card is reset. In this mode, the attribute memory space, including the card configuration registers, is not accessible. The task file registers are mapped into I/O address space.

2 Example System Design Requirements

Although Compact Flash storage devices are very flexible in supporting different operating modes and bus widths, the mode chosen for a particular system design depends upon many factors including performance requirements, system interface requirements, complexity of Compact Flash controller, and existing software base requirements. Many times, design trade-offs must be made to achieve the best possible design, given the system requirements. Consider the following examples:

- If a Compact Flash storage device is used as a direct replacement for an IDE hard drive in an existing system, operating the Compact Flash in true IDE mode probably presents the least risk in terms of impact to existing software.
- If the system requires the highest data transfer throughput, a 16-bit data bus interface is a better choice than an 8-bit data bus interface.
- If the system requires hot insertion and removal capability, implementing a PCMCIA controller and operating the Compact Flash storage device in a PCMCIA-compliant mode is necessary.

For the design example outlined in the rest of this paper, the system requirements are as follows:

- A Compact Flash storage device interfaces to a PowerQUICC™ III device through the local bus operating at 66 MHz. The PowerQUICC III system clock frequency is 266 MHz.
- Support for hot insertion and removal of the Compact Flash storage device is not required.
- The Compact Flash storage device can operate in PC Card ATA using memory mode with an 8-bit data interface.
- The Compact Flash card in the design example is an industrial grade (extended temperature) SanDisk (http://www.sandisk.com) Compact Flash card, part number SDCFBI-64-101-80.

3 Compact Flash Controller Design Implementation

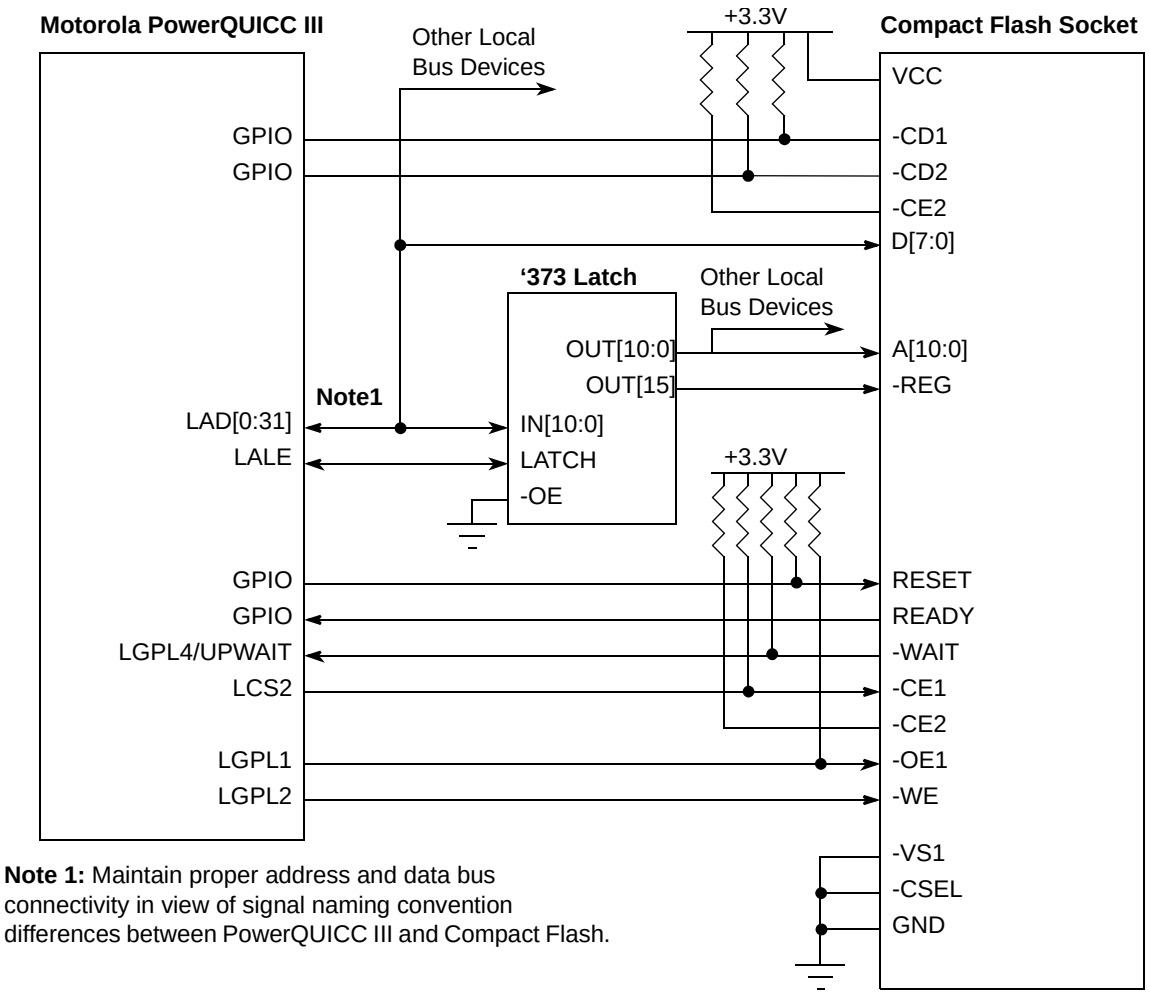
The following general information notes apply to the design example:

- The block diagram for the design is shown in Figure 2.
- Although the MPC8560 core voltage is 2.5 V, its I/O ring operates at 3.3 V, which is compatible with Compact Flash signal voltage levels when it operates at 3.3 V. Because this design is required to support only 3.3 V mode for the Compact Flash, -VS1 is pulled low.
- Because support for hot insertion and removal of the Compact Flash storage device is not required, isolation buffers are not required on the address, data, or control signals.
- Although the SanDisk Compact Flash card does not generate a -WAIT signal, the signal line is connected to the PowerQUICC III to support other Compact Flash cards that drive this signal.
- The Compact Flash card is assigned to $\overline{\text{LCS2}}$ for this example.
- Because only an 8-bit data interface is required, pulling -CE2 high is permissible.
- The divider to generate the local bus clock from the system clock is 4 (266 MHz/66.6 MHz); the time between consecutive local bus clock rising edges is 15 ns.
- PowerQUICC III GPIO (general-purpose I/O) pins are used for some control and status signals:
  - The Compact Flash card RESET line is tied to a GPIO pin; so software must reset the card before initializing it.

— The Compact Flash card detect lines, -CD1 and -CD2, are connected to GPIO pins. Software can periodically poll the status of these pins to determine whether a Compact Flash card is inserted. Alternatively, -CD1 and -CD2 can be connected to two external interrupt input lines and the interrupt controller and interrupt service routines can be configured to detect a change of state on these signals.

— The Compact Flash card READY signal is connected to a GPIO pin, and the status of this pin can be polled during a Flash Card reset to determine when the Compact Flash card has completed its reset sequence.

- Because the local bus implements a multiplexed address and data bus, an external latch is required to hold the address during an access to the Compact Flash device. The local bus signal, LALE, controls when the address is latched.
- Because this design has no requirements for implementing a separate high-speed data path on the local bus, a separate data bus transceiver is not required. Depending on specific system requirements, a data bus transceiver can be added to the design.
- A user-programmable machine (UPM) on the PowerQUICC III assigned to a local bus address range generates the appropriate control signals for the Compact Flash storage device. For this design, UPMA was selected.



Note 1: Maintain proper address and data bus connectivity in view of signal naming convention differences between PowerQUICC III and Compact Flash.

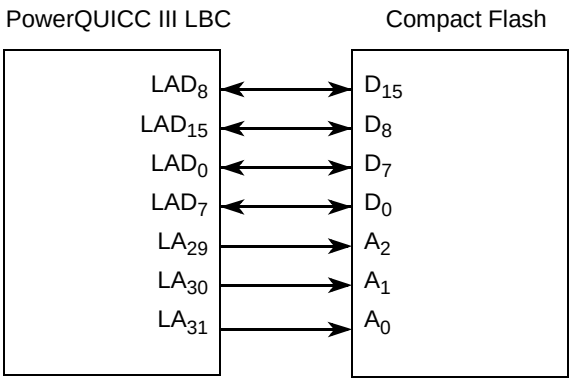
Figure 2. Compact Flash Connection to PowerQUICC III

3.1 Endianness and Signal Naming Conventions

To interface a Compact Flash card to the PowerQUICC III local bus, it is necessary to account for the differences in endianness and signal naming conventions between the two devices. Compact Flash cards are little-endian, with the least significant byte of a multibyte value stored in the lowest byte address. In contrast, the PowerQUICC III is a big-endian device, with the most significant byte of a multi-byte value stored in the lowest byte address. When interfacing to a 16-bit Compact Flash card, care must be taken to ensure that the byte lanes are connected correctly between the devices.

For a Compact Flash card operating in True IDE 16-bit mode, maintaining proper endianness is slightly more complicated because the Compact Flash card supports both 8-bit (task file register) and 16-bit data accesses. For 16-bit data accesses, the Compact Flash card data bus is defined such that D00 is the LSB of the Even Byte of the 16-bit word, and D08 is the LSB of the odd byte of the 16-bit word. For 8-bit task file register accesses, the Compact Flash card data bus is defined such that D00 is the LSB of the register data, while bits D08 through D15 are unused.

Figure 3 shows one option for connecting a 16-bit Compact Flash card to the PowerQUICC III. This option employs an address invariance scheme in which the byte addresses of each byte are maintained, but the interpreted values of multi-byte words are different between the Compact Flash card and the PowerQUICC III. Figure 4 shows how the address invariance scheme results in different interpretations of multi-byte words that are stored in memory. To avoid misinterpreting data, it may be necessary to swap bytes in software in order to maintain the proper data endianness.



PowerQUICC III and Compact Flash Interconnection

Notes:
- LBC port assigned to Task File registers defined as 8-bit interface
- LBC port assigned to data defined as 16-bit interface
- Task File registers 0x0 through 0x7 addressed through consecutive LBC byte addresses (0x0 through 0x7)
- Task File and data D[7:0] of Compact Flash transferred on LAD[0:7] of LBC
- Data D[15:8] of Compact Flash transferred on LAD[8:15] of LBC
- 16-bit data must be byte swapped to maintain proper endianness

Figure 3. PowerQUICC III/Compact Flash Connectivity Assuming “Address Invariance”

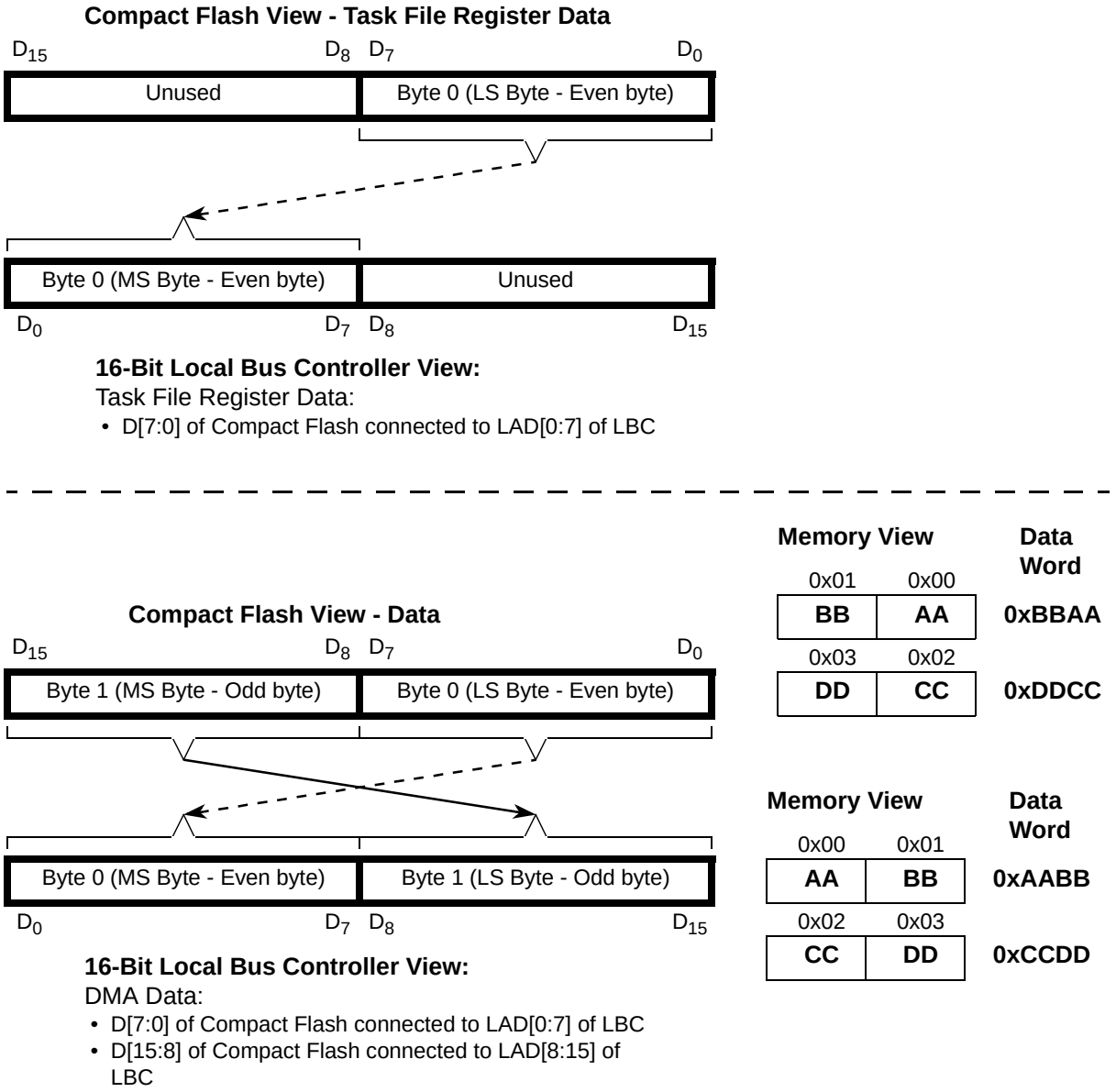
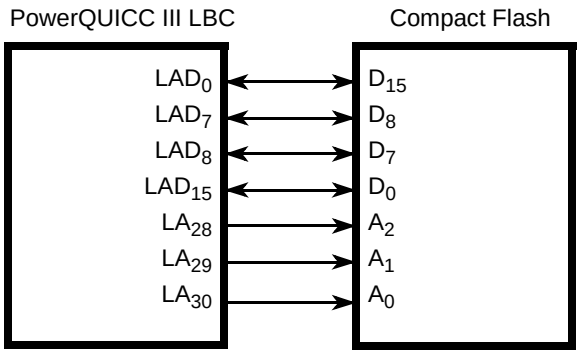


Figure 4. PowerQUICC III/Compact Flash Data Transfers Assuming "Address Invariance"

Figure 5 shows another option for connecting the Compact Flash card to the PowerQUICC III. This option employs a data invariance scheme in which the byte addresses of multi-byte words are altered to maintain the interpretation of the values of the multi-byte words on each device. Figure 6 shows how the data invariance scheme results in identical interpretations of multi-byte words that are stored in memory. However, with this scheme, it is necessary to define the LBC port size for the 8-bit task file register accesses as 16 bits, with the data appearing on eLBC LAD[0:7] discarded for these accesses.

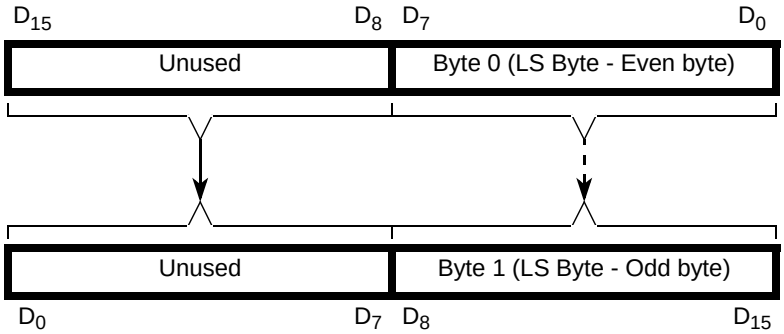


PowerQUICC III - Compact Flash Interconnection

Notes:
- LBC port assigned to Task File registers defined as 16-bit interface; data in unused byte should be masked off
- LBC port assigned to data defined as 16-bit interface
- Task File registers 0x0 through 0x7 addressed through consecutive eLBC even byte addresses (0x0, 0x2, 0x4, 0x6, 0x8, 0xA, 0xC, 0xE); LBC LA_{31} is unused
- Task File and data D[7:0] of Compact Flash transferred on LAD[8:15] of LBC
- Data D[15:8] of Compact Flash transferred on LAD[0:7] of LBC
- No byte swapping of data is necessary to maintain proper endianness

Figure 5. PowerQUICC III/Compact Flash Connectivity Assuming "Data Invariance"

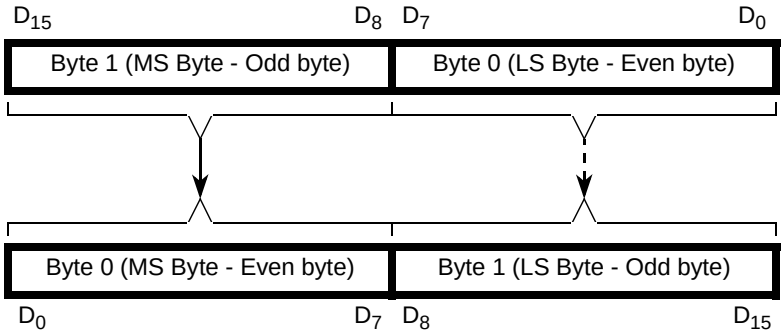
Compact Flash View - Task File Register Data



16-Bit Local Bus Controller View:

Task File Register Data:
- D[7:0] of Compact Flash connected to LAD[8:15] of LBC

Compact Flash View - Data



Memory View / **Data Word**

0x01	0x00	
BB	AA	0xBBAA
0x03	0x02	
DD	CC	0xDDCC

Memory View / **Data Word**

0x00	0x01	
BB	AA	0xBBAA
0x02	0x03	
DD	CC	0xDDCC

16-Bit Local Bus Controller View:

Data:
- D[7:0] of Compact Flash connected to D[8:15] of LBC
- D[15:8] of Compact Flash connected to D[0:7] of LBC

Figure 6. PowerQUICC III/Compact Flash Data Transfers Assuming Data Invariance

Note that for this example, the Compact Flash storage device operates in PC Card ATA using memory mode with an 8-bit data interface. To connect the Compact Flash storage device to the PowerQUICC III local bus, we implement the mapping shown in Table 2:

Table 2. PowerQUICC III to Compact Flash Bit Mapping

PowerQUICC III LAD Bit Number	Compact Flash Address Bit Number (through '373 Latch)	Compact Flash Data Bit Number	PowerQUICC III LAD Bit Number	Compact Flash Address Bit Number (through '373 Latch)	Compact Flash Data Bit Number
0	N/C	7	16	-REG	N/C
1	N/C	6	17	N/C	N/C
2	N/C	5	18	N/C	N/C
3	N/C	4	19	N/C	N/C
4	N/C	3	20	N/C	N/C
5	N/C	2	21	10	N/C
6	N/C	1	22	9	N/C
7	N/C	0	23	8	N/C
8	N/C	N/C	24	7	N/C
9	N/C	N/C	25	6	N/C
10	N/C	N/C	26	5	N/C
11	N/C	N/C	27	4	N/C
12	N/C	N/C	28	3	N/C
13	N/C	N/C	29	2	N/C
14	N/C	N/C	30	1	N/C
15	N/C	N/C	31	0	N/C

3.2 Hardware Connections

Table 3 shows pins that are used on the Compact Flash storage device to connect to the PowerQUICC III local bus.

Table 3. Compact Flash Card / PowerQUICC III Connections

Compact Flash Pin	Direction (Referenced to Compact Flash card)	Description	Connection to PowerQUICC III
RESET	Input	Active high card reset signal	GPIO
-CE1	Input	Chip select	Connected to $\overline{\text{LCS2}}$
-CE2	Input	Chip select; Tied high since unused in 8-bit data interface mode	N/C
-WE	Input	Write Enable	LGPL2
-OE	Input	Output Enable	LGPL1

Table 3. Compact Flash Card / PowerQUICC III Connections (continued)

Compact Flash Pin	Direction (Referenced to Compact Flash card)	Description	Connection to PowerQUICC III
A[10:0]	Input	Latched address Lines (MSB:LSB); connected to A[10:0] outputs of 373 Latch	Through 373 latch
D[7:0]	Input/Output	Data lines (MSB:LSB)	LAD[0:7]
-REG	Input	Attribute/common memory select; connected to the output of 373 Latch corresponding to the latched version of LAD[16]	Through 373 latch
-WAIT	Output	Wait output from Compact Flash card; not generated by SanDisk card	LGPL4
-CSEL	Input	Not used	GROUND
-CD1	Output	Card Detect, Low if card inserted	GPIO
-CD2	Output	Card Detect, Low if card inserted	GPIO
READY	Output	High value indicates card completed RESET operation	GPIO
BVD1	N/A	Not used	N/C
BVD2	N/A	Not used	N/C
WP	N/A	Not used	N/C
-INPACK	N/A	Not used	N/C
-IORD	N/A	Not used	N/C
-IOWR	N/A	Not used	N/C
-VS1	GROUND	3.3V Interface select	N/C
VCC	+3.3V	Power	+3.3V
GND	GROUND	Ground	GROUND

3.3 Compact Flash Memory Map

Compact Flash storage devices operating in memory mode have two distinct memory spaces, common memory and attribute memory. Table 4 shows the address and control signal truth table for accesses to these areas. Note that accesses to common memory and attribute memory are distinguished by the value of the -REG signal. When -REG is low, attribute memory is accessed; otherwise, common memory is accessed. The -REG signal is typically tied to a high-order address bit. In the case of this design, the latched version of LAD[16] is used.

Table 4. Compact Flash Card Configuration Registers and Memory Space Decoding

Selected Register	-CE2	-CE1	-REG	-OE	-WE	A[10:0]
Standby	1	1	X	X	X	0bXXX_XXXX_XXXX
Configuration Registers Read	X	0	0	0	1	0b01X_XXXX_XXX0
Common Memory Read (8 Bit D7-D0)	1	0	1	0	1	0bXXX_XXXX_XXXX

Table 4. Compact Flash Card Configuration Registers and Memory Space Decoding (continued)

Selected Register	-CE2	-CE1	-REG	-OE	-WE	A[10:0]
Common Memory Read (8 Bit D15-D8)	0	1	1	0	1	0bXXX_XXXX_XXXX
Common Memory Read (16 Bit D15-D0)	0	0	1	0	1	0bXXX_XXXX_XXX0
Configuration Registers Write	X	0	0	1	0	0b01X_XXXX_XXX0
Common Memory Write (8 Bit D7-D0)	1	0	1	1	0	0bXXX_XXXX_XXXX
Common Memory Write (8 Bit D15-D8)	0	1	1	1	0	0bXXX_XXXX_XXXX
Common Memory Write (16 Bit D15-D0)	0	0	1	1	0	0bXXX_XXXX_XXX0
Card Information Structure Read	X	0	0	0	1	0b00X_XXXX_XXX0
Invalid Access (CIS Write)	1	0	0	1	0	0b00X_XXXX_XXX0
Invalid Access (Odd Attribute Read)	1	0	0	0	1	0bXXX_XXXX_XXX1
Invalid Access (Odd Attribute Write)	1	0	0	1	0	0bXXX_XXXX_XXX1
Invalid Access (Odd Attribute Read)	0	1	0	0	1	0bXXX_XXXX_XXXX
Invalid Access (Odd Attribute Write)	0	1	0	1	0	0bXXX_XXXX_XXXX

3.4 Compact Flash Memory Access Timing

Figure 7 shows the timing diagram for Compact Flash read accesses. Figure 8 shows the timing diagram for Compact Flash write accesses. The specific timing requirements for different types of read accesses and write accesses for the SanDisk Compact Flash card are shown in Table 5 and Table 6, respectively. Note that although the memory write timings for both attribute and common memory are identical in the SanDisk Compact Flash device, there are minor differences in the attribute and common memory accesses in the memory read timings. The most notable differences are in the read cycle time and several of the access time specifications, with the slowest timings associated with attribute memory accesses. To minimize the amount of interface logic, the memory read state machine uses the slower attribute memory timings. Note that Compact Flash storage devices support only individual (non-burst) accesses; therefore, the slight memory read timing differences are likely be masked by the time required for the UPM to not only acknowledge and terminate one access but also to decode and begin driving the control signals for a subsequent access. If further optimization is required, either the timings associated with the UPM control signals can be adjusted to match the specified parameters of the Compact Flash device or other design approaches can be used. See Section 4, “Design Alternatives” on page 21.

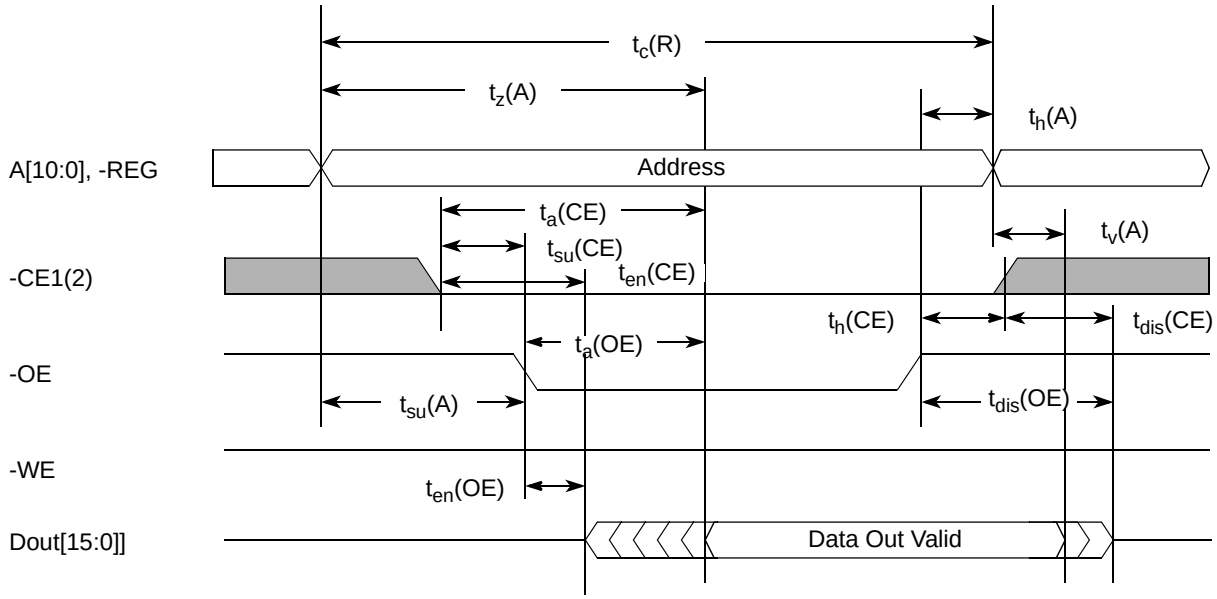


Figure 7. Compact Flash Common and Attribute Memory Read Timing Diagram

Table 5. Memory Read Timing Specifications

Parameter	Symbol	Compact Flash Specifications				SanDisk Compact Flash (250 ns version)				# of Local Bus Clocks @66MHz
		Attribute Memory (ns)		Common Memory (ns)		Attribute Memory (ns)		Common Memory (ns)		
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_c(R)	300	*	*	*	300	**	250	**	20
Address Access Time	t_a(A)	*	300	*	*	**	300	**	250	20
Card Enable Access Time	t_a(CE)	*	300	*	*	**	300	**	250	20
Output Enable Access Time	t_a(OE)	*	150	*	125	**	150	**	125	10
Output Disable Time from -OE	t_{dis}(OE)	*	100	*	100	**	100	**	100	7
Output Disable Time from -CE	t_{dis}(CE)	*	100	*	*	**	100	**	100	7
Output Enable Time from -OE	t_{en}(OE)	5	*	*	*	5	**	5	**	1
Output Enable Time from -CE	t_{en}(CE)	5	*	*	*	**	**	5	**	1
Data Valid from Address Change	t_v(A)	0	*	*	*	0	**	0	**	0
Address Setup Time	t_{su}(A)	30	*	30	*	30	**	30	**	2
Address Hold Time	t_h(A)	*	*	20	*	20	**	20	**	2
Card Enable Setup Time	t_{su}(CE)	*	*	0	*	0	**	0	**	0
Card Enable Hold Time	t_h(CE)	*	*	20	*	20	**	20	**	2

Note: * Indicates timing parameters not specified in Compact Flash specification
Note: ** Indicates timing parameters not specified in SanDisk part specification

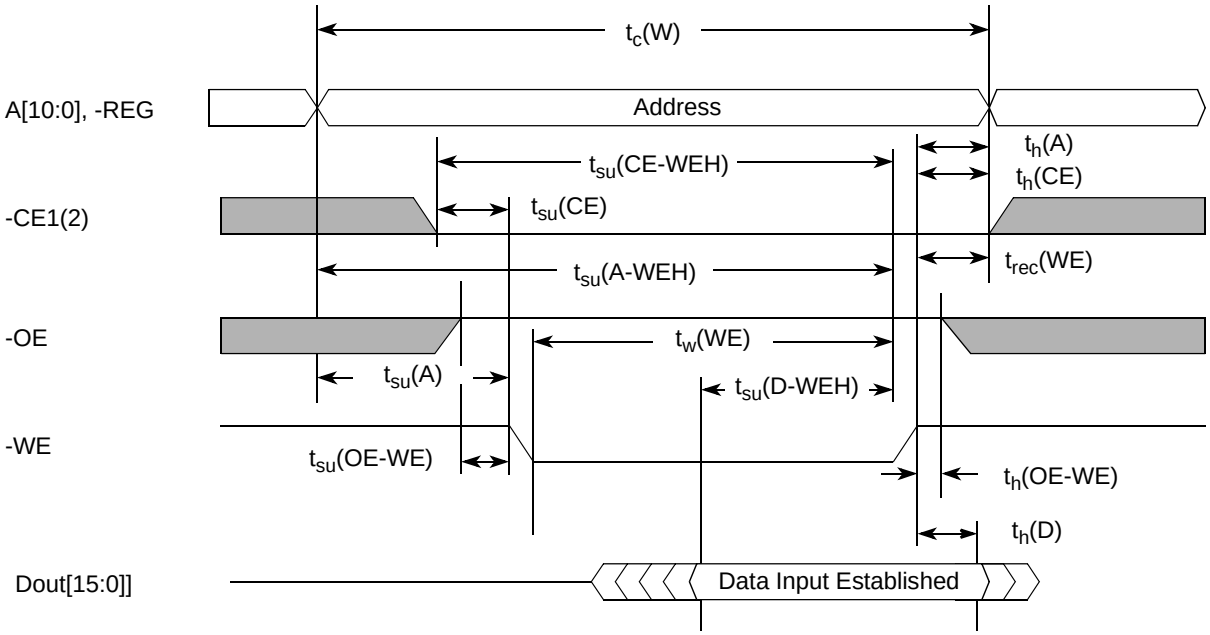


Figure 8. Compact Flash Common and Attribute Memory Write Timing Diagram

Table 6. Memory Write Timing Specifications

Parameter	Symbol	Compact Flash Specifications				SanDisk Compact Flash (250 ns version)				# of Local Bus Clocks @66MHz
		Attribute Memory (ns)		Common Memory (ns)		Attribute Memory (ns)		Common Memory (ns)		
		Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_c(W)	250	*	*	*	250	**	250	**	17
Write Pulse Width	t_w(WE)	150	*	150	*	150	**	150	**	10
Address Setup Time	t_{su}(A)	30	*	30	*	30	**	30	**	2
Address Setup Time for -WE	t_{su}(A-WEH)	*	*	*	*	180	**	180	**	12
Card Enable Setup TIme for -WE	t_{su}(CE-WEH)	*	*	*	*	180	**	180	**	12
Data Setup Time from -WE	t_{su}(D-WEH)	80	*	80	*	80	**	80	**	6
Data Hold Time	t_h(D)	30	*	30	*	30	**	30	**	2
Address Hold Time	t_h(A)	*	*	20	*	**	**	**	**	2
Write Recovery Time	t_{rec}(WE)	30	*	30	*	30	**	30	**	2
Output Disable Time from -WE	t_{dis}(WE)	*	*	*	*	**	100	**	100	7
Output Disable Time from -OE	t_{dis}(OE)	*	*	*	*	**	100	**	100	7
Output Enable Time from -WE	t_{en}(WE)	*	*	*	*	5	**	5	**	1
Output Enable Time from -OE	t_{en}(OE)	*	*	*	*	5	**	5	**	1
Output Enable Setup from -WE	t_{su}(OE-WE)	*	*	*	*	10	**	10	**	1

Table 6. Memory Write Timing Specifications (continued)

Parameter	Symbol	Compact Flash Specifications				SanDisk Compact Flash (250 ns version)				# of Local Bus Clocks @66MHz
		Attribute Memory (ns)		Common Memory (ns)		Attribute Memory (ns)		Common Memory (ns)		
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Enable Hold from -OE	t_h(OE-WE_	*	*	*	*	10	**	10	**	1
Card Enable Setup Time	t_{su}(CE)	*	*	0	*	0	**	0	**	0
Card Enable Hold Time	t_h(CE)	*	*	20	*	20	**	20	**	2

Note:
* indicates timing parameters not specified in Compact Flash specification.
** indicates timing parameters not specified in SanDisk part specification.

3.5 PowerQUICC III BRx and ORx Register Settings

Table 7 and Table 8 contain the recommended values for the BRx and ORx registers corresponding to $\overline{\text{LCS2}}$ (Chip Select 2) on the PowerQUICC III local bus:

Table 7. BR2 Register Programming

Bits	Name	Value	Description
0–16	BA	x	Base Address. Triggers Chip Select ($\overline{\text{LCS2}}$) if an address match occurs; use with OR2.
17–18	Reserved	0b00	Reserved
19–20	PS	0b01	Port size; set to 01 for 8-bit port
21–22	DECC	0b00	Data Error Checking; disabled
23	WP	0b0	Write protect; enable reads and writes
24–25	MSEL	0b100	Machine select; assign $\overline{\text{LCS2}}$ to UPMA
27	Reserved	0b0	Reserved
28–29	ATOM	0b00	Atomic Operations; no atomic operations supported on this Chip Select
30	Reserved	0b0	Reserved
31	V	0b1	Valid bit; set after programming BR2, OR2, and UPMA to indicate that the selection parameters for $\overline{\text{LCS2}}$ are valid

Table 8. OR2 Register Programming

Bits	Name	Value	Description
0–16	AM	all ‘1’s	UPM Address Mask. Corresponds to BR2 address mask; used to trigger a chip select if an address match occurs.
17–18	XAM	0b00	Extended address mask; no extended address mask needed

Table 8. OR2 Register Programming (continued)

Bits	Name	Value	Description
19	BCTLD	0b1	Data Buffer control disable; LBCTL is not enabled during an access to address range that hits in LCS2
20–22	Reserved	0b000	Reserved
23	BI	0b1	Burst inhibit; burst accesses disabled. A burst access is executed as a series of single accesses
24–28	Reserved	0b000	Reserved
29–30	TRLX,EHTR	0b00	Normal timing generated by memory controller
31	EAD	0b0	External address latch delay; LALE asserted for one bus clock cycle only

3.6 PowerQUICC III Local Bus Configuration Register (LBCR) Settings

Table 9 contains the recommended values for specific fields within the Local Bus Configuration Register (LBCR) register. Note that settings within the LBCR affect all local bus entities. Take care to program the LBCR correctly to ensure that all devices attached to the local bus can operate correctly.

Table 9. LBCR Register Programming

Bits	Name	Value	Description
0	LDIS	0b0	Enables the local bus
1–7	Reserved	0bxx_xxxx	Reserved
8–9	BCTLC	0bxx	Defines use of LBCTL; don't care for Compact Flash card because LBCTL is not used
10–13	Reserved	0bxxxx	Reserved
14	LPBSE	0b0	Enables parity byte select on LGPL4/UPWAIT; if Compact Flash card WAIT signal is connected, this bit must be disabled
15	EPAR	0bx	Even or odd parity; don't care for Compact Flash card interface
16–23	BMT	0bxxxx_xxxx	Bus monitor timeout where timeout is = BMT × 8; set to highest timeout value of local bus device – must be at least 5 (40 clock cycles). Can be adjusted if necessary for Compact Flash card.
24–31	Reserved	0bxxxx_xxxx	Reserved

3.7 PowerQUICC III Local Bus Clock Ratio Register (LCRR) Settings

Table 10 contains the recommended values for specific fields within the local bus clock ratio register (LCRR). Note that settings within the LCRR affect all local bus entities. Take care to program the LCRR correctly to ensure that all devices attached to the local bus can operate correctly.

Table 10. LCRR Register Programming

Bits	Name	Value	Description
0	DBYP	0b0	DLL bypass; enable the DLL
1	Reserved	0bx	Reserved
2–3	BUFCMDC	0bxx	Additional delay cycles for SDRAM control signals; don't care for Compact Flash card
4–5	Reserved	0bxx	Reserved
6–7	ECL	0bxx	Extended CAS latency for SDRAM; don't care for Compact Flash card
8–13	Reserved	0bxx_xxxx	Reserved
14–14	EADC	0b01	External address delay cycles; set to 1 for Compact Flash card access
16–27	Reserved	0bxxxx_xxxx_xxxx	Reserved
28–31	CLKDIV	0b0100	Local bus clock divider from system clock; set to 4 since system clock is 266 MHz and the local bus clock is 66 MHz. This configuration can be adjusted if necessary for the Compact Flash card.

3.8 PowerQUICC III UPMA Mode Register (MAMR) Settings

Table 11 lists the recommended values for specific fields within the UPMA mode register (MAMR).

Table 11. MAMR Register Programming

Bits	Name	Value	Description
0	Reserved	0b0	Reserved
1	RFEN	0b0	Refresh enable; refresh not required for Compact Flash.
2–3	OP	0b00	Command opcode; set to normal operation after the UPMA is set up and the corresponding RAM array is programmed.
4	UWPL	0b1	UPWAIT polarity; if connected to Compact Flash card, the polarity is active low.
5–7	AM	0b000	Address multiplex size; not used for Compact Flash card, so clear this bit.
8–9	DS	0b01	Disable timer period between successive accesses to same bank; set to 1 clock cycles between successive accesses - can be lengthened if needed
10–12	G0CL	0b000	General line 0 control; not used in this Compact Flash design, so clear this field.
13	GPL4	0b1	LGPL4 output line disable; set to force LGPL4 to be the UPWAIT input.
14–17	RLF	0b0101	Read loop field; can be changed to adjust timing if required.
18–21	WLF	0b0101	Write loop field; can be changed to adjust timing if required.

Table 11. MAMR Register Programming (continued)

Bits	Name	Value	Description
22–25	TLF	0b0001	Refresh loop field; not used in this Compact Flash design, so set this bit.
26–31	MAD	0bxx_xxxx	Machine address; used to program the UPMA RAM area. This field is not used in normal operation

3.9 UPMA RAM Array Programming

To program the UPMA RAM array to provide the required control signals to the Compact Flash card, the number of local bus clock cycles to meet each of the Compact Flash memory read and write requirements must be calculated. This information is presented in Table 5 and Table 6. Based on this information, the UPM programming tool for the PowerQUICC III device can be used to generate the RAM table entries that produce the required control signals and timing when the Compact Flash card is addressed. The UPM programming tool is available at the Freescale web site under listed on the back cover of this document.

Figure 9 shows the waveform generated by UPMA for a single-beat read from the Compact Flash card. The corresponding control bit patterns for this waveform are shown in Table 12. Figure 10 shows the waveform generated by UPMA for a single-beat write to the Compact Flash card. The corresponding control bit patterns for this waveform are shown in Table 13. Note that neither burst accesses nor refresh timing are supported for the Compact Flash port control state machine, defined as UPMA. Therefore, the values for the following UPMA RAM areas have not been defined: RBS, WBS, and RTS.

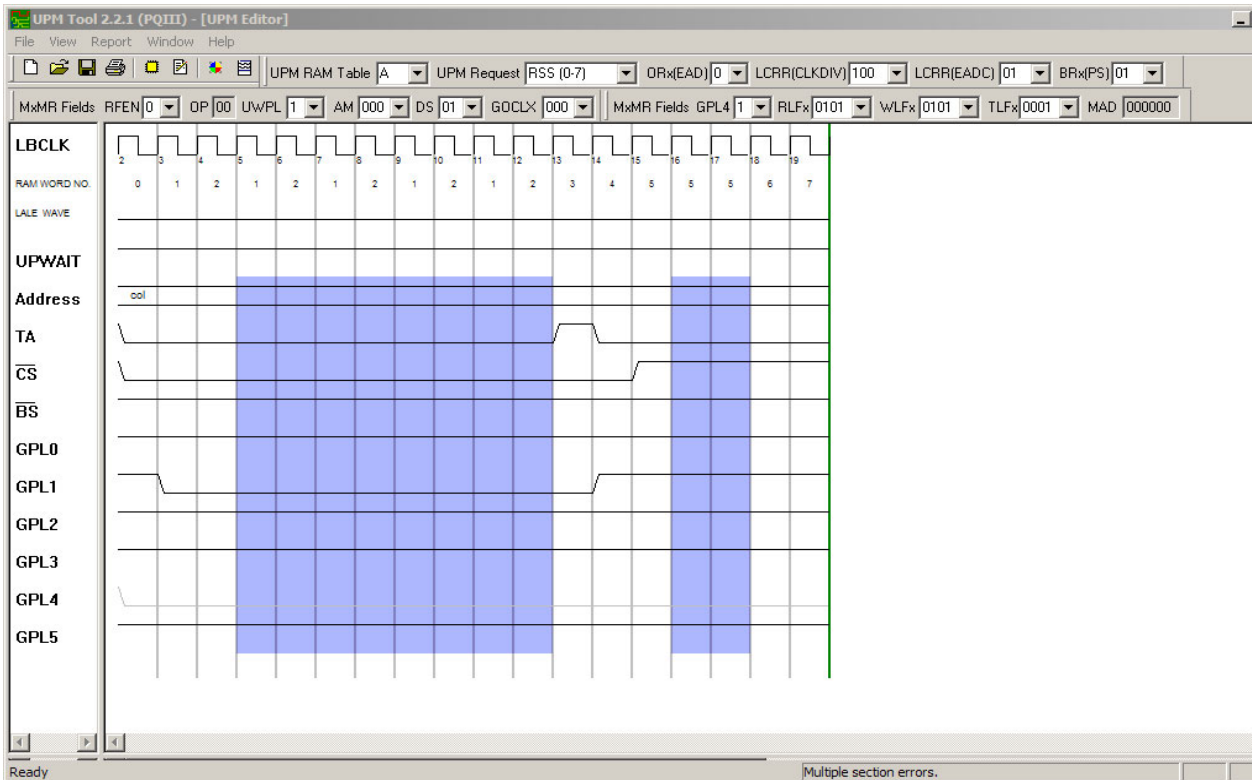


Figure 9. UPMA Single-Beat Read Waveform for Compact Flash Memory Accesses

Table 12. UPMA Read Single-Beat Request (RSS) RAM Word Definitions

Bit Name	UPM RAM Word Number								Bit Name	UPM RAM Word Number							
	0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7
CST1	0	0	0	0	0	1	1	1	G3T1	1	1	1	1	1	1	1	1
CST2	0	0	0	0	0	1	1	1	G3T3	1	1	1	1	1	1	1	1
CST3	0	0	0	0	0	1	1	1	DLT3	1	1	1	1	1	1	1	1
CST4	0	0	0	0	0	1	1	1	WAEN	1	1	1	1	1	1	1	1
BST1	1	1	1	1	1	1	1	1	G5T1	1	1	1	1	1	1	1	1
BST2	1	1	1	1	1	1	1	1	G5T3	1	1	1	1	1	1	1	1
BST3	1	1	1	1	1	1	1	1	REDO0	0	0	0	0	0	1	0	0
BST4	1	1	1	1	1	1	1	1	REDO1	0	0	0	0	0	0	0	0
G0L0	1	1	1	1	1	1	1	1	LOOP	0	1	1	0	0	0	0	0
G0L1	1	1	1	1	1	1	1	1	EXEN	0	0	0	0	0	0	0	0
G0H0	1	1	1	1	1	1	1	1	AMX0	0	0	0	0	0	0	0	0
G0H1	1	1	1	1	1	1	1	1	AMX1	0	0	0	0	0	0	0	0
G1T1	1	0	0	0	1	1	1	1	NA	0	0	0	0	0	0	0	0
G1T3	1	0	0	0	1	1	1	1	UTA	0	0	0	1	0	0	0	0
G2T1	1	1	1	1	1	1	1	1	TODT	0	0	0	0	0	0	0	0
G2T3	1	1	1	1	1	1	1	1	LAST	0	0	0	0	0	0	0	1

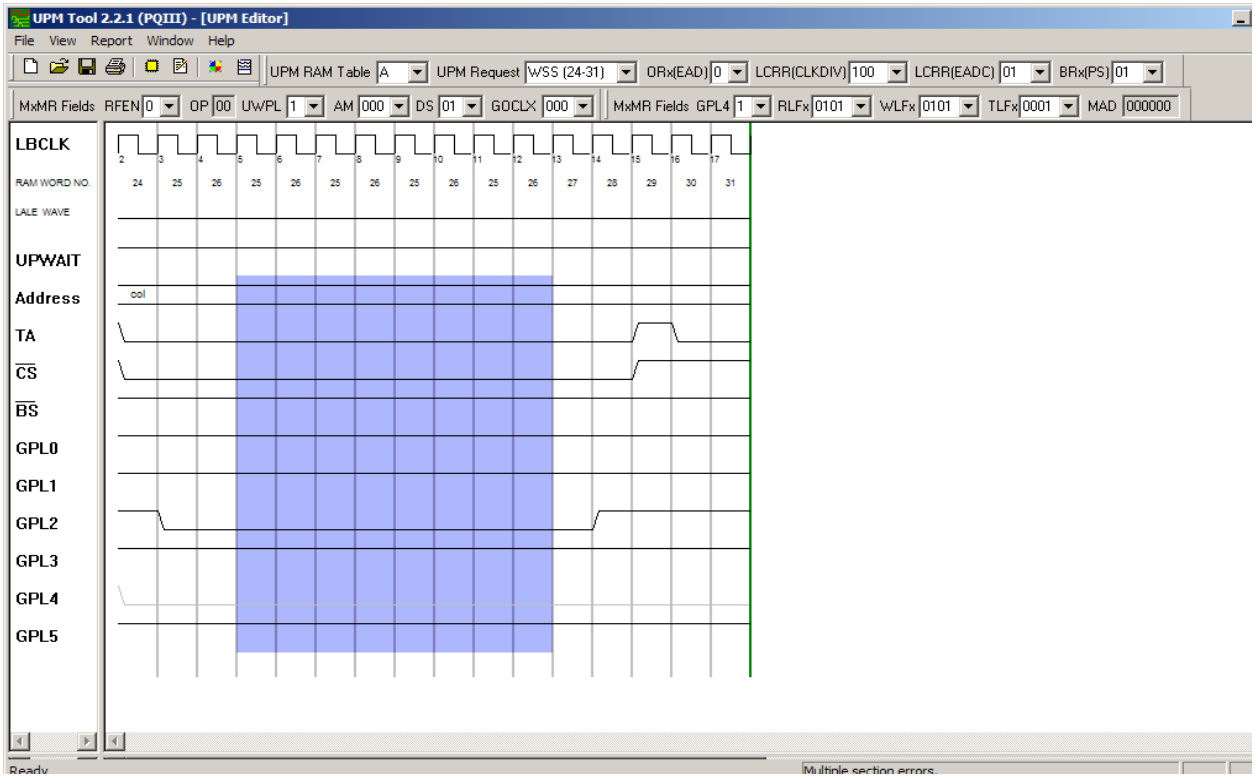


Figure 10. UPMA Single-Beat Write Waveform for Compact Flash Memory Accesses

Bit Name	UPM RAM Word Number								Bit Name	UPM RAM Word Number							
	24	25	26	27	28	29	30	31		24	25	26	27	28	29	30	31
CST1	0	0	0	0	0	1	1	1	G3T1	1	1	1	1	1	1	1	1
CST2	0	0	0	0	0	1	1	1	G3T3	1	1	1	1	1	1	1	1
CST3	0	0	0	0	0	1	1	1	DLT3	1	1	1	1	1	1	1	1
CST4	0	0	0	0	0	1	1	1	WAEN	1	1	1	1	1	1	1	1
BST1	1	1	1	1	1	1	1	1	G5T1	1	1	1	1	1	1	1	1
BST2	1	1	1	1	1	1	1	1	G5T3	1	1	1	1	1	1	1	1
BST3	1	1	1	1	1	1	1	1	REDO0	0	0	0	0	0	0	0	0
BST4	1	1	1	1	1	1	1	1	REDO1	0	0	0	0	0	0	0	0
G0L0	1	1	1	1	1	1	1	1	LOOP	0	1	1	0	0	0	0	0
G0L1	1	1	1	1	0	1	1	1	EXEN	0	0	0	0	0	0	0	0
G0H0	1	1	1	1	1	1	1	1	AMX0	0	0	0	0	0	0	0	0
G0H1	1	1	1	1	1	1	1	1	AMX1	0	0	0	0	0	0	0	0
G1T1	1	1	1	1	1	1	1	1	NA	0	0	0	0	0	0	0	0
G1T3	1	1	1	1	1	1	1	1	UTA	0	0	0	0	0	1	0	0
G2T1	1	0	0	0	1	1	1	1	TODT	0	0	0	0	0	0	0	0
G2T3	1	0	0	0	1	1	1	1	LAST	0	0	0	0	0	0	0	1

Table 13. UPMA Write Single-Beat Request (WSS) RAM Word Definitions

4 Design Alternatives

The previous design example using memory mode with an 8-bit data interface is just one of many ways a Compact Flash device can interface to a PowerQUICC III device on the local bus. Other possible design alternatives include the following:

- Memory mode with a 16-bit data bus interface. -CE1 and -CE2 are tied together and controlled by a single chip select from the local bus. Common memory data appears on D[15:0], and attribute memory data appears on D[7:0]. Address bit A[0] must always be low.
- “Optimized” memory mode with a 16-bit data bus interface. This alternative uses two UPMs to optimize timing for the two different memory access types. One UPM is programmed to meet the slower attribute memory timing specifications, and another UPM is programmed to meet the faster common memory timing specifications. -CE1 is tied to its own GPL line (GPL5 for example), and this GPL line is not driven (or shared) by any other local bus programmable machine or device except for the two UPMs dedicated to the Compact Flash device interface. -CE2 is tied to a chip-select line associated with the common memory UPM. -REG is still driven by a high-order address bit. When attribute memory is accessed, the attribute memory UPM is programmed to drive -CE1 low and control the -OE and -WE signals; the timing of these signals meets the slower attribute memory timing specifications. -CE2 is driven low by the chip select line when an address

in common memory is accessed and the program defined by the common memory UPM is selected. The common memory UPM drives -CE1 low and controls the -OE and -WE signals; the timing of these signals meets the faster common memory timing specifications. Common memory data appears on D[15:0], and attribute memory data appears on D[7:0]. Address bit A[0] must always be low.

- True IDE Mode with a 16-bit data bus interface. -CS0, which is used to access task file registers, and -CS1, which is used to access the alternate status register and the device control register, are assigned to different UPMs that are mapped into different local bus address ranges and therefore not active simultaneously. Task file data appears on D[7:0], data register data appears on D[15:0], and control and alternate status data appears on D[7:0]. The UPMs can be programmed to meet the specific timing requirements for mode 3 or mode 4, which have the fastest transfer rates and do not use the -IOCS16 signal. The IORDY is input into GPL4, and -IORD and -IOWR are driven by GPL lines, each under the control of both UPM machines.

5 References

- *CF+ and CompactFlash Specification,* Revision 1.4.
- *MPC8560 PowerQUICC™ III Reference Manual*.

6 Documentation Revision History

Table 14 provides a revision history for this application note.

Table 14. Document Revision History

Rev. No	Substantive Change(s)
0	Initial release
1	• Provided additional details on endianness. • Corrected RSS and WSS RAM word bits. • Added waveforms to reflect RAM word updates.

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