Freescale Semiconductor
Application Note

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Signal Integrity Considerations with MPC5500-based Systems

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1 Introduction

As external bus interfaces increase in operating frequency, signal integrity becomes a major concern for board designers. An increase in operating frequency usually requires shorter rise and fall times, and these faster edges produce more noise. Furthermore, higher operating frequencies have shorter periods, which means that there is less time available to wait for noisy signals to settle out. The MPC5500 family of devices are designed for a maximum external bus frequency of 75 MHz with edge rates in the range of 400 ps to 3 ns depending on the system configuration. Without proper attention to board design, signal integrity issues can be a major problem for MPC5500-based systems. However, if the guidelines presented in this application note are implemented, then signal integrity issues can be avoided in MPC5500-based systems.

This application note is intended to assist the board designer in ensuring signal integrity of the external bus in MPC5500-based systems.

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2 Problem Description

There are several types of signal integrity effects that occur in high-speed digital systems. This application note will focus on the three effects that are anticipated to be the most troublesome in MPC5500-based systems. These effects are ringing, VDDE droop, and ground bounce.

In order to define and explain these effects, a simple model will be discussed in Section 2.1, "Simple Model." Appendix A, ": Glossary of Terms" also provides definitions for special technical terms used in this document.

Ringing, VDDE droop, and ground bounce can cause a host of potential issues in the system. Two potentially dangerous issues in MPC5500-based systems are false switching and double clocking. These issues are further discussed in Section 2.2, "Potential Issues."

2.1 Simple Model

Consider the simple model shown in Figure 1. This model consists of two inverters and their capacitive loads. Resistors are used to model the impedance of the bondwires that connect to VDDE, VSSE, and the outputs of the two inverters. In other words, this is a simple four-pin chip.

Suppose that the input to the switching inverter changes state from a logic 1 to a logic 0, causing the inverter's N-channel MOSFET to turn off and its P-channel MOSFET to turn on. When the P-channel MOSFET turns on, current flows from the board power supply through the P-channel MOSFET and out to the load capacitor, thereby charging up the load capacitor. When the inverter's input changes state from a logic 0 to a logic 1, its P-channel MOSFET turns off and its N-channel MOSFET turns on, causing current ($I_{discharge}$) to flow from the charged up load capacitor through the N-channel MOSFET and out to ground (gnd). The switching inverter creates a waveform, called the 'switching line,' which transitions from low-to-high and then from high-to-low. Meanwhile, the quiet inverter has an unchanging logic 1 input, which means that its P-channel MOSFET is off and its N-channel MOSFET is on. This results in the quiet inverter having a steady output that is at the ground potential. The output of the quiet inverter is called the 'quiet line' and it too has a load capacitor connected to it.

When the switching inverter goes from high-to-low, the load capacitor connected to the switching inverter discharges producing a current labeled $I_{discharge}$ that flows to ground. After flowing through the switching inverter's N-channel MOSFET, $I_{discharge}$ then flows through the VSSE routing on the chip following two paths out the chip to ground. One path is through the VSSE bondwire, and current that flows through this path is called I_{gnd}. The other path is through the quiet inverter's N-channel MOSFET, output bondwire, and load capacitor. Current that flows through this unintended path is called I_{quiet}. Ground bounce is caused by I_{gnd} flowing through the VSSE bondwires. Quiet line bounce is caused by I_{quiet} flowing out the quiet inverter's output bondwire and charging up the quiet inverter's load capacitor. Ground bounce and quiet line bounce can both be seen in the waveforms in Figure 1. Often, the term ground bounce is used when discussing either the actual ground bounce or the quiet line bounce.

When the switching inverter transitions from a low-to-high, the load capacitor connected to the switching inverter charges up. The current required to charge up the load capacitor comes from the board power supply. The charging current flows out the board power supply, through the VDDE bondwire, through the switching inverter's P-channel MOSFET, through the output bondwire, and ultimately to the load capacitor. As the charging current flows through the VDDE bondwire, VDDE droop occurs. Furthermore,

quiet line droop can occur if the quiet inverter's P-channel MOSFET is turned on while the charging current is flowing. Quiet line droop is caused by current flowing from the quiet inverter's load capacitor, through the quiet inverter's P-channel MOSFET, through the VDDE routing on chip, through the switching inverter's P-channel MOSFET, out the switching inverter's output bondwire, and ultimately to the switching inverter's load capacitor. Often, the term VDDE droop is used when referring to either actual VDDE droop or quiet line droop.

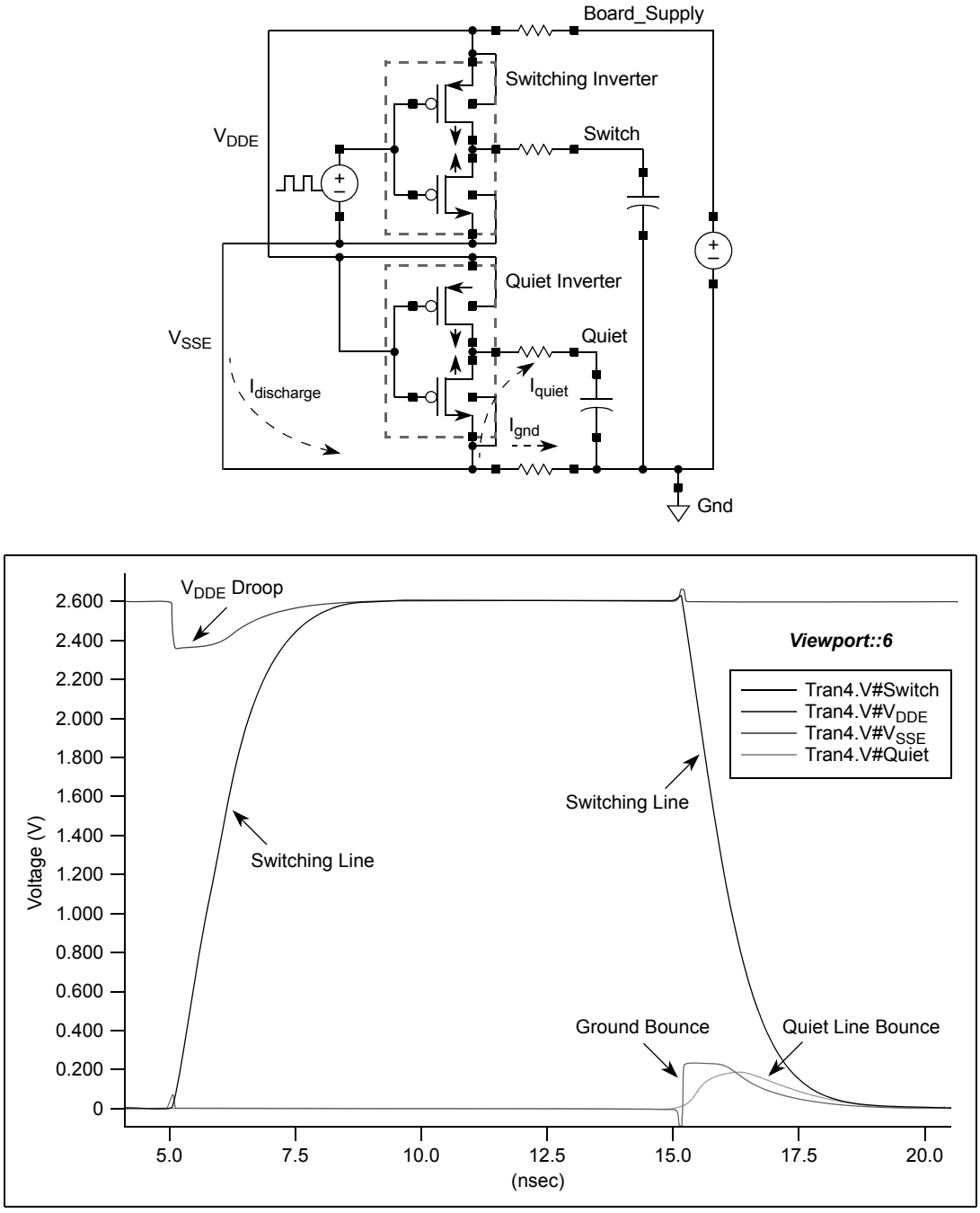

Figure 1. Simple Model with Resistive Return Path

Another way of looking at quiet line bounce and quiet line droop is by examining the isolation of the charge on the quiet inverter's load capacitor. When the switching inverter transitions from a low-to-high, current is needed to charge the switching inverter's load capacitor. This charging current mostly comes from the board power supply by way of the VDDE bondwire. However, some current comes from the quiet inverter's load capacitor. The better the isolation of the quiet inverter's load capacitor, the smaller the amount of current that gets pulled from the quiet inverter's load capacitor, and thus the smaller the amount of quiet line droop that will occur. When the switching inverter transitions from a high-to-low, current is discharged from the switching inverter's load capacitor. Most of the discharge currents flows to ground through the VSSE bondwire. However, some of the discharge current flows out through the quiet inverter's output bondwire and charges up the quiet inverter's load capacitor causing quiet line bounce. The better the isolation of charge on the quiet inverter's load capacitance, the less quiet line bounce that will occur.

Now consider what happens when the bondwires are modeled using an inductor instead of a resistor. Figure 2 shows a schematic of the simple model using inductors to model the bondwires. In this case, a simple RLC circuit is formed. When the switching inverter's load capacitance is charged up and the switching inverter's N-channel MOSFET turns on, the charge on the load capacitor is discharged to ground. In this case, the resistance of the switching inverter's N-channel MOSFET, the inductance of the bondwires, and the capacitance of the switching inverter's capacitor form the RLC circuit. Usually, the RLC circuit will be underdamped and undershoot will occur. Also, the waveform produced will oscillate as energy is transferred back and forth between the capacitance and inductance. The oscillations will be damped by the resistance and eventually the circuit will become stable at the ground potential. The oscillations are known as ringing.

Many conclusions can be drawn from analyzing these two simple models.

First, ground bounce and VDDE droop occur because the ground and VDDE bondwires have an impedance associated with them and current flowing through that impedance will cause a voltage drop. It should be noted that ground bounce and VDDE droop can be seen in the waveforms for both simple models. In the first model, the bondwire impedance is resistive; in the second model, the bondwire impedance is inductive. In both models, the bondwire impedance produces a voltage drop. The way to reduce the amplitude of the ground bounce and VDDE droop is to reduce the magnitude of the VSSE and VDDE impedance. Methods for accomplishing this will be further discussed later in this application note.

Second, when the bondwire is modeled using an inductor a simple RLC circuit results. Usually, this RLC circuit is underdamped creating overshoot, undershoot, and ringing. The way to control overshoot, undershoot, and ringing is to make the RLC circuit look less underdamped and more critically damped. Methods for accomplishing this will be further discussed later in this application note.

Third, the quiet line bounce is not exactly equivalent to the ground bounce. Likewise, the quiet line droop is not exactly equivalent to the VDDE droop. Nonetheless, the terms ground bounce and VDDE droop are usually used to refer to quiet line bounce and quiet line droop as well.

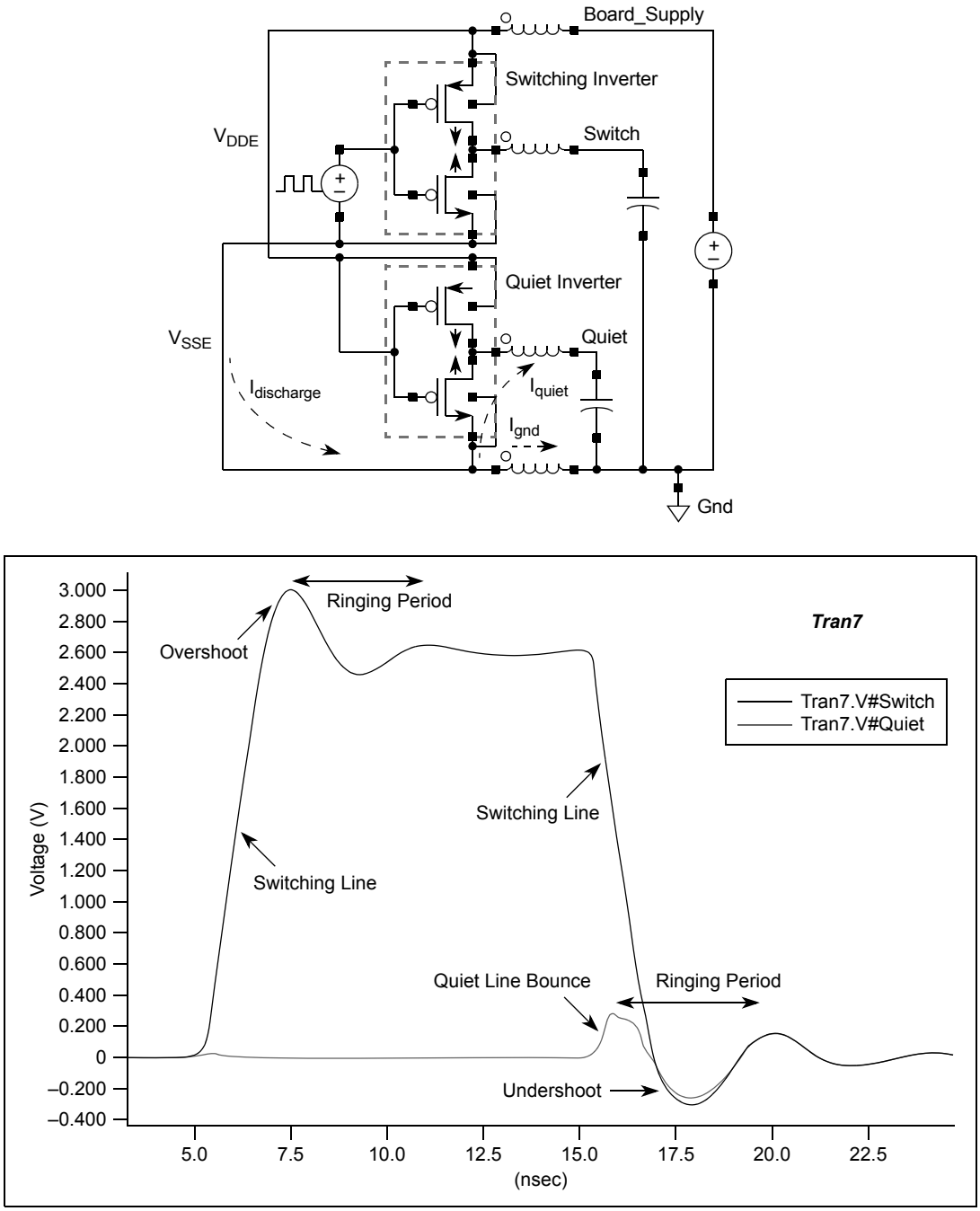

Figure 2. Simple Model with Inductive Return Path

2.2 Potential Issues

Ringing, ground bounce, and VDDE droop can potentially cause many issues for MPC5500-based systems. Two significant issues that should be considered are false switching and double clocking.

False switching and double clocking could easily occur in a poorly designed MPC5500-based system. However, false switching and double clocking will not occur in a well designed MPC5500-based system.

The guidelines outlined in Section 3, “Recommended Guidelines” should be followed to ensure a well designed board.

2.2.1 False Switching

False switching can occur on bus pins that are not supposed to switch. Quiet lines at a logic 1 state are subject to false switching to a logic 0 state when VDDE droop occurs; quiet lines at a logic 0 state are subject to false switching to a logic 1 state when ground bounce occurs. In order for a memory input to experience false switching, the quiet line glitch due to VDDE droop or ground bounce must be of a large enough amplitude and a long enough duration such that the memory input’s flip-flop switches state.

One conservative approach to ensure that false switching does not occur is to make sure that the ground bounce amplitude is less than the VIL of the memory, and likewise that the VDDE droop is above the VIH of the memory. This approach is conservative because VIL and VIH are the DC input thresholds, and the memory can actually withstand glitches of larger magnitude for short periods of time. It should also be noted that the glitch amplitude will be smaller on the memory die than it will be on the board trace due to the parasitic filtering of the memory package and bondwire.

The best way to ensure that false switching will not occur in a MPC5500-based system is to follow the board design guidelines presented in Section 3, “Recommended Guidelines” and then to test for false switching by taking measurements in the actual system.

False switching can occur on any of the MPC5500 pins, but is mostly a problem with the address and data bus. The address and data bus pins are the most susceptible to false switching because the glitch amplitude is highest when many adjacent pins switch simultaneously.

Glitches on the address and data bus pins will result in incorrect writes to the memory, as either the wrong data is written to the correct address location or the correct data is written to the wrong address location. Although memory write failures are the primary concern with false switching, all pins located near the address and data pins should also be examined for glitches. Pins that are located very far away from the switching pins are unlikely to have a large enough glitch amplitude to cause false switching.

One final note on false switching is that large quiet line glitches are acceptable as long as they do not occur during signal valid times. For example, large glitches may occur on the data bus when the data bus is switching, but as long as these signals settle out to their true values before the data valid time, then the large glitches do not matter. In general, it is very desirable to try and maximize the amount of settling time available.

2.2.2 Double Clocking

Severe ringing can cause unintended edges on clock signals. For example, consider the waveform in Figure 3 and suppose that its rising edge is used as a clock reference. The first clock edge is seen on the signal’s initial rising edge. This is the intended 1st clock edge. However, the signal then experiences severe ringing and the voltage collapses enough such that a falling edge is seen. Then the ringing causes the voltage to rise again, causing an unintended 2nd rising edge. This unintended 2nd rising edge results in double clocking because two rising edges are seen in one period. Severe ringing occurs when the circuit is severely underdamped. In a MPC5500-based system, severe ringing can occur when a fast pad (pad type = pad_fc) is enabled in its highest drive mode (mode = 11) when driving light loads (ex: 10pF) with

uncontrolled impedance signal routing. In order to ensure that double clocking does not occur in a MPC5500-based system, all signals used as clock references should be tested by taking measurements on the actual application board.

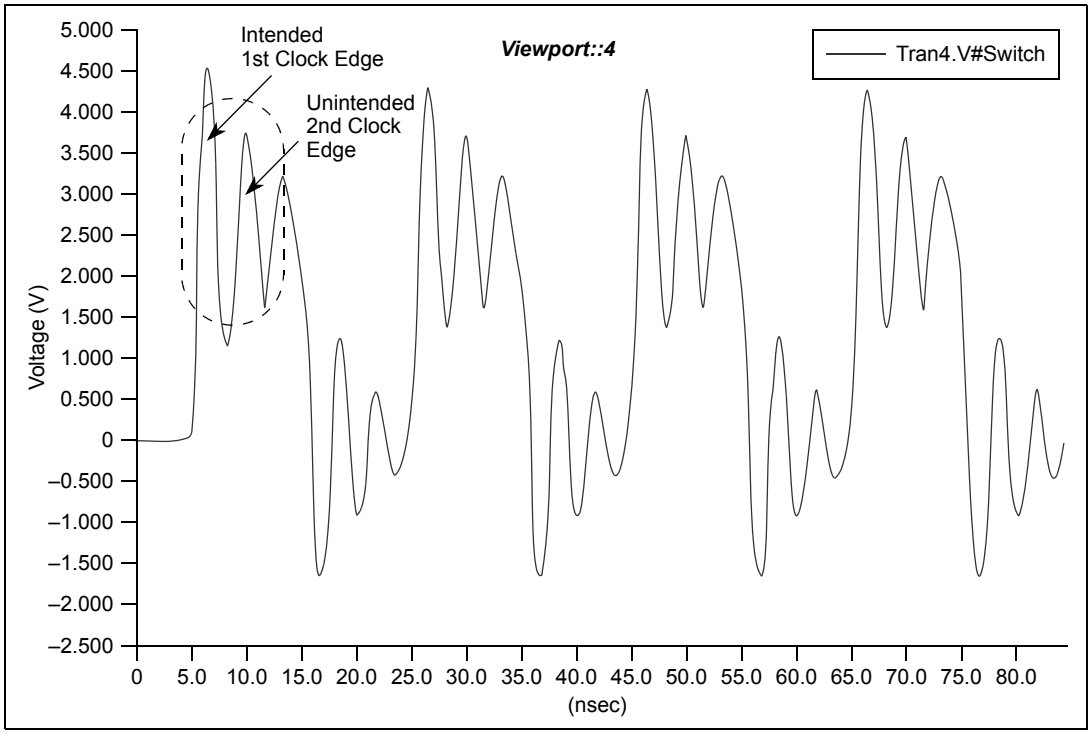

Figure 3. Double Clocking

3 Recommended Guidelines

In order to reduce the risk of experiencing a signal integrity problem, the following board design guidelines should be followed. The guidelines are divided into two sections; the first section addresses software guidelines and the second section addresses hardware guidelines.

Many simulations of anticipated MPC5500-based systems were performed to develop the guidelines described in this section. Appendix B, “: Data Bus Simulations” and Appendix C, “: CLKOUT Simulations” describe the simulations that were performed and should be reviewed by those interested in a deeper understanding of the basis and importance of the guidelines.

3.1 Software Guidelines

3.1.1 Match Drive Strength Selection to Application Load

The pad_fc allows for four drive mode options. The drive mode 11 is the lowest impedance and the drive mode 00 is the highest impedance (see Appendix D, “: Driver Impedance” and Table 1).

Table 1. Drive Mode Options for pad_fc

Drive Mode	Drive Strength
00 (weakest)	10 pF
01	20 pF
10	30 pF
11 (strongest)	50 pF

It is extremely important to select the appropriate drive mode for the specific application. In general, the goal is to drive as slow as possible while still meeting the timing requirements for the specific application. Normally, drive mode 00 should be used when there is one memory load. Similarly, drive mode 01 should be used for two memory loads and drive mode 10 should be used for three memory loads. Furthermore, if slower rise and fall times are acceptable in the specific application, then the two memory and three memory loads may be driven with a reduced drive mode. Simulated derated rise and fall times are provided in Appendix E, ": Derated Data Bus Simulations".

3.2 Hardware Guidelines

3.2.1 Route Bus Signals with Controlled Impedance

All bus signals should be routed with controlled impedance. The bus signals include address and data pins, control signals, and CLKOUT. The controlled impedance routing can be either stripline or microstrip geometries, although stripline is preferred over microstrip. Figure 4 shows a side view of the stripline and microstrip geometries. The ground planes shown in the stripline and microstrip drawings could be power planes instead, as long as good decoupling is used on both the driving and the receiving devices. The characteristic impedance (Z_0) of the board trace should be equal to the average driver impedance (see Table 6). Using a Z_0 that is less than the average driver impedance is acceptable, as long as the slower edges resulting from an overdamped line is acceptable. Using a Z_0 that is greater than the average driver impedance will result in an underdamped line that will cause overshoot. If the overshoot amplitude for the underdamped line is too high, a series termination resistor can be used. The bus signals should be routed on only one layer. Routing on more than one layer will cause impedance discontinuities. Also, slots in the power or ground planes should be avoided as they too will cause impedance discontinuities. Follow the bus traces from driver to receiver and make sure that there are no slots in the power and ground planes around the signal trace which would obstruct the flow of return current on the reference planes. Similarly, bus signals should not be routed over via antipads in the reference planes as the via antipads will also cause impedance discontinuities. Finally, there should not be any embedded traces in the reference planes especially around the bus signals.

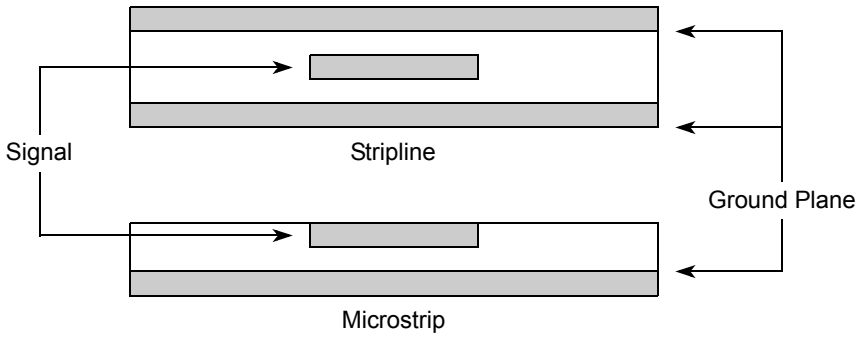

Figure 4. Stripline and Microstrip Routing

3.2.2 Use Termination Resistors on Bus Signals

When the characteristic impedance (Z_0) of the board trace routing is greater than the average driver impedance (Z_S), the line is underdamped and overshoot will occur. In order to make the line critically damped, a termination resistor (R_T) should be used. The value of the termination resistor can be calculated from the following equation.

$$R_T = Z_0 - Z_S \qquad \textit{Eqn. 1}$$

For example, if the drive mode 10 is selected with a VDDE of 2.5V, then the average driver impedance is 26.5 Ω. If the pad is driving a transmission line with a characteristic impedance of 50 Ω, then a 23.5 Ω termination resistor should be used.

In addition to the impedance matching described above, termination resistors also help to isolate the quiet lines from VDDE droop and ground bounce. Even small values of resistance (i.e. 10 Ω) can significantly help to isolate the quiet lines.

Termination resistors can also help when uncontrolled impedance routing or very short transmission lines are used. In these cases, it is a little harder to determine what value of termination resistor to use. One simple approach is to continue increasing the resistor value on the board until the overshoot amplitude is reduced to an acceptable level.

The use of termination resistors will slow down the edge rates. The amount of how much the edge rate will be increased can be approximated by using the RC time constant. The time it takes to charge the load capacitor up 95% is calculated by multiplying three times the RC time constant, or 3RCs. For example, if Z_S is 25 Ω, there is a 30 pF capacitive load, and no resistor is used then 3RCs will be 2.25 ns. However, if a 25 Ω resistor is used, then 3RCs will be 4.5 ns. In order words, when the total resistance (Z_S+R_T) was doubled, the rise time doubled. Of course, this is just an approximation. The best way to determine the impact of a termination resistor on edge rates is to measure the edge rate on the application board.

Termination resistors should be located near the driver as opposed to the receiver.

3.2.3 Minimize Board Propagation Delay

Board propagation delay is the amount of time it takes a signal to propagate from the driver to the receiver. The board propagation delay can be approximated by the following equation.

$$\text{prop delay} = (\text{length of line}) / (1.5 \times 10^8 \text{ meters/second}) \quad \textit{Eqn. 2}$$

For example, a 4 cm long line would have a prop delay of approximately 266 ps. A more accurate calculation of the prop delay would take into account the dielectric constant of the board and the board routing characteristic impedance; however, that type of analysis is beyond the scope of this application note. For our purposes, the equation given above is a close enough approximation.

The board propagation delay should be minimized. This is accomplished by minimizing the length of the routing lines. The prop delay will determine when the reflection comes back. The sooner the reflection comes back, the faster the signal will rise and the sooner the signal will settle out.

3.2.4 Avoid Routing Stubs

Routing stubs are board traces that do not connect to a load. For example, traces may be connected to a footprint for a memory device, but then the memory device is not populated. Since there is no load at the end of a routing stub, large amplitude reflections will be created. It is recommended that routing stubs be avoided. However, if routing stubs are necessary, then the routing stubs should be terminated.

3.2.5 Use Good Decoupling Techniques

Good board decoupling of the bus power supply is very important to ensure signal integrity. The general recommended technique is to have a dedicated power plane (i.e. VDDE plane) for the bus supply and then decouple the power plane. All bus supply balls should be connected directly to the power plane. There should be at least one via per supply ball; more vias are even better. There should be at least three values of discrete surface mount capacitors, all of which connect between the power plane and the ground plane. The power plane and the ground plane should be adjacent layers and the distance between the planes should be minimized (i.e. do not have thick core material between the power and ground planes). The positive terminal of the decoupling capacitors should be connected to the power plane with at least two vias. Likewise, the negative terminal of the decoupling capacitors should be connected to the ground plane with at least two vias.

Convenient values for the decoupling capacitors are 10 nF, 100 nF, and 10 µF. The high frequency current will be pulled from the 10 nF capacitors, and the 100 nF and 10 µF capacitors are used to recharge the 10 nF capacitors. The location of the 10 nF capacitors is very important. The 10 nF capacitors should be located as close as possible to the MPC5500 device. The 10 nF capacitors should be located on the opposite side of the board as the MPC5500 device and positioned in the keep out area of the ball grid array (see Figure 5). If this is not possible, then the capacitors should be distributed evenly around the bus area of the MPC5500 device. The location of the 100 nF and 10 µF capacitors is not as important. There should be at least ten 10 nF decoupling capacitors used; more 10 nF capacitors is even better. One 100 nF and one 10 µF capacitor is generally sufficient.

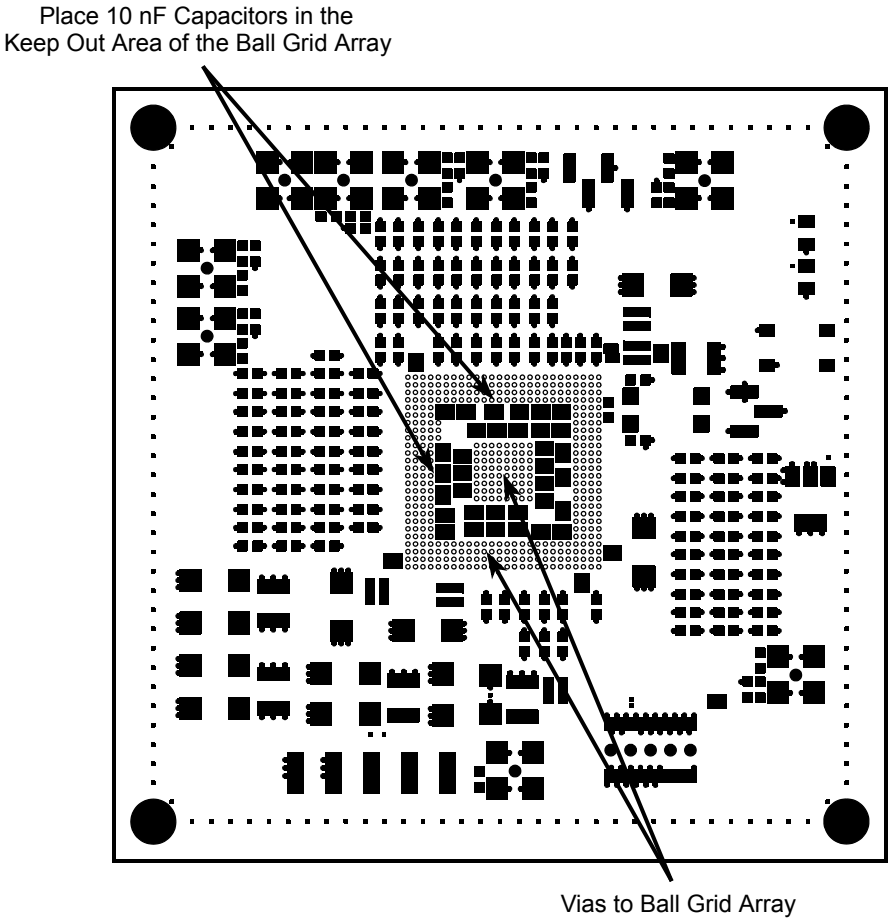

Figure 5. Bus Decoupling Capacitor Layout Example

Board decoupling of the CLKOUT supply is less important than board decoupling of the bus supply, because the CLKOUT supply has 600 pF of on-chip decoupling capacitance, whereas the bus supply does not have any on-chip decoupling capacitance. In fact, in many applications, the CLKOUT supply balls can be connected directly to the bus power plane without having to add any additional decoupling capacitors. Generally speaking, if the CLKOUT application load is 30 pF or less, then a discrete decoupling capacitor is not needed for the CLKOUT supply. The recommended method for decoupling the CLKOUT supply is to connect the CLKOUT supply balls directly to the bus power plane and then add one additional 10 nF capacitor that should be placed as close as possible to the CLKOUT supply balls. The additional 10 nF capacitor should be connected to the power and ground planes with two vias per capacitor terminal.

Another novel approach to board decoupling for the bus supply is to use embedded decoupling capacitance. Embedded decoupling capacitance is the plane to plane capacitance that exists between the power plane and the ground plane. Embedded decoupling capacitance enhances the plane to plane capacitance by using a very thin, high dielectric constant laminate material. It is possible to get 2.2 nF per square inch using embedded decoupling capacitance. On many boards, the embedded decoupling capacitance provides enough capacitance to remove all the discrete 10 nF capacitors from the board. It is still very important to use many vias when connecting the MPC5500 power and ground balls to the power and ground planes. Also, the 100 nF and 10 µF discrete capacitors are still needed and two vias per capacitor terminal connection should still be used for them.

3.2.6 Use a Good Layer Stackup

A good layer stackup is critical in ensuring signal integrity of MPC5500-based systems. In general, a good layer stackup will have the following two characteristics.

1. There should be a dedicated power plane for the bus supply and a dedicated ground plane. The power and ground planes should be on adjacent layers such that there is a metal to metal capacitance between them. If possible, the power to ground plane capacitance should be enhanced by using an embedded capacitor laminate material.
2. The high speed signals (i.e. bus signals) will be routed on internal layers. Ideally, the high speed signals should be routed on internal layers using stripline geometry, and the adjacent reference layers should be ground.

Table 2 provides an example of a good stackup for a ten layer board.

In this example, the high speed signals (i.e. the bus signals) are routed on layer 2 and layer 4. These are internal layers and the routing is done using stripline geometry and a target characteristic impedance of 35 Ω. The reference planes for the stripline routing of the high speed signals are on layer 1, layer 3, and layer 5. The reference planes on these layers is ground, but full ground planes are not used. Instead, partial ground planes are used only in the areas where the high speed signal routing is done. Using partial ground reference planes allows other routing to be accomplished on these layers as well.

This example also includes a power plane specifically for the bus supply. The bus supply power plane is layer 7, labeled 2.6 V. Layer 8 is one of several ground planes. The laminate material between layer 7 and layer 8 is an embedded capacitor laminate. There are also embedded capacitors between layers 8 and 9, and layers 9 and 10.

Table 2. Layer Stackup Example

Layer	Type	Description
1	plane/signal	ground, components
2	signal	high-speed signal
3	plane	ground, 3.3V, 5.0V
4	signal	high-speed signal
5	plane	ground
6	signal	signal
7	plane	2.6V (bus supply)
8	plane	ground
9	plane	1.5V (V_{DD} supply)
10	plane	ground, components

The 10 layer stackup discussed is only an example and is used to highlight several available techniques. Many applications will use fewer layers. The minimum recommended number of layers for an expanded mode application is 6 layers. The techniques presented in the 10 layer example can also be applied to applications which use fewer layers although tradeoffs will need to be made.

3.2.7 Board Design Checklist

The board design checklist in this section can be used to make sure that all guidelines have been considered when performing the board design. Checklist items #1-7 should be done for all bus signals for the specific MPC5500 device used.

Pad Configuration

1. Pad drive mode matched to application load and timing target.

Signal Routing

2. Z_0 set equal to Z_S

   If the target Z_0 is too small to be achieved by the specific board, then series termination resistors are used and $R_T = Z_0 - Z_S$.
3. Traces are routed on internal layers.
4. Traces do not jump layers (i.e. routed on layer 2 for 2 cm then routed on layer 4 for 2 cm.)
5. Traces are as short as possible.
6. No routing stubs are present in the traces.
7. Signal reference planes (i.e. for stripline or microstrip routing) do not have slots, embedded traces, or any other features which would obstruct the flow of signal return current.

Decoupling

8. There is a dedicated power plane for the bus supply (i.e. VDDE plane).
9. There is a dedicated ground plane adjacent to the VDDE plane.
10. The MPC5500 device's bus supply and CLKOUT supply balls are connected to the VDDE plane with at least one via per ball.
11. The MPC5500 device's ground balls are connected to the ground plane with at least one via per ball.
12. There are at least ten 10 nF decoupling capacitors connected to the VDDE and ground planes, or a sufficient amount of embedded decoupling capacitance is present between the VDDE and ground planes.
13. The 10 nF decoupling capacitors are located as close as possible to the bus VDDE balls.
14. There are at least one 100 nF and one 10 µF decoupling capacitors connected to the VDDE and ground planes.
15. All decoupling capacitors are connected to the VDDE and ground planes with at least two via pairs per capacitor.
16. If the CLKOUT load is greater than 30 pF, then a 10 nF capacitor is used for decoupling the CLKOUT supply and this capacitor is located as close as possible to the CLKOUT VDDE ball(s).

4 IBIS Simulations

4.1 Performing IBIS-based Signal Integrity Simulations

IBIS models are available for MPC5500 devices. The IBIS model can be used with board level signal integrity tools in order to perform board-level signal integrity simulations. These types of simulations are

extremely useful for examining relative effects such as comparing the overshoot on a signal routed with a 150 Ω characteristic impedance versus a 75 Ω characteristic impedance. IBIS-based simulations are also somewhat useful for determining absolute performance such as addressing whether the quiet line bounce will cause false switching. However, the uncertainty of the modeling must be taken into consideration when looking at absolute performance. In general, the simulations will predict worse performance than will actually occur; therefore, there will be a significant number of false warnings when looking at absolute performance. Nevertheless, it is better to experience a false warning than to have no warning at all.

4.2 How to Calculate the Average Driver Impedance from the IBIS Model

The average driver impedance can be calculated from the IBIS model. It is useful to determine the average driver impedance when determining how best to impedance match the driver to a load. The IBIS model is an ASCII file and can be opened using any text editor. Inside the device IBIS model there will be models for each pad type. The fast pad is called pad_fc. There will be four different pad_fc models: one for each drive mode. For each drive mode, there will be a pull-up and pull-down table. Select the typical pull-up and pull-down currents (I_{typ}) at the midpoint voltage. The midpoint voltage ($V_{midpoint}$) will be VDDE/2. For example, in the model where VDDE is equal to 1.8V the midpoint voltage is 900 mV. Calculate the pull-up and pull-down impedance by using the following equation.

$$Z_S = V_{midpoint}/I_{typ} \qquad \textit{Eqn. 3}$$

The average driver impedance is then calculated by taking the average of the pull-up and pull-down impedances.

5 References

5.1 MPC5500 Family Reference Documentation

1. *MPC5553/MPC5554 Reference Manual*

5.2 Freescale Semiconductor Application Notes

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3. Dobrasevic, Stevan. “EMC Guidelines for MPC5500-based Systems.” Freescale Semiconductor Application Note AN2706. 2004

5.3 General Signal Integrity References

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3. Ott, Henry. *Noise Reduction Techniques in Electronic Systems*. Wiley and Sons, 1976.

Appendix A: Glossary of Terms

- Bondwire - This is a small wire which connects the chip to the package.
- BGA - ball grid array. This is a type of semiconductor package.
- Die - Another name for the micro controller chip.
- Drive mode xx - This refers to the drive mode selection of the pad. For the pad_fc, there are four drive modes available. The strongest drive mode is drive mode 11 and the weakest drive mode is drive mode 00. The mode number refers to actual bits so could be expressed as drive mode 0b11 or drive mode 0b00.
- Ground bounce - An increase in the on-chip ground voltage when a pad drives from high-to-low.
- Overshoot - When voltage in a circuit exceeds the supply voltage due to reactive effects in a underdamped circuit.
- Pad - This is a small block on the chip which performs input and output functions. A bondwire connects the pad to the package.
- Pad_fc - This is one of the functional pad types. It is the fastest pad available and it is used for the bus and nexus signals.
- Padring - Individual pads placed one next to another around the periphery of the chip.
- Pins - Any external connection on the package. Since MPC5500 devices are in BGA packages, each ball is a pin.
- PVT - Process voltage temperature. Semiconductor device behavior strongly depends on these variables, therefore, the PVT is often specified when discussing device behavior.
- Quiet line bounce - An increase in the off-chip voltage of a pin that is held at a logic 0 state as another pin switches from high-to-low.
- Quiet line droop - A reduction in the off-chip voltage of a pin that is held at a logic 1 state as another pin switches from low-to-high.
- Ringing - Oscillations in a circuit that are due to reactive effects in an underdamped circuit.
- RLC - Resistor inductor capacitor. Refers to a simple model that consists of a resistor, an inductor, and a capacitor connected in series.
- R_T - The value of a series termination resistor.
- Undershoot - When voltage in a circuit goes below the ground voltage due to reactive effects in an underdamped circuit.
- VDDE droop - A reduction in the on-chip power supply voltage when a pad drives from low-to-high.
- V_{ds} - This is the drain to source voltage of a transistor device.
- Z_0 - Characteristic impedance of a transmission line.
- Z_S - The driver impedance of a transistor. This is the impedance between the source and the drain.

Appendix B: Data Bus Simulations

This appendix presents simulation data for a realistic MPC5500-based system. The data bus was modeled as is shown in Figure 6. The padring model contains all of the transistors that are actually in the pad_fc (pad_fc is the pad type used on the data bus).

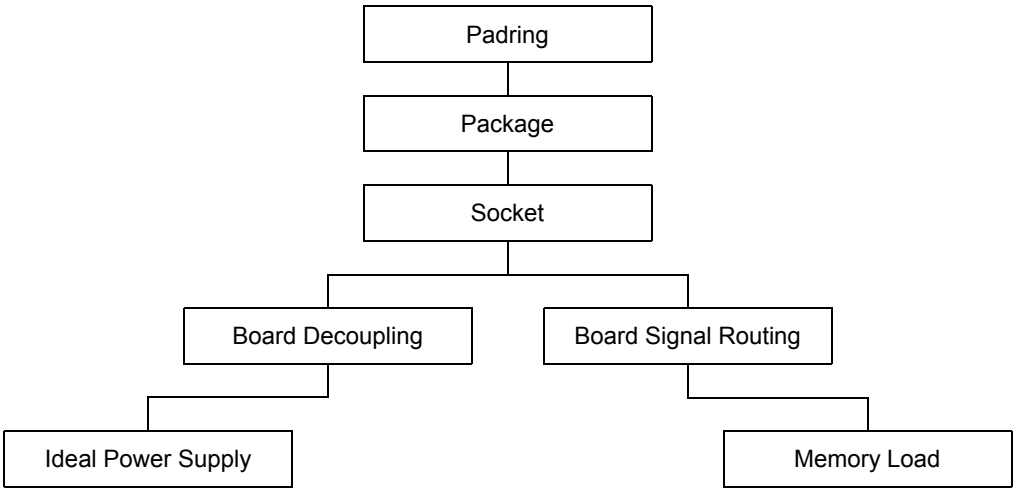


Figure 6. Block Diagram of Data Bus Model

Thirty-two pad models are instantiated; one for each data pin. There are also pad models for the VDDE and VSSE pads. All of the data, VDDE, and VSSE pads are connected together to form a mini padring. The term mini padring is used because it is a partial padring consisting of only the pads in the data bus area of the padring. The on-chip metal connections among the pads are modeled using resistors. The mini padring then connects to the package model.

The package model was extracted using an Electromagnetics tool called Momentum. The package model connects the padring to the socket.

The socket model contains just one inductor to model the L_{eff} of the VDDE connections through the socket. The socket model does not contain any elements to model the data line routing through the socket. The socket connects to the board decoupling model.

The board decoupling model contains a RLC model for each capacitor used in the model. It is assumed that the board has a power plane and a ground plane, and that the socket and the capacitors are connected directly to the planes. The board decoupling model then connects to an ideal power supply.

The data signals from the package connect to the board signal routing model. The board signal routing model contains transmission line models for each of the data signals. The board signal routing then connects to a memory load model.

Several variables were studied. Table 3 describes the configuration for each of the eleven data plots that are numbered from #1 - 11. The data plots appear in the following sections. It should be noted that the baseline case is the -40 C curve in plot #1. All variables were tested one at a time starting from the baseline. Since the VDDE droop for the baseline case is only 12%, the differences due to each of the variables appear to be less dramatic than they would be if a worse baseline had been chosen. In other words, even though all of the VDDE droop curves in a plot may appear acceptable, the point is that the variable tested

does impact the overall VDDE droop and understanding how much so is valuable knowledge. The impact of each of the variables will be given as a percentage of VDDE so that it is easier to compare the impact of different variables.

The ground bounce is not presented in the data plots, but its magnitude will be approximately the same as the VDDE droop magnitude. For example, if the VDDE droop was 500 mV, then the ground bounce would also be approximately 500 mV.

Table 3. Data Bus Simulation Variables

Plot Number	Variable	Temperature (C)	Process	Voltage (V)	Drive Mode	Decoupling Model	Termination Resistor (ohms)	Socket	Number of Memories	Routing Impedance (ohms)
1	Temperature	-40, 25, 150	bcs	1.62	00	good	0	no	1	33
2	Process	-40	bcs, typ, wcs	1.62	00	good	0	no	1	33
3	Voltage	-40	bcs	1.62, 3.60	00	good	0	no	1	33
4	Drive Mode	-40	bcs	1.62	00, 01, 10, 11	good	0	no	1	33
5	Decoupling Model	-40	bcs	1.62	00	bad, good, embed	0	no	1	33
6	Termination Resistor	-40	bcs	1.62	00	good	0, 10, 33	no	1	33
7	Socket	-40	bcs	1.62	00	good	0	yes, no	1	33
8	Number of Memories	-40	bcs	1.62	00, 01, 10	good	0	no	1, 2,3	33
9	Routing Impedance	-40	bcs	1.62	00	good	0	no	1	33, 75, 150
10	Example #1	-40	bcs	3.60	10	bad	0	no	1	150
11	Example #2	-40	bcs	3.60	11	good	0	yes	3	75

B.1 Temperature

Temperature affects the noise because it affects the signal rise and fall times. Colder temperatures result in faster edges than warmer temperatures, as can be seen in Figure 7. Therefore, the VDDE droop will be the worst at -40 C and best at 150 C. The baseline case is the -40 C curve which shows a VDDE droop of 12%. At 25 C, the VDDE droop is 10% and at 150 C it is 8%.

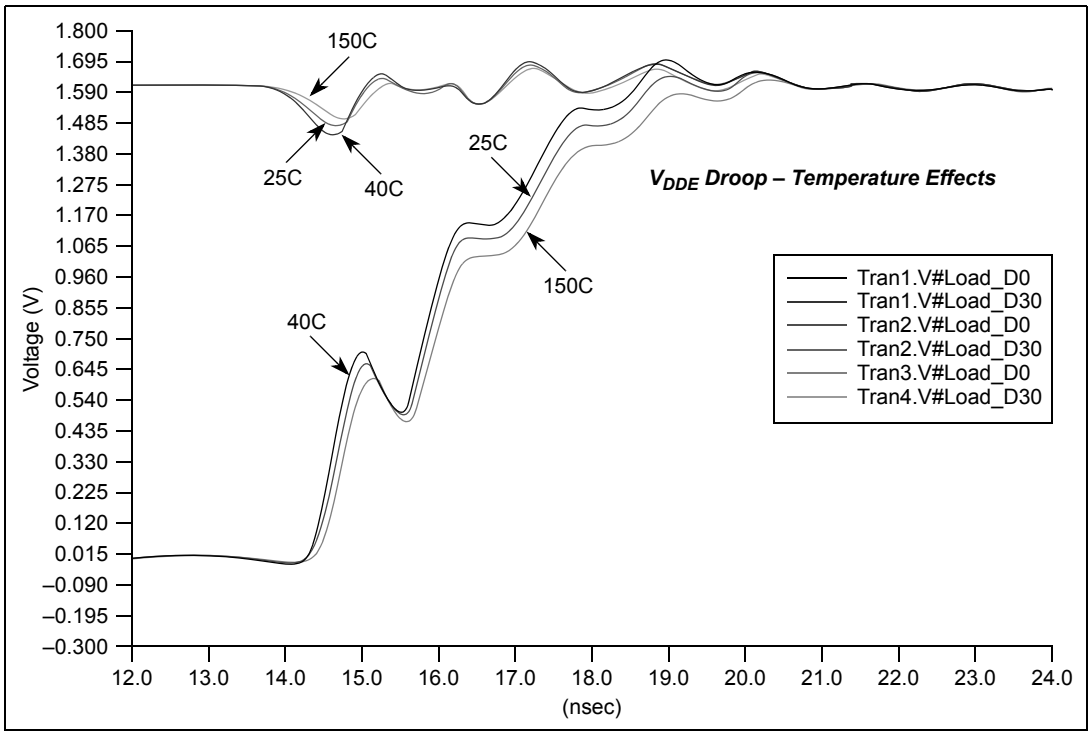


Figure 7. Temperature

B.2 Process

Variations in silicon processing affects the edge rates and thus the magnitude of the VDDE droop. For example, consider two extremes of processing variation which will be called the best case (BCS) and the worst case (WCS). A die whose process variation resembles BCS will have much faster edges than a die whose process variation resembles WCS. In other words, BCS implies that the variation in the processing features (ex: channel length, threshold voltage, etc.) for this specific die resulted in the best case or fastest die. Whereas, WCS implies that in this specific die, the variation in the processing features resulted in a worst case or slowest die. The TYP curve is for a die with typical process features. As can be seen in Figure 8, the BCS curve has the fastest rise time and the WCS curve has the slowest rise time. Correspondingly, the VDDE droop is 12% for BCS and only 6% for WCS. Therefore, two different die that were processed separately could potentially have a 2X difference in their measured VDDE droop.

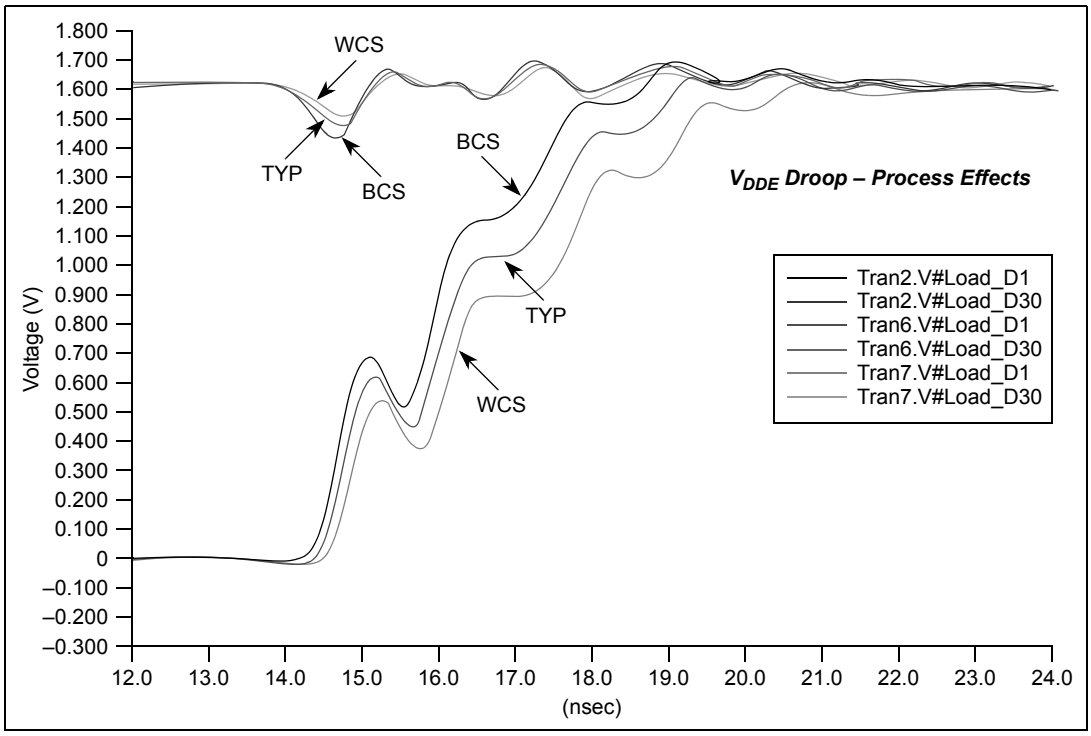


Figure 8. Process

B.3 Voltage

Edges rates are affected by the VDDE voltage. Higher voltage means faster edges. Therefore, the VDDE droop will be worse at higher voltage than it will be at lower voltage. The maximum VDDE is 3.60V and the minimum VDDE is 1.62V. The VDDE droop at 3.60V is 31% and the VDDE droop at 1.62V is 8% (see Figure 9). However, the absolute lowest VDDE droop occurs when the VDDE is 1.62V. This is because a small droop at a lower voltage can result in a lower absolute voltage than a large droop at a higher voltage. Therefore, VDDE droop should be evaluated when the VDDE is set to the maximum application voltage, as well as when the VDDE is set to the minimum application voltage.

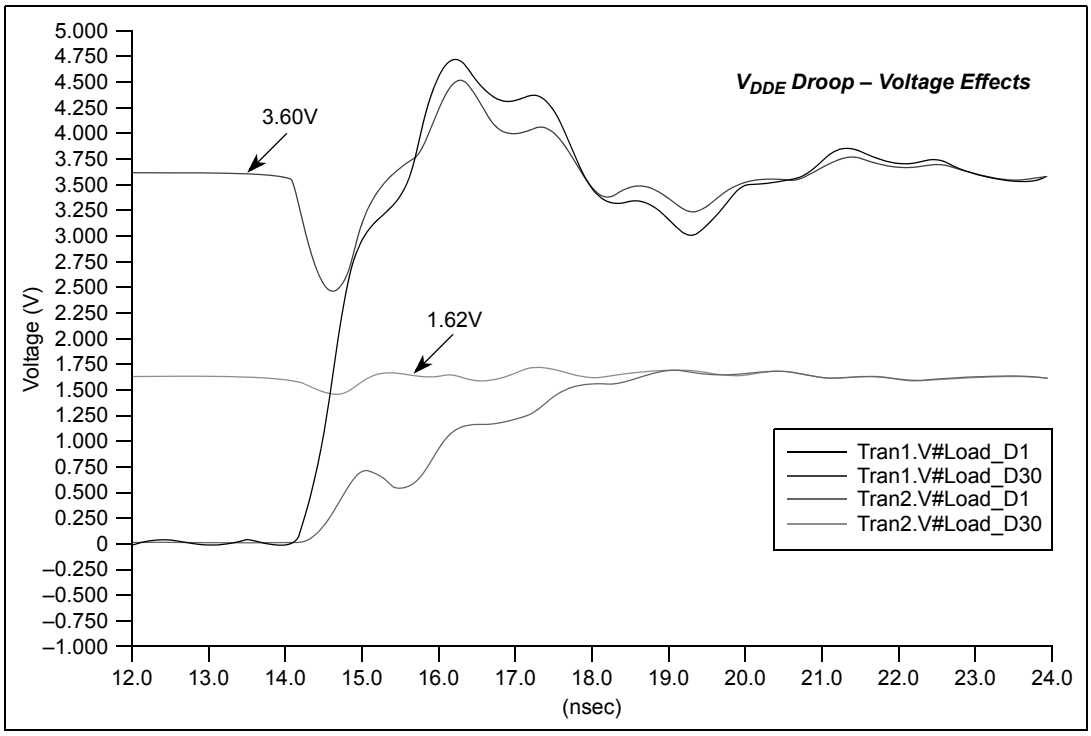


Figure 9. Voltage

B.4 Drive Mode

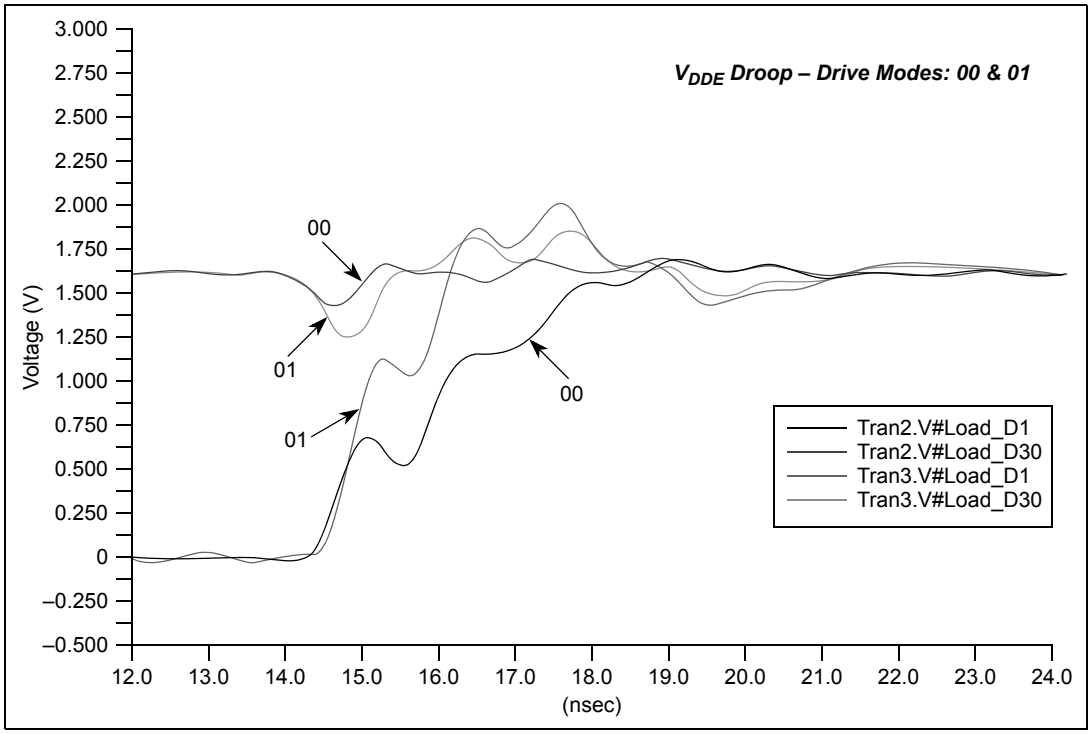
The drive mode selection has a substantial impact on both the VDDE droop and the overshoot performance. It is extremely important to select the drive mode in order to match the signal loading. For example, if the signal loading is 10 pF or less, then the drive mode 00 should be selected resulting in a 12% VDDE droop and a 1% overshoot both of which are acceptable. However, if a higher drive mode is selected to drive the 10 pF load, then the pad will be overdriving (i.e. the circuit will be underdamped) and the VDDE droop and the overshoot will get significantly worse. Table 4 summarizes the impact of overdriving a 10 pF load. If a 10 pF load is overdriven by selecting drive mode 11, then the VDDE droop will be 43% and the overshoot will be 70% both of which could potentially be unacceptable. The simulation plots for drive modes 00, 01, 10, and 11 each driving a 10 pF load can be seen in Figure 10.

Overdriving can also occur with 20 pF and 30 pF loads. If the load is 20 pF, then the drive mode 01 should be used. If drive mode 10 or 11 is used with a 20 pF load, then the load will be overdriven. If the load is 30 pF, then the drive mode 10 should be used. If drive mode 11 is used with a 30 pF load, then the load will be overdriven.

Data for the 10 pF load was included in this section because most MPC5500-based systems are expected to use only one memory device, which means that the load will be approximately 10 pF. Data was not included for the 20 pF or 30 pF cases, but overdriving these loads will also result in worse VDDE droop and overshoot performance as compared to driving the loads with their intended drive mode.

Table 4. Drive Mode Affect on VDDE Droop and Overshoot for a 10 pF Load

Drive Mode	VDDE Droop	Overshoot
00 (weakest)	12%	1%
01	23%	23%
10	32%	46%
11 (strongest)	43%	70%



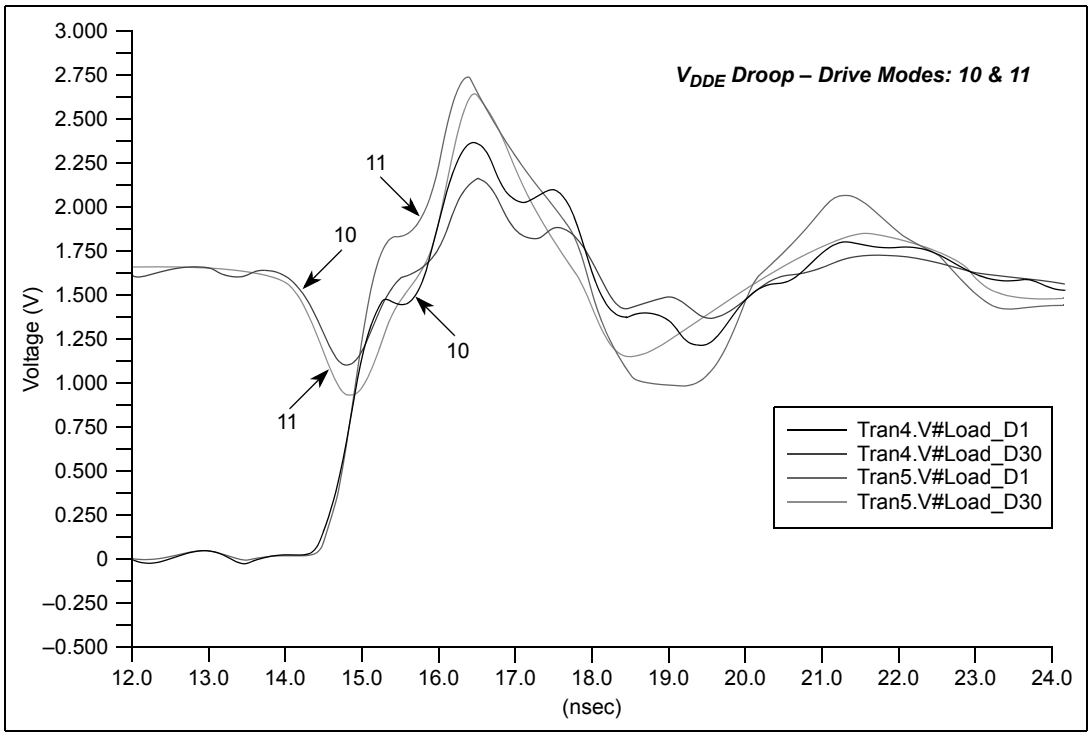


Figure 10. Drive Mode

B.5 Decoupling Models

In order to study the effect of decoupling on the VDDE droop, three decoupling models were developed. The bad decoupling model is meant to emulate a board with bad decoupling design. Likewise, the good decoupling model represents a board with good decoupling design, and the embed decoupling model represents a board that uses embedded decoupling capacitors.

Embedded decoupling capacitors are built by using special dielectric laminates to enhance the VDDE plane to ground plane capacitance in the board. For embedded capacitors, the VDDE plane and the ground plane must be on adjacent layers. The special laminates have high dielectric constants and are very thin. Each of the three decoupling models will be further discussed and then the simulation results will be shown.

The bad decoupling model can be seen in Figure 11. The model consists of four 10 nF capacitors that are in 0805 packages. The model also includes a 100 nF capacitor and a 10 µF capacitor. The equivalent series resistance (ESR) and the equivalent series inductance (ESL) of each capacitor is included in the model. All capacitors are connected to the power plane through inductors that model the vias. The bad decoupling model assumes that one via per capacitor is used to connect the positive side of the capacitor to the power plane (VDDE plane), and one via per capacitor is used to connect the negative side of the capacitor to the ground plane. In other words, there is only one via pair per capacitor. Additionally, there is a 1 µH choke filter and an ideal power supply. The power plane connects to the MPC5500 device through a 3 nH inductor which is meant to model poor board routing. There are four main characteristics that make this a bad decoupling model:

1. The poor board routing from MPC5500 device to the power plane.
2. Only one via pair per capacitor to connect to the power and ground planes.
3. Insufficient number of 10 nF capacitors.
4. The 10 nF capacitors are in the 0805 package.

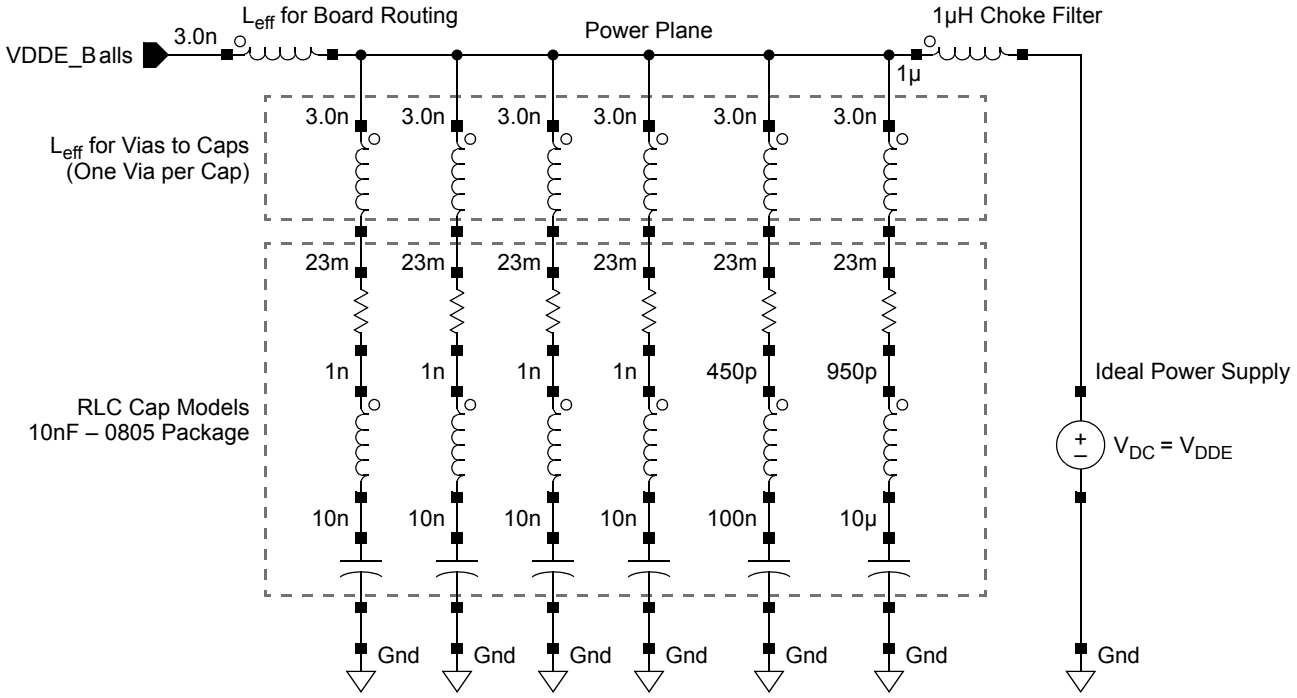


Figure 11. Bad Decoupling Model

The good decoupling model is similar to the bad decoupling model except that all four of the problems with the bad decoupling model have been fixed on the good decoupling model. Figure 12 presents a schematic of the good decoupling model. On the good decoupling model, the VDDE balls connect directly to the power plane (VDDE plane) using at least one via per VDDE ball (26 vias total). The good decoupling model has ten 10 nF capacitors, all of which are in a low inductance 0306 package and each capacitor connects to the power and ground planes with two via pairs instead of one via pair. The good decoupling model still suffers from the series resistance and inductance that is inherent in the discrete capacitor components. Also, even though there are two via pairs per capacitor, the inductance that is inherent in having to connect the discrete capacitor components to the power planes limits the performance of the good decoupling model.

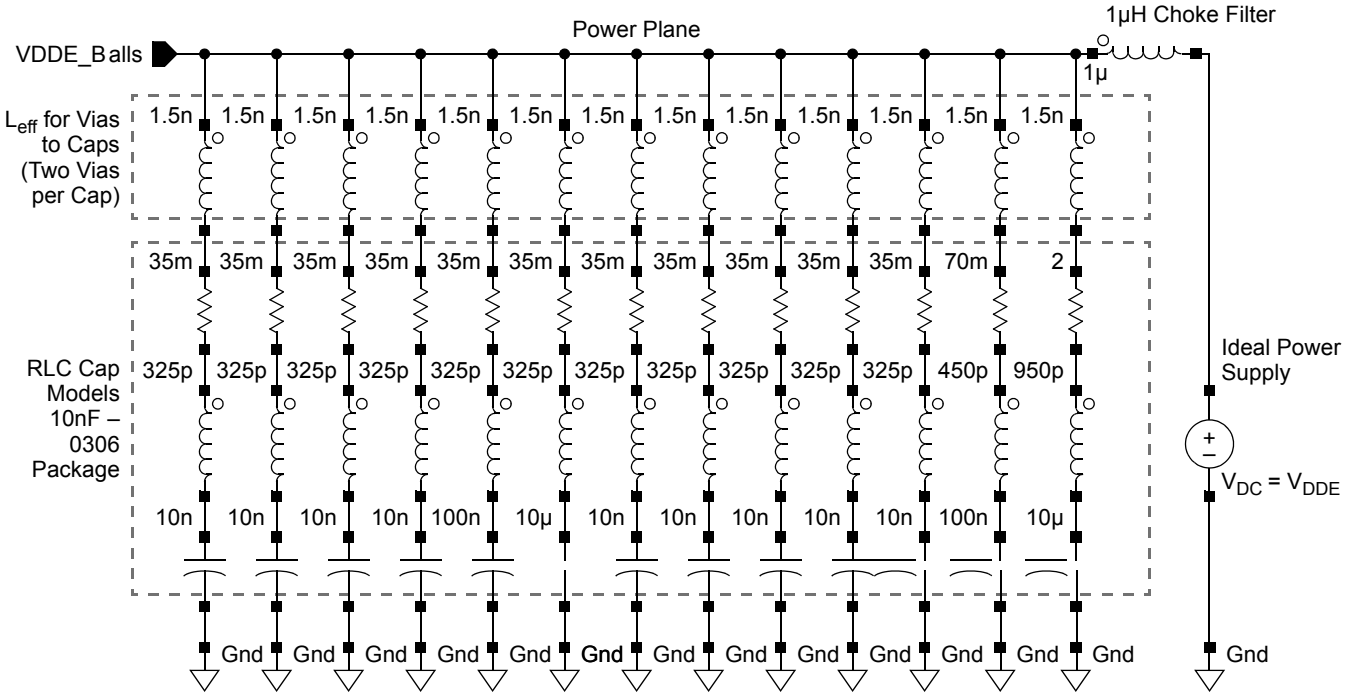


Figure 12. Good Decoupling Model

The embed decoupling model, shown in Figure 13, removes the limitations imposed on the good decoupling model by replacing the discrete capacitors with an embedded decoupling capacitor. The embedded decoupling capacitor is the capacitance between the power and ground planes that has been enhanced by using a thin, high dielectric laminate material. When developing the embed decoupling model, it was assumed that the board was 10” by 10” and that the embedded decoupling capacitor yielded 2.2 nF per square inch. This resulted in a total capacitance of 220 nF. Any series resistance or inductance associated with the embedded decoupling capacitor was left out of the model because it was assumed to be negligible.

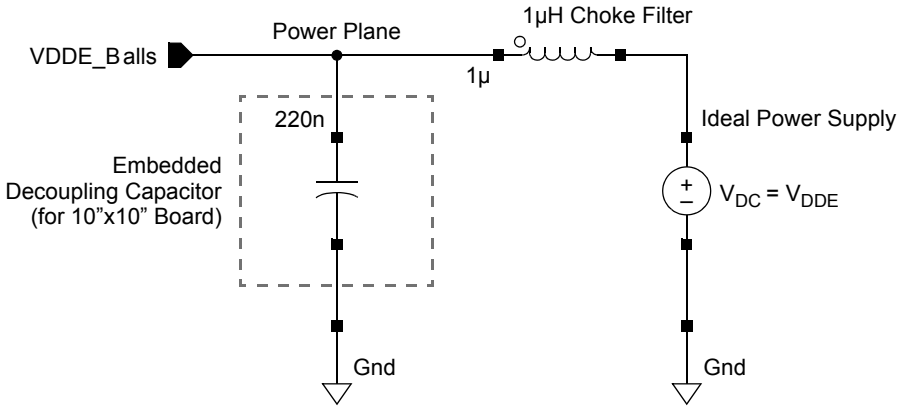


Figure 13. Embed Decoupling Model

Simulations were run using each of the three decoupling models and the results are presented in Figure 14. Looking at the data, it appears that the embed decoupling model gives the fastest edge rate, which should be expected since the embed decoupling model should have the lowest impedance. The good decoupling model edge rate is close to the embed decoupling model edge rate but just a little slower. The bad decoupling model produces an edge rate that is significantly slower than the edge rates in either of the other two models.

However, even though the edge rate is much slower with the bad decoupling model, the bad decoupling model has the worst VDDE droop performance with 20% droop. Furthermore, the bad decoupling model leads to a very unstable supply, as can be seen by the lower frequency resonances in the data plot. The good decoupling model has better VDDE droop performance with 12% droop, and the embed decoupling model has the best VDDE droop performance with only 9% droop.

Because the embed decoupling model allows faster edges with less VDDE droop, it is the preferred method of decoupling. Nonetheless, the good decoupling model probably has adequate performance for most MPC5500-based applications.

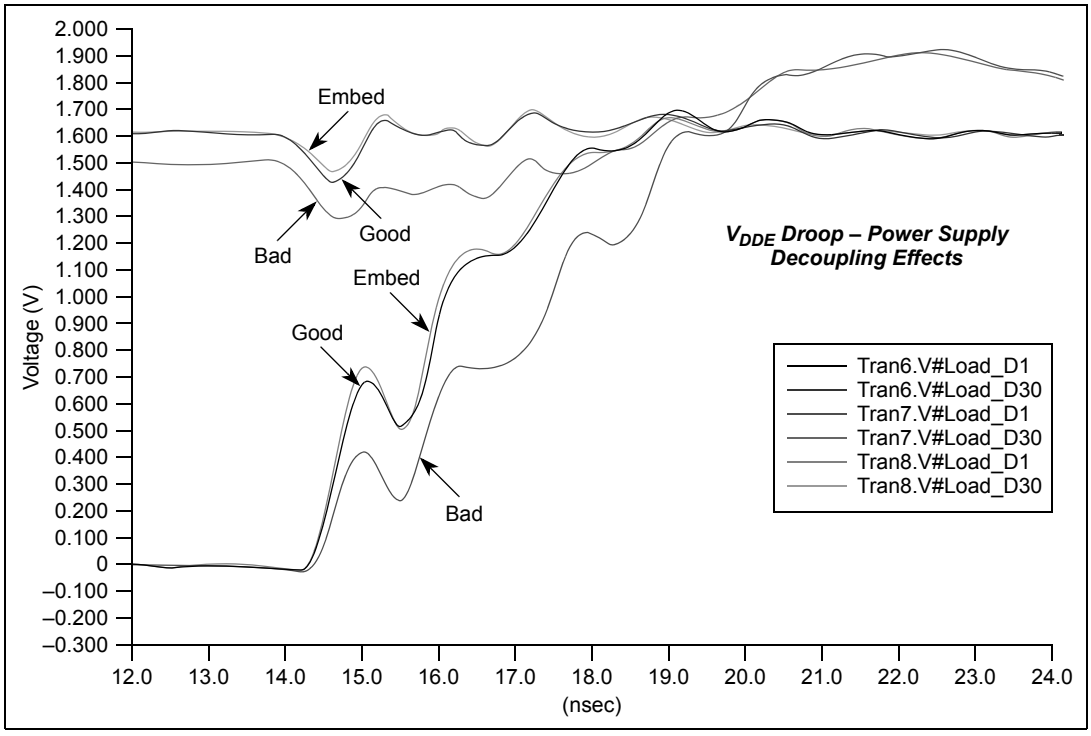


Figure 14. Decoupling Model

B.6 Termination Resistor

Figure 15 indicates that the VDDE droop with no series termination resistor (i.e. 0 Ω) is 12%, whereas, the droop is 10% when a 10 Ω resistor is used, and only 7% when a 33 Ω resistor is used.

Termination resistors can improve signal integrity in two ways. First, termination resistors can be used to critically damp a switching line circuit that would otherwise be underdamped. This will reduce overshoot

and undershoot on the switching line. The termination resistor value (R_T) should be determined using the following formula.

$$R_T = Z_0 - Z_S \qquad \textit{Eqn. 4}$$

In this formula, Z_S is the MOSFET driver impedance and in this simulation the pull-up impedance (i.e. the P-channel MOSFET impedance) is approximately 150 Ω. Z_0 is the characteristic impedance of the board routing. In this simulation, the board routing impedance is 33 Ω. Therefore, the calculated R_T is -117 Ω, which means that in this example the signal will always be overdamped even if no termination resistor is used. The circuit is known to be overdamped because Z_S is greater than Z_0, which results in a negative calculated R_T. If the calculated R_T is positive, then the circuit is underdamped. In order to make the circuit in this example critically damped, the routing impedance should be increased to 150 Ω. Another way of looking at this is that the circuit is critically damped when the driver impedance plus the termination resistor is matched (i.e. equal to) the routing impedance.

Even though the signal is already overdamped in this example, there is still a reduction in the VDDE droop when termination resistors are used.

The second way in which termination resistors improve signal integrity is that they provide isolation for the quiet lines.

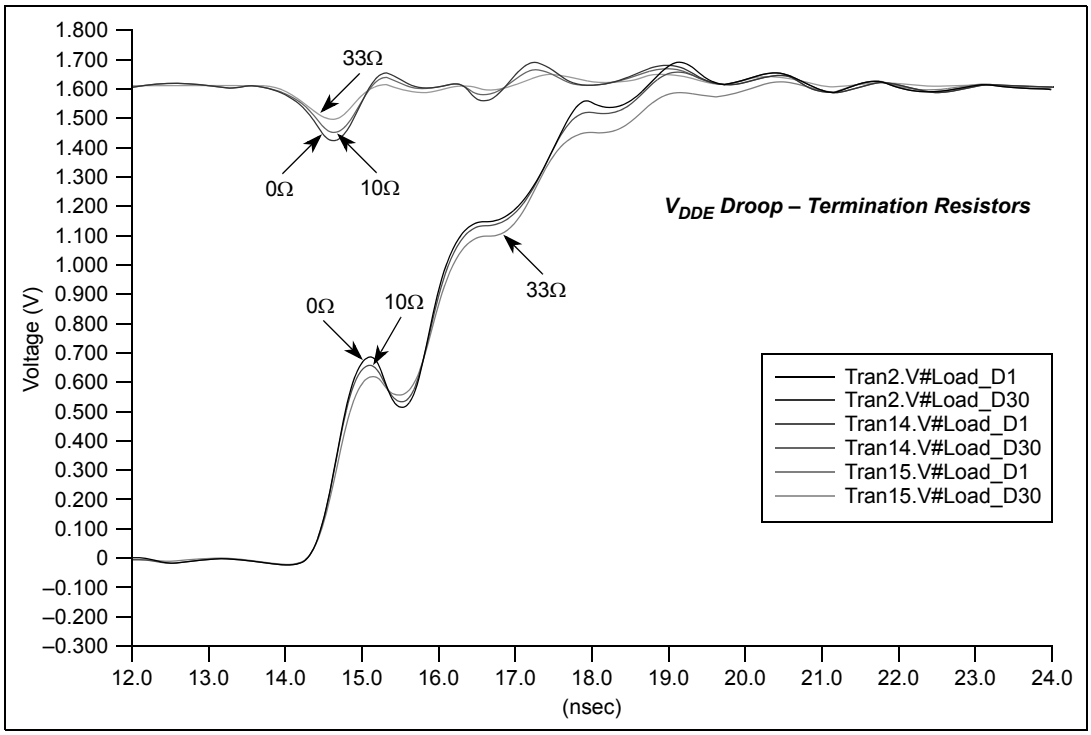


Figure 15. Termination Resistor

B.7 Socket

The use of a socket will make the VDDE droop worse because, generally speaking, the socket will increase the inductance. The VDDE droop without a socket is 9%, and the VDDE droop with a socket is 14%. The socket also slows down the edge rate, as can be seen in Figure 16.

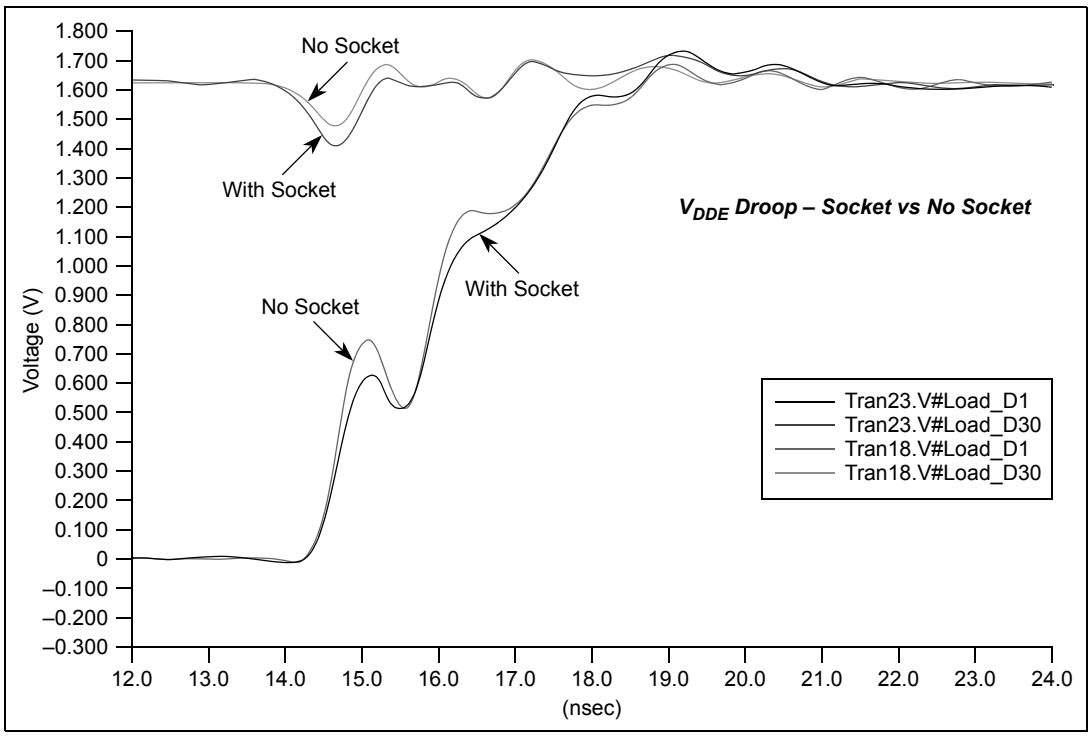


Figure 16. Socket

B.8 Number of Memories

The simulation data in Figure 17 shows the VDDE droop when driving one, two, and three memory devices. When driving one memory, the drive mode 00 was used. Similarly, when driving two memories, the drive mode 01 was used, and the drive mode 10 was selected when driving three memories. In other words, the drive mode was matched to the load.

There are two main effects that must be considered when evaluating the VDDE droop performance as a function of the number of memory devices that are driven. First, more memory devices means a heavier load, which means more drive current is required. A higher current demand will cause more VDDE droop if all else is held constant. The second effect to be considered is the edge rate. The edge rate will be determined by the drive current and the load. The design goal for pad_fc was to have the edge rates equal for each of the drive modes (assuming that each drive mode was driving its intended load). However, looking at the simulation data, it appears that the two memory load case has a slightly slower edge than the one memory or three memories cases.

The VDDE droop with three memories is the worst at 15%, followed by the one memory case which has 12% VDDE droop, and finally the two memory case results in the smallest amount of VDDE droop at only 10%. The VDDE droop is best for the two memory case because the rise time was slowest for the two

memory case. The three memory case is likely worse than the one memory case because it has more drive current.

It should be noted, the VDDE droop performance is acceptable for the one, two, or three memory loads, as long as the drive mode is selected to match the load.

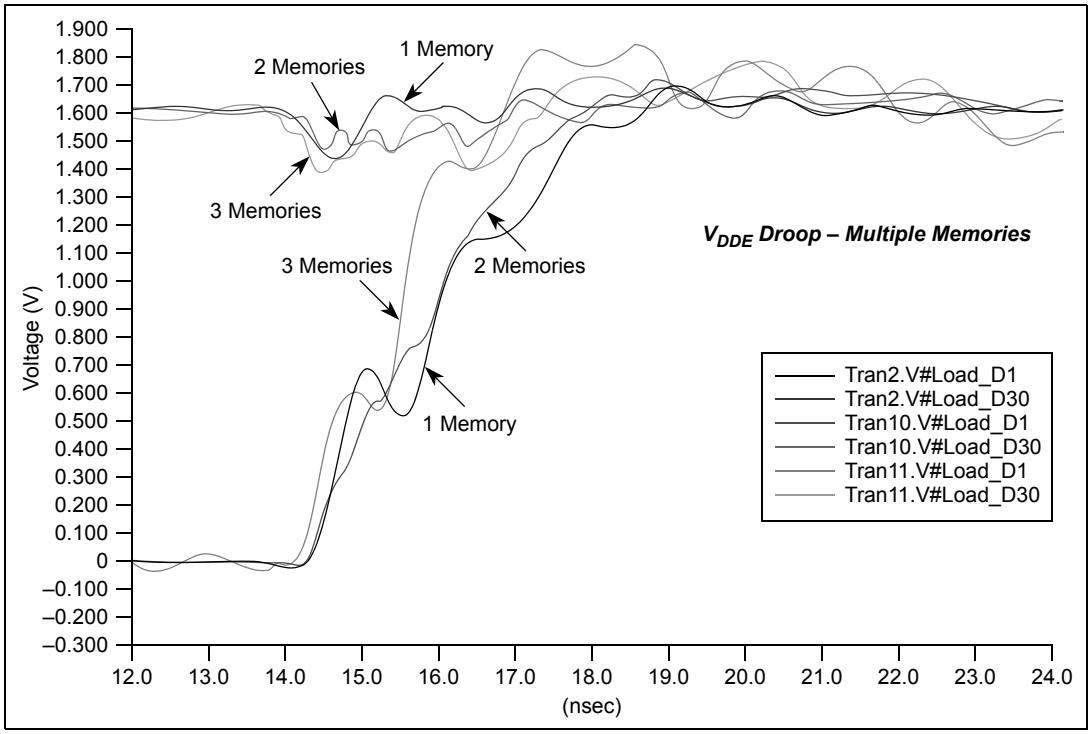


Figure 17. Number of Memories

B.9 Routing Impedance

Figure 18 shows the difference in signal waveform and VDDE droop when driving each of a 33 Ω, 75 Ω, and 150 Ω transmission line. The best result occurs when using the 150 Ω transmission line. The 150 Ω characteristic impedance gives the best result because it is the closest match to the driver impedance. In this simulation, the driver pull-up impedance is approximately 150 Ω. Therefore, when a routing impedance of 150 Ω is used, there is a very good impedance match between the driver and the transmission line. This results in a critically damped circuit. When a routing impedance of 75 Ω or 33 Ω is used, there is an impedance mismatch between the driver and the transmission line, and in this case the circuit is overdamped.

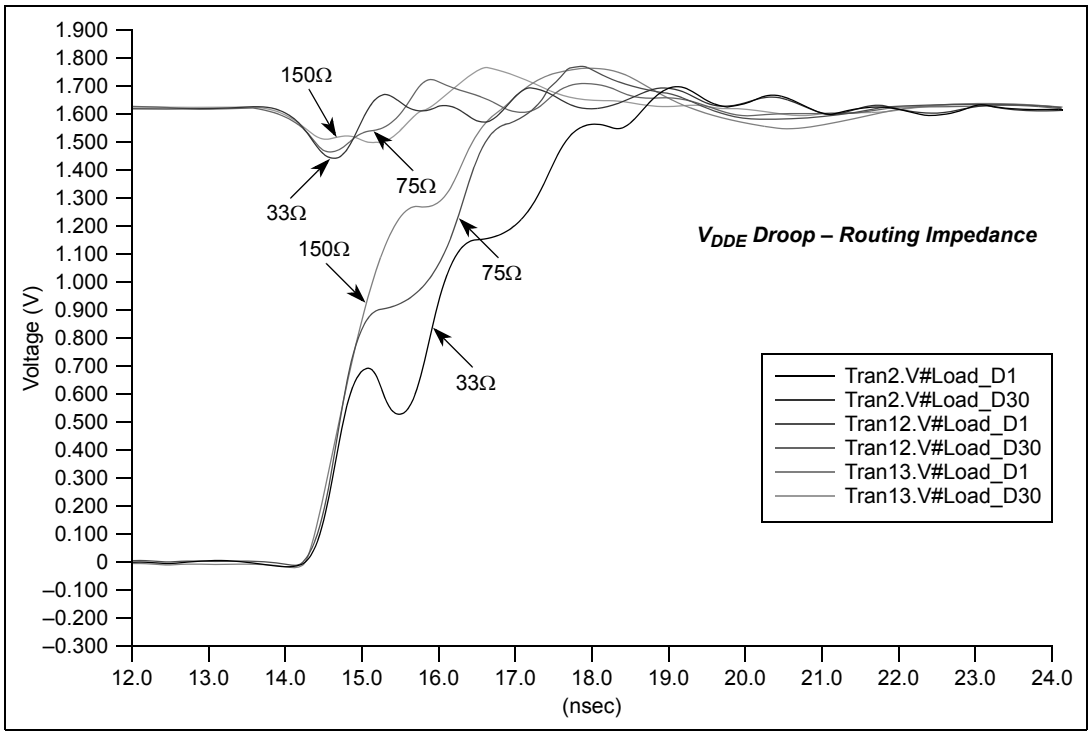


Figure 18. Routing Impedance

B.10 Example 1

Example 1 is intended to represent a poorly designed application board. In this example, the board is poorly designed because the drive mode does not match the load, the routing impedance does not match the driver impedance, and the decoupling is not good.

Since the load is one memory, the drive mode 00 should have been used, but instead the drive mode 10 was selected and thus the pad is overdriving the load. For the drive mode 10 and a VDDE of 3.6V, the driver pull-up impedance is approximately 20 Ω; however, a board routing impedance of 150 Ω was used. Therefore, there is a large impedance mismatch between the driver and the transmission line. Furthermore, the decoupling is considered poor for the same reasons described in section Section B.5, “Decoupling Models” when discussing the bad decoupling model.

The simulation data for this poorly designed application board is presented in Figure 19. The overshoot is 46% and the VDDE droop is 70%. False switching is likely to occur with such a large amount of VDDE droop. Furthermore, the signal valid time will be pushed out due to the significant ringing on the switching line.

In this example, the poorly designed application board could be fixed by selecting the drive mode 00 and improving the decoupling. Also, since the driver pull-up impedance for the drive mode 00 with a VDDE of 3.6V is around 60 Ω, the board routing impedance should be changed to 60 Ω.

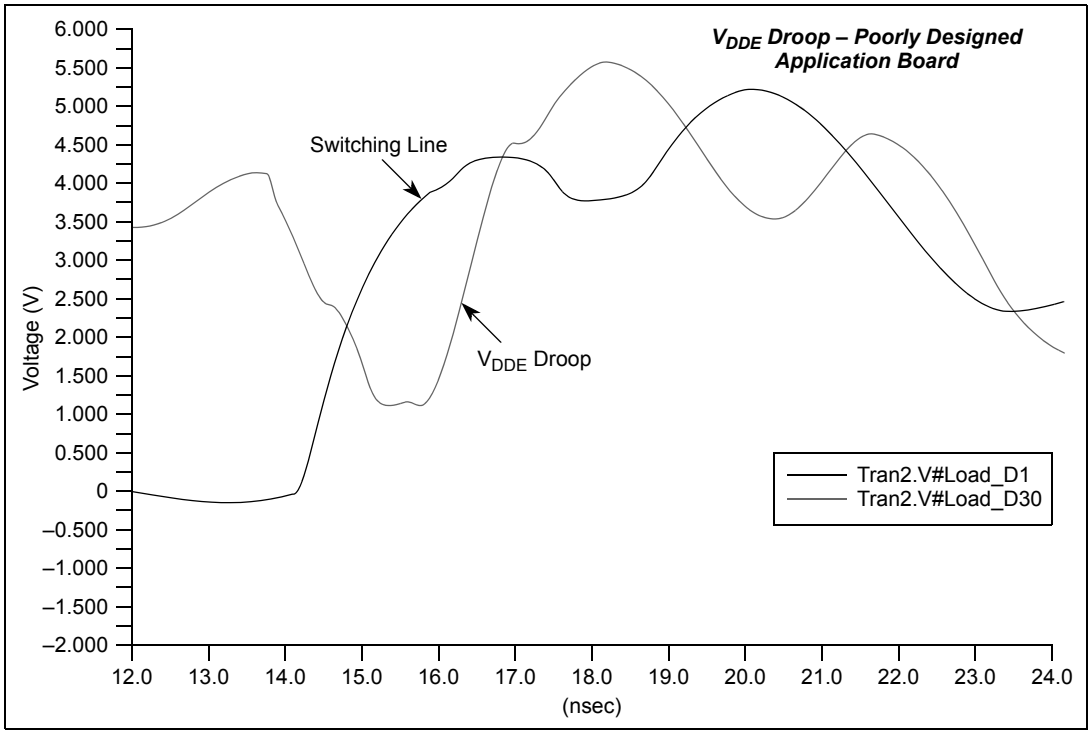


Figure 19. Example 1

B.11 Example 2

Example 2 is intended to represent a poorly designed evaluation board. In this example, the board is poorly designed because the drive mode does not match the load and the routing impedance does not match the driver impedance. Because there are three memories on this board, the drive mode 10 should have been used, but instead the drive mode 11 was selected and thus the pad is overdriving the load. The driver pull-up impedance for the drive mode 11 with VDDE of 3.6V is approximately 10 Ω; however, the board routing impedance is 75 Ω.

Figure 20 shows the simulation data for the poorly designed evaluation board. The overshoot is 86% and the ringing is very bad. The VDDE droop is about 36%, which could potentially cause false switching, but it is unlikely. However, the signal valid time for the switching line will need to get significantly pushed out in order to wait for the ringing to settle.

In this example, the poorly designed evaluation board could be fixed by selecting the drive mode 10 instead of the drive mode 11. Furthermore, the driver pull-up impedance for the drive mode 10 with VDDE of 3.6V is approximately 20 Ω. Therefore, the board routing impedance should also be 20 Ω, or alternatively, termination resistors should be used such that $R_T = Z_0 - Z_S$. For example, if the routing impedance is 75 Ω and Z_S is 20 Ω, then a 55 Ω termination resistor should be used. Additionally, the board decoupling, although good, could be further improved if embedded decoupling capacitors were used instead of discrete surface mount decoupling capacitor components.

Often it will make sense to use embedded decoupling capacitors on an evaluation board even if they are not used on the application board.

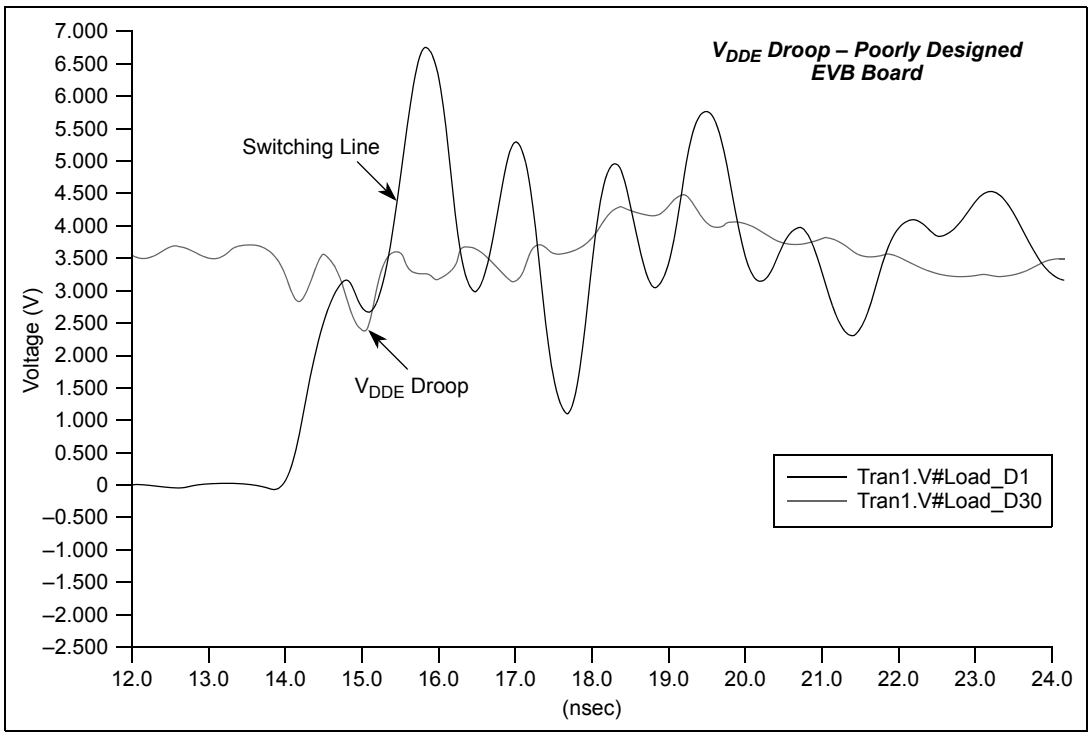


Figure 20. Example 2

Appendix C: CLKOUT Simulations

Simulations were performed in order to evaluate the signal integrity performance of the CLKOUT circuit. For these simulations, a transistor based model was used to model the pad_fc that is the pad type used for CLKOUT. The CLKOUT pad is supplied by VDDE. However, the CLKOUT VDDE is not the same as the external bus VDDE. For example, on the MPC5554, CLKOUT uses VDDE5 and the external bus uses VDDE2. For the rest of this section, assume that VDDE is the CLKOUT supply. The CLKOUT circuit model also included the on-chip capacitance that is connected to VDDE. The amount of the on-chip capacitance connected to the CLKOUT supply is approximately 600 pF. The package model was extracted using a tool called Momentum. The board power supply model for the CLKOUT supply was developed by assuming that there would be one 10 nF capacitor for decoupling. The CLKOUT signal routing on the board was modeled by using transmission lines and the devices to which CLKOUT is connected were modeled as a 7 nH series inductor (models package inductance) with a 7 pF load capacitor (models gate on input device). The model of the receiver device also included diodes from the pad to both power and ground meant to model expected input protection devices normally used on memory devices. Figure 21 shows a block diagram of the model used for the CLKOUT simulations.

For the CLKOUT simulations, there is only one pad switching, and therefore VDDE droop and ground bounce are not issues. However, ringing on the CLKOUT signal is potentially a significant issue. There are five main variables that affect the ringing on CLKOUT and they are:

1. The number of devices connected to CLKOUT
2. The characteristic impedance of the board routing for the CLKOUT signal
3. The use of a termination resistor on CLKOUT
4. Decoupling of the CLKOUT supply
5. The drive mode selected

Table 5 describes the simulations that were performed.

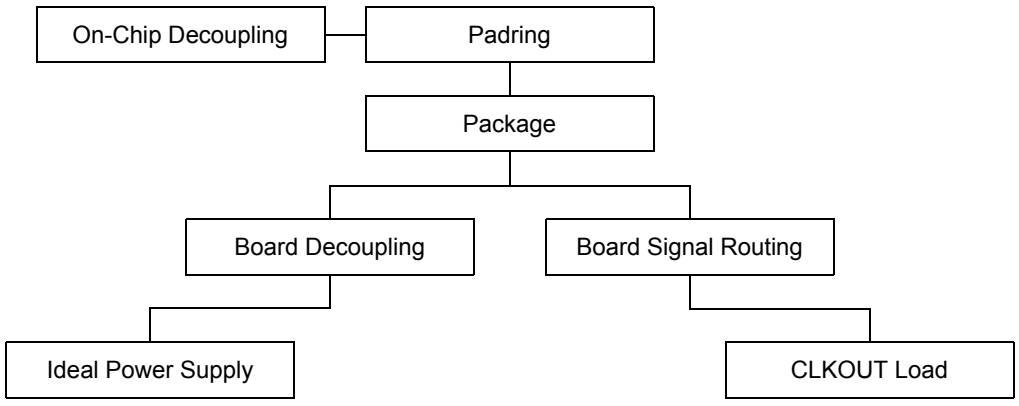


Figure 21. Block Diagram of CLKOUT Model

Table 5. CLKOUT Simulation Variables

Variable Number	Effect Studied	Drive Mode	Number of Memories	Characteristic Impedance (Z_0)	Termination Resistor (R_T)	Board Decoupling	On-chip Decoupling
1	Intended use for driving 1, 2, and 3 memory devices with proper matching of drive mode and Z_0	00, 01, 10	1, 2, 3	78Ω, 41Ω, 25Ω	0Ω	10nF with good connection	600pF
2	Z_0 effect	00	1	150Ω, 80Ω, 33Ω	0Ω	10nF with good connection	600pF
3	R_T effect	00	1	150Ω	100Ω, 72Ω, 40Ω, 20Ω, 0Ω	10nF with good connection	600pF
4	Board Decoupling effect	10	3	75Ω	0Ω	10nF with good connection, 10nF with bad connection, without 10nF cap	0pF
5	On-chip Decoupling effect	10	3	75Ω	0Ω	10nF with good connection, 10nF with bad connection, without 10nF cap	600pF
6	Overdriving effect	00, 01, 10, 11	1	150Ω	0Ω	10nF with good connection	600pF

C.1 Intended Use for Driving 1, 2, and 3 Memory Devices with Proper Matching of Drive Mode and Z_0

The simulation data in Figure 22 shows three switching waveforms of the signal at the receiver input node. The waveform for one memory has very good signal quality and a rise time of 1.66 ns. The drive mode 00 was used to drive the one memory. The average driver impedance for drive mode 00 with VDDE of 2.5V is 79.5 Ω (see Appendix D, ": Driver Impedance"); therefore, a Z_0 of 78 Ω was used in order to ensure an impedance match between the driver and the transmission line.

The waveform for the two memory case shows ringing, however, the signal quality is still acceptable for normal operation. The drive mode 01 was used to drive the two memory load. The rise time is approximately 1.76 ns. A Z_0 of 41 Ω was used because the average driver impedance for drive mode 01 with a VDDE of 2.5V is 40 Ω. For the three memory case, the drive mode 10 was used and Z_0 was made 25 Ω in order to impedance match.

The three memory waveform also has acceptable signal quality despite its ringing. The signal rise time for the three memory case was 1.88ns.

With proper matching of drive mode and Z_0, acceptable signal quality can be achieved for one, two, or three memory loads. The rise times for each of the three cases discussed are all approximately the same.

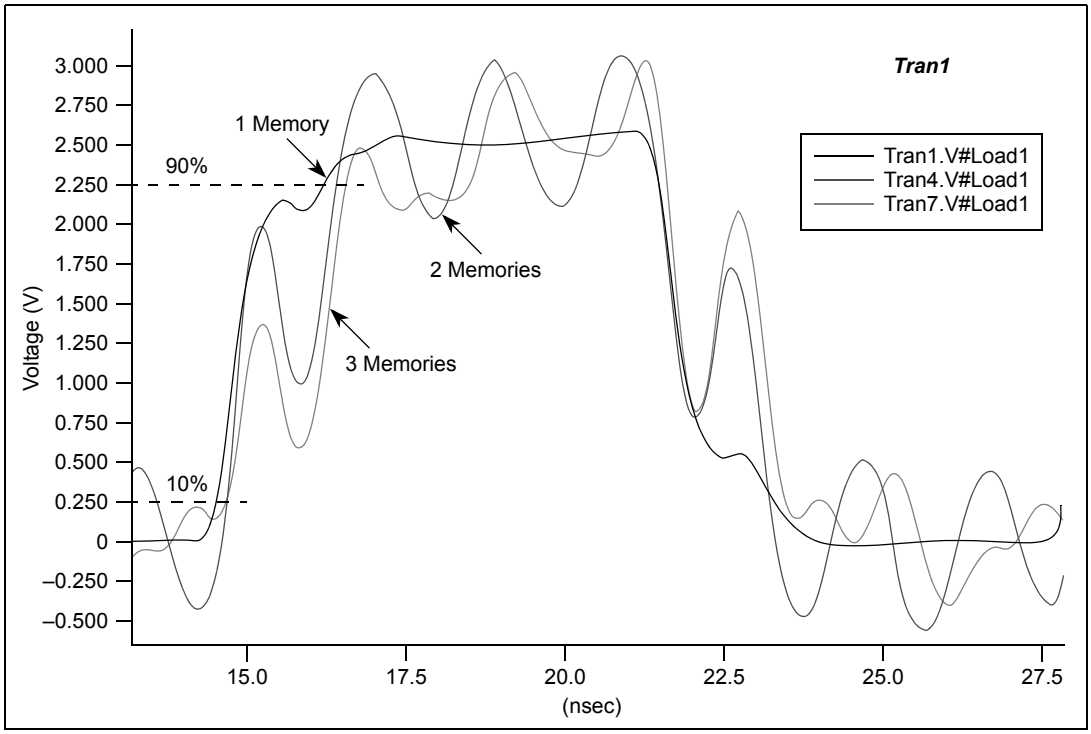


Figure 22. Intended Use for Driving 1, 2, and 3 Memory Devices with Proper Matching of Drive Mode and Z_0

C.2 Z_0 Effect

Another important variable that affects the signal integrity of the CLKOUT signal in a MPC5500-based system is the characteristic impedance (Z_0) of the board routing trace. Ideally, the Z_0 of the board trace should be equal to the driver impedance (Z_S). If Z_0 is set equal to Z_S, then the waveform will not have any reflections caused by an impedance mismatch between the driver and the transmission line and the line is said to be critically damped. The waveforms in Figure 23 show the effect of different values of Z_0 when the driver is driving one memory with the drive mode 00 selected. In this case the average driver impedance is 79.5 Ω (see Appendix D, ": Driver Impedance") and therefore the line is critically damped when a Z_0 of 80Ω is used. When Z_0 is less than Z_S, then the line is overdamped and the signal slows down as is shown by the increased rise time in the 33Ω case. When Z_0 is greater than Z_S, the line is underdamped and overshoot results as is observed in the 150Ω simulation.

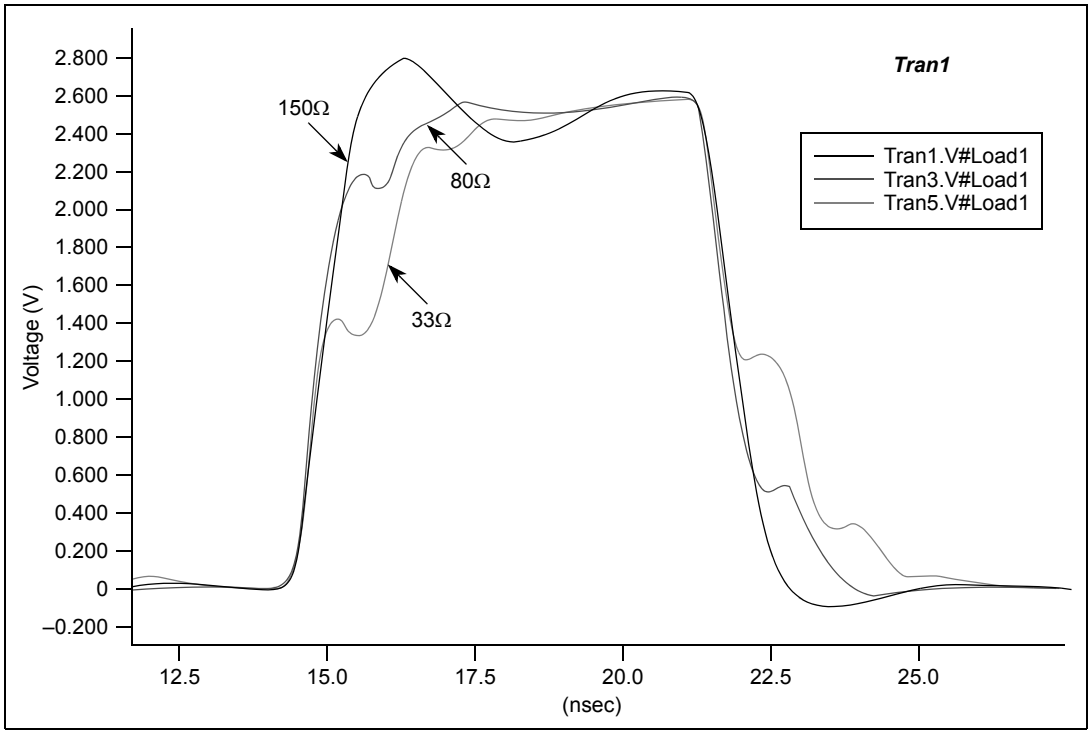


Figure 23. Z_0 Effect

C.3 R_T Effect

When Z_S is smaller than Z_0, the line is underdamped and a termination resistor (R_T) can be used to make the line critically damped. Figure 24 presents switching waveforms at the receiver when various values of R_T are used. In this simulation, the drive mode 00 is selected and the driver is driving one memory. The average driver impedance in this case is 79.5 Ω (see Appendix D, ": Driver Impedance") and a transmission line with a characteristic impedance of 150 Ω was used. Since Z_S is smaller than Z_0, the line is underdamped and overshoot occurs as can be seen in the waveform where R_T is 0 Ω. In order to make the line critically damped, the value of R_T must be equal to Z_0 minus Z_S which in this case would be 70.5 Ω. The 72 Ω waveform shows a very smooth switching signal as should occur when the line is

critically damped. Although the 20 Ω and 40 Ω cases do not provide enough resistance to critically damp the line, they do help reduce the overshoot amplitude nonetheless. Also, when a larger than needed value of R_T is used, the line will become overdamped, as can be seen in the 100 Ω waveform. It should be noted that in all cases, adding series termination resistance will slow down the signal transition.

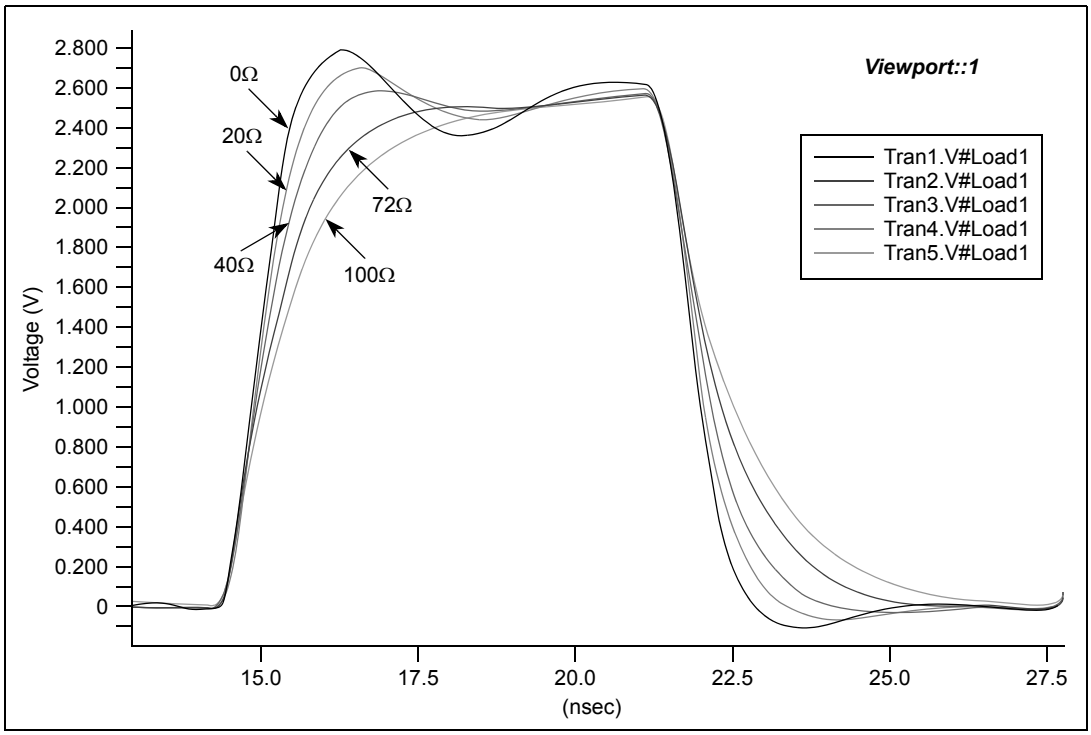


Figure 24. R_T Effect

C.4 Board Decoupling Effect

Figure 25 shows the effect of various board decoupling strategies. The 600 pF on-chip capacitance was removed for these simulations in order to highlight the impact of the board decoupling. The drive mode 10 was selected for these simulations, and the driver is driving three memory loads. There are three board decoupling cases examined. The first case shows the effect of no board decoupling, and in this case the signal quality is very poor. The second case shows the impact of using one 10nF capacitor, but the capacitor has a bad connection to the micro controller supply ball. In this context, a bad connection refers to a highly inductive connection. Adding the 10 nF capacitor even with a bad connection is a definite improvement over no decoupling. The final case shows the improvement gained when the connection to the 10 nF capacitor is good. Two conclusions can be drawn from this data:

1. Better board decoupling will improve signal quality.
2. Better board decoupling will improve signal transition times.

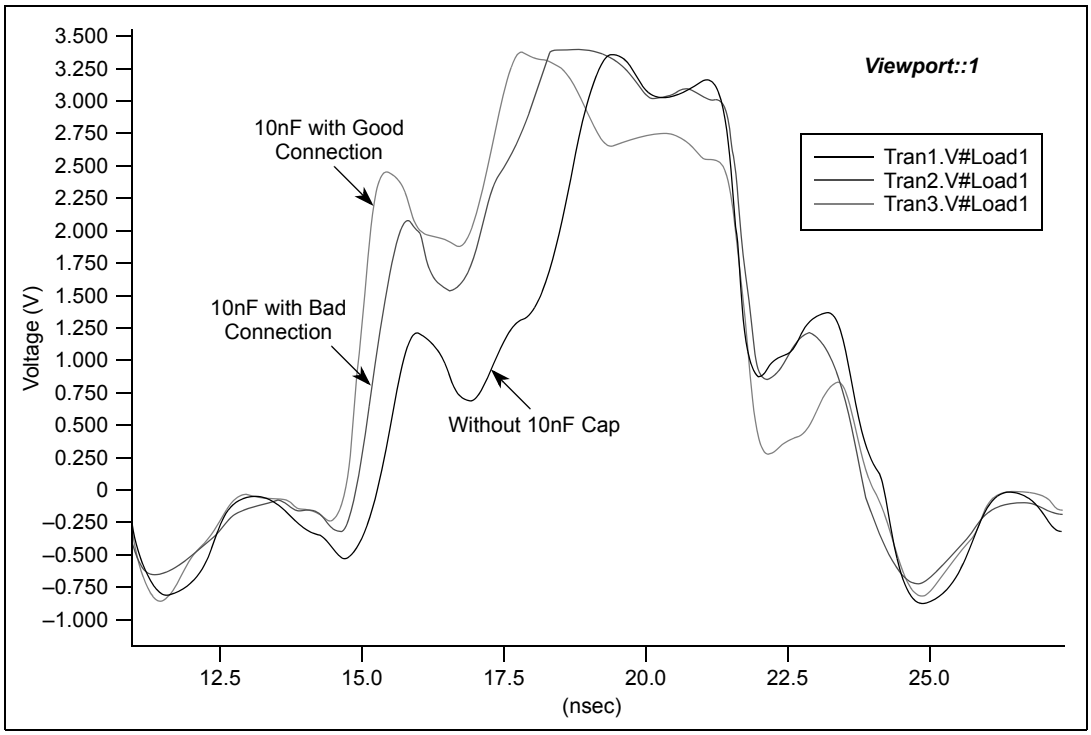


Figure 25. Board Decoupling Effect

5.4 On-chip Decoupling Effect

The simulation data in Figure 26 highlights the benefit of the on-chip capacitance and also shows the relative importance of board decoupling when on-chip decoupling is present. The 600 pF on-chip decoupling is included for these simulations. The simulations use the drive mode 10 driving 3 memory loads. Therefore, the on-chip decoupling capacitance (at 600 pF) is 20 times larger than the load (at 30 pF). Since the on-chip capacitance is 20X the load capacitance, the relative importance of the board decoupling is anticipated to be small. The three waveforms for the three board decoupling schemes all look

approximately the same, which is further evidence that the board decoupling is of reduced importance when large amounts of on-chip decoupling is used.

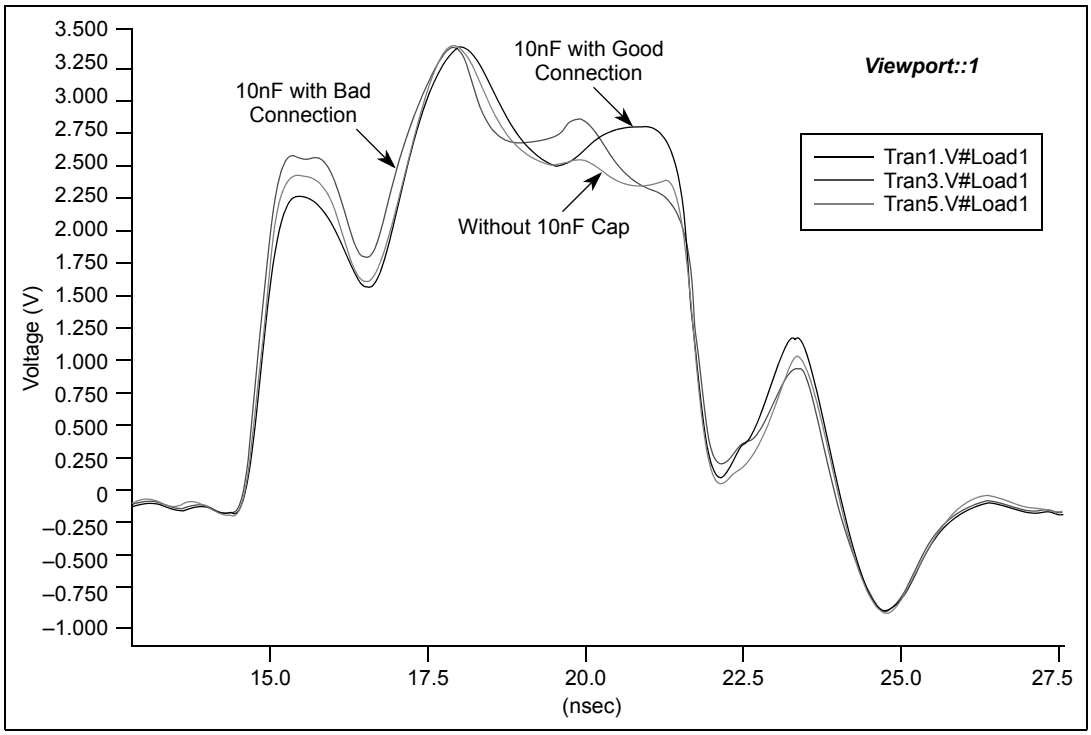


Figure 26. On-chip Decoupling Effect

C.5 Overdriving Effect

The final effect to be discussed for the CLKOUT simulations is the importance of selecting the intended drive mode based on the load. Figure 27 shows waveforms for each of the drive modes all driving a one memory load. When driving a one memory load, the drive mode 00 should be selected and indeed the 00 waveform shows good signal quality. However, when any of the other three drives modes are selected, the load is overdriven and massive overshoot and ringing results. The overshoot is clamped by the input protection diodes on the receiver. Similarly, the undershoot is also clamped by the receiver's input protection diodes. Although the initial overshoot is not a problem because it is clamped, the large amplitude ringing that follows the initial overshoot can cause double clocking.

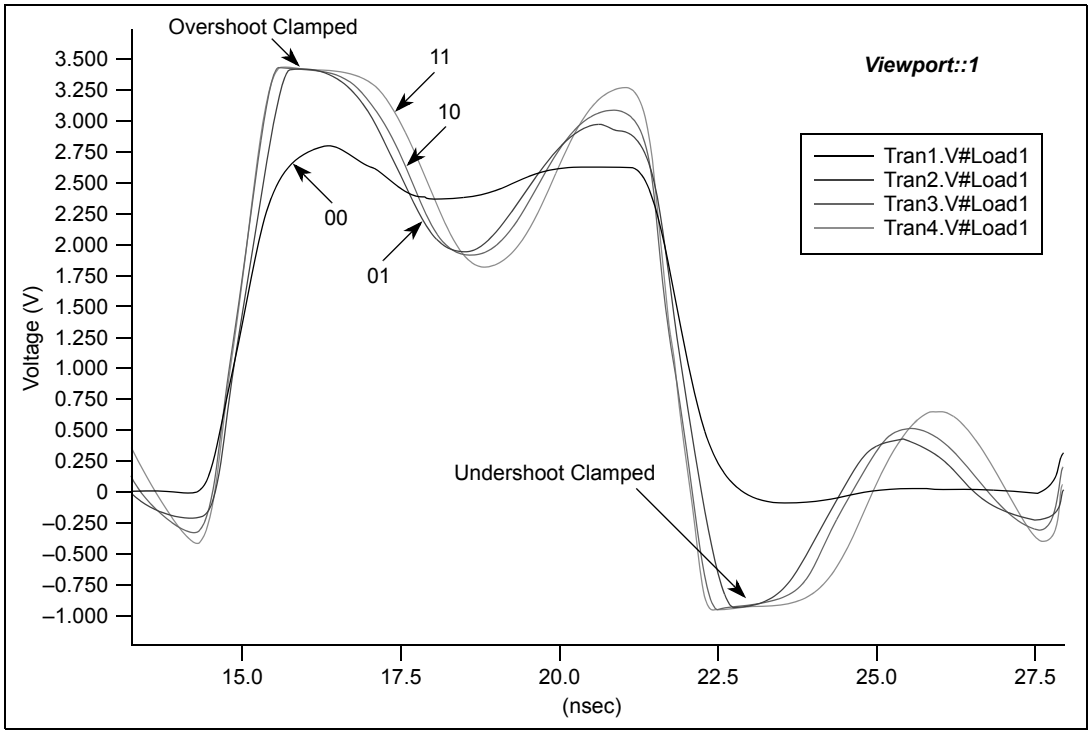


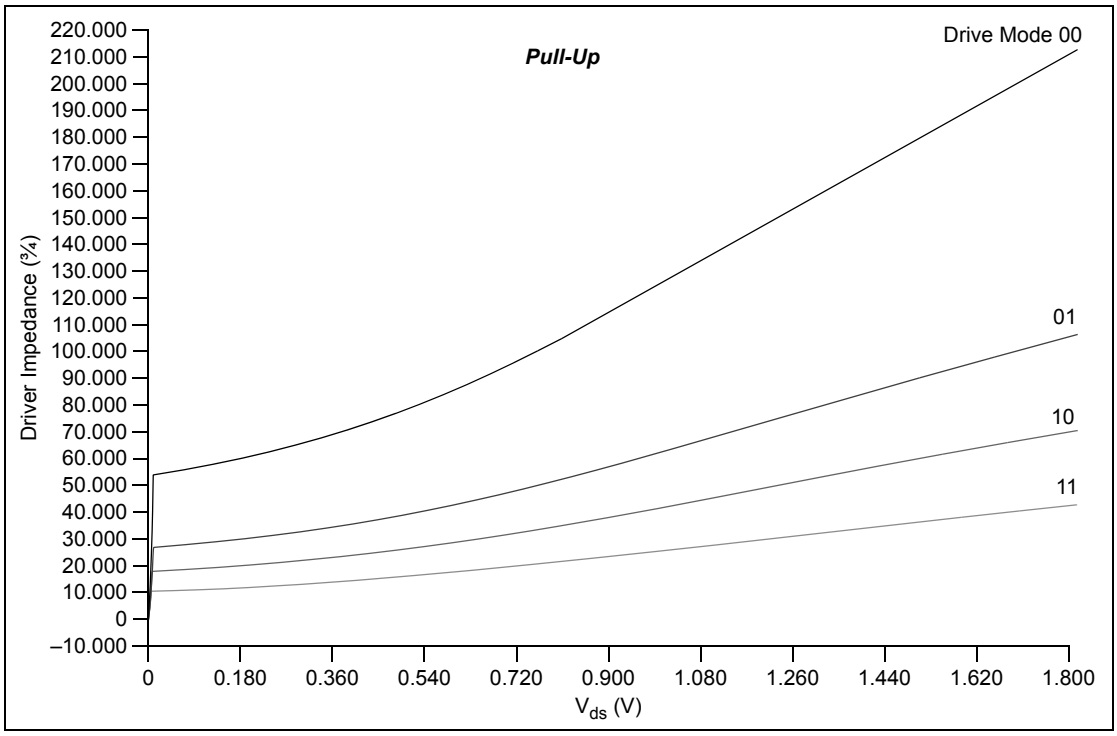
Figure 27. Overdriving Effect

Appendix D: Driver Impedance

This appendix contains simulation data for the pull-up and pull-down impedance of the fast pad (pad type = pad_fc). The fast pad can have a VDDE from 1.62V to 3.6V. Therefore, pull-up and pull-down impedance curves are presented for three different VDDE settings, namely 1.8V, 2.5V, and 3.3V. The impedance of MOSFET devices varies over process, voltage, and temperature. The impedance of a MOSFET device also varies as a function of the drain-to-source voltage (V_{ds}), which means that the impedance changes as the signal is switching. Nevertheless, in order to do impedance matching of the driver to the load it is necessary to determine one impedance value for the driver that will be called the average driver impedance. It is necessary to determine the average driver impedance, because the board routing can only have one target impedance value and likewise the termination resistor (if used) can also only have one target value. Therefore, only one value for the driver impedance can be considered. If impedance matching is done using the average driver impedance, then the driver will be roughly matched to the load under all the various operating conditions. The average driver impedance is calculated by taking the average of the pull-up impedance and the pull-down impedance. The pull-up and pull-down impedances are selected at the point where V_{ds} is equal to VDDE/2. Table 6 shows the average driver impedance for each of the drive modes.

Table 6. Driver Impedance

Drive Mode	VDDE	Pullup Impedance (Ω)	Pulldown Impedance (Ω)	Average Driver Impedance (Ω)
00	1.8V	115	76	95.5
01	1.8V	57	38	47.5
10	1.8V	38	25	31.5
11	1.8V	23	15	19
00	2.5V	73	86	79.5
01	2.5V	37	43	40
10	2.5V	24	29	26.5
11	2.5V	15	17	16
00	3.3V	56	100	78
01	3.3V	28	50	39
10	3.3V	19	34	26.5
11	3.3V	11	20	15.5



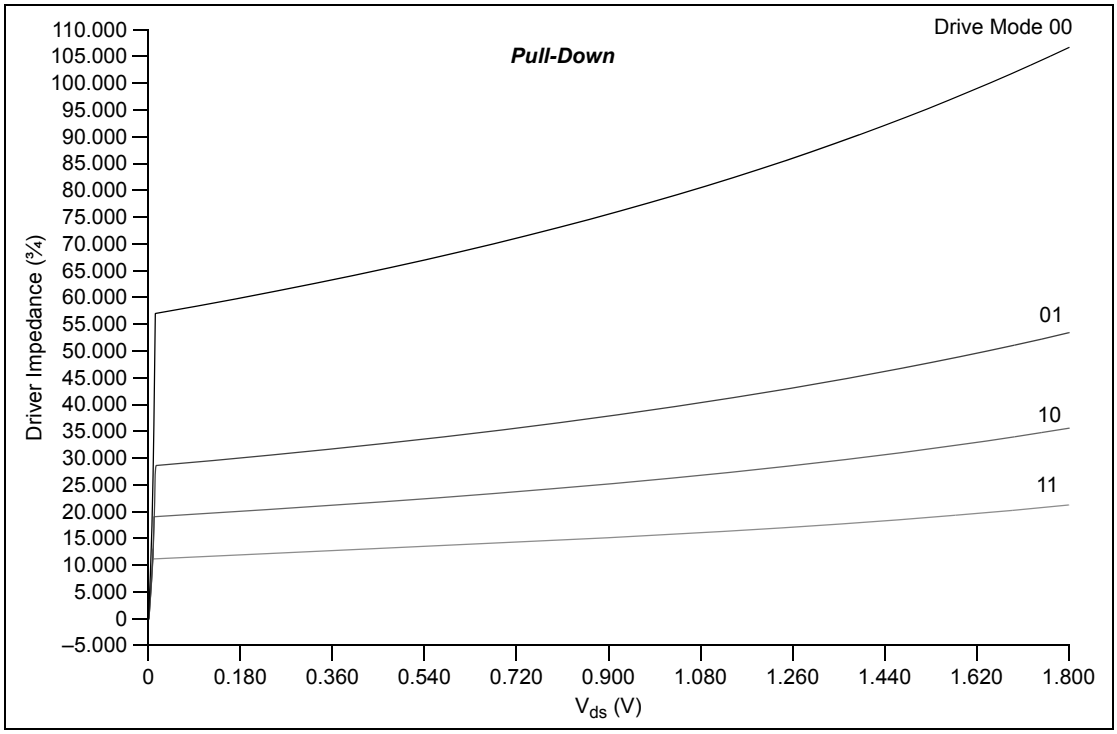
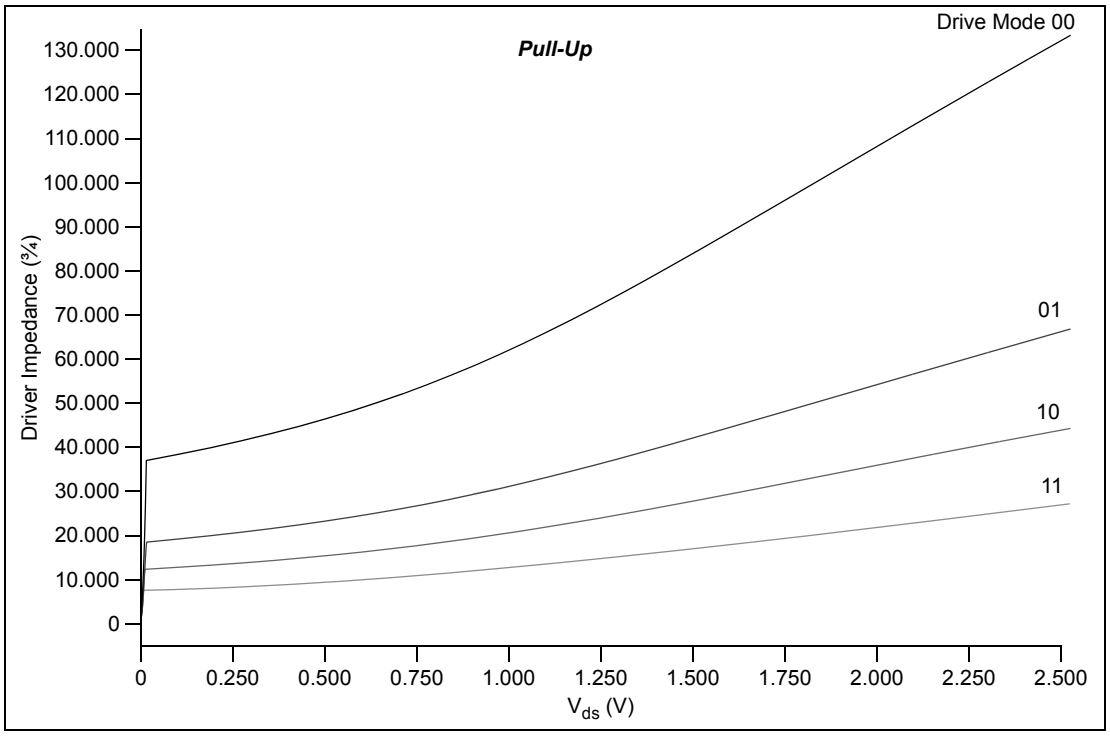


Figure 28. Driver Impedance with VDDE = 1.8V



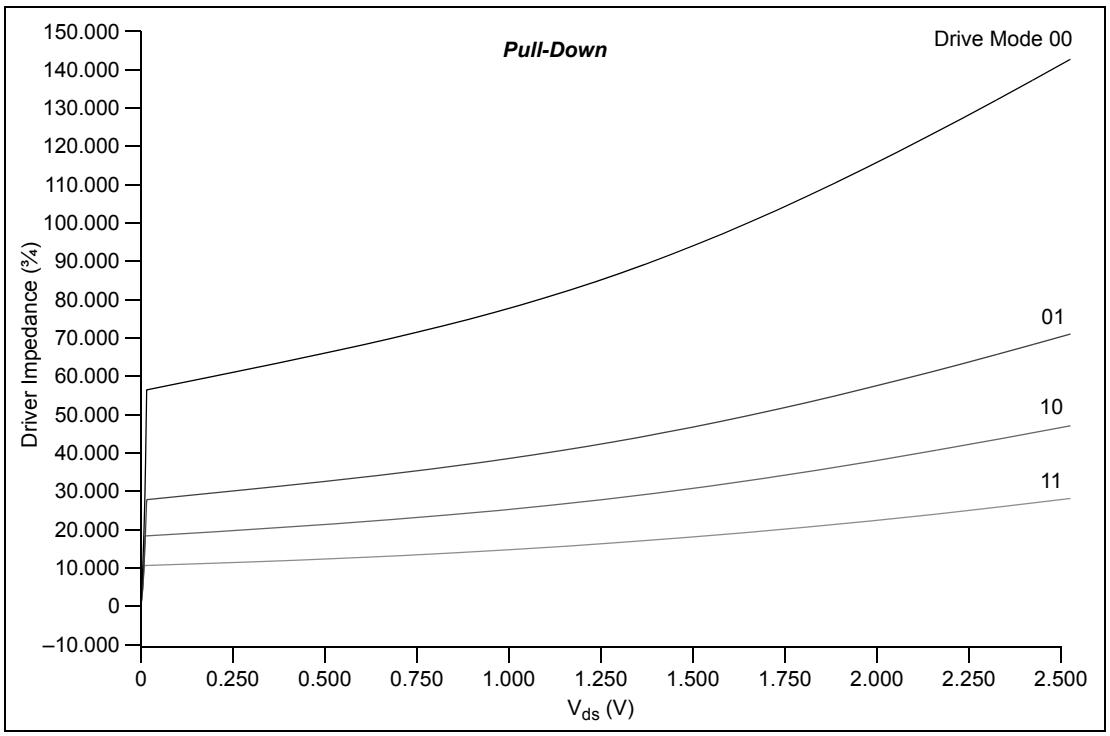
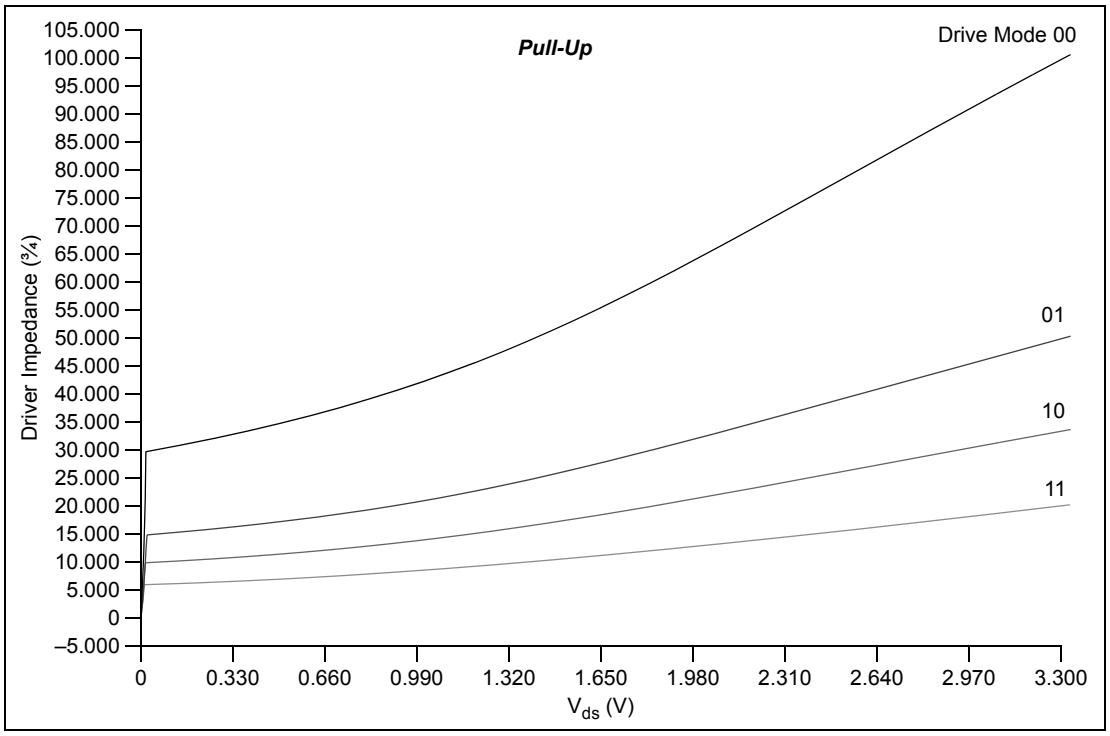


Figure 29. Driver Impedance with VDDE = 2.5V



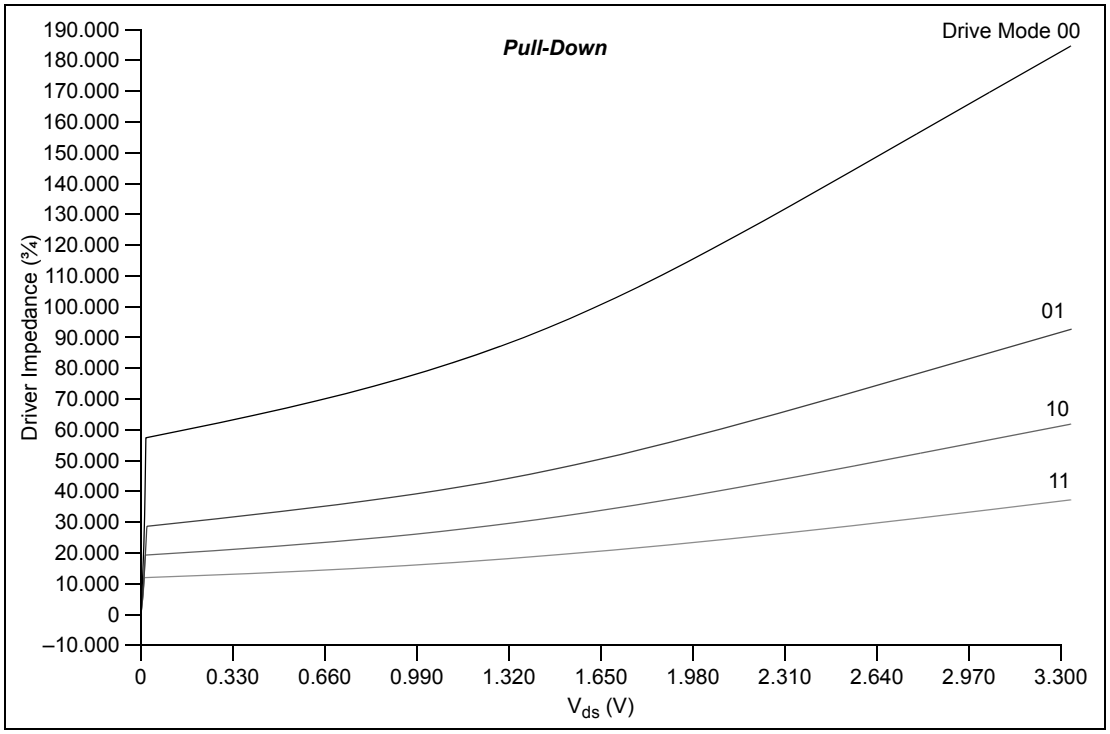


Figure 30. Driver Impedance with VDDE = 3.3V

Appendix E: Derated Data Bus Simulations

Data bus simulations with reduced drive mode were performed in order to provide derated rise and fall times. Three situations were evaluated. First, the two memory load case was considered. Normally, the drive mode 01 should be selected in order to ensure specified rise and fall times. However, if slower rise and fall times are acceptable, then the drive mode can be reduced to drive mode 00. Table 7 shows the rise and fall times when driving two memories with drive mode 00.

Table 7. Derating for Drive Mode 00 Driving 2 Memories

VDDE (V)	Rise (ns)	Fall (ns)
1.8	10.82	7.45
2.5	6.27	6.72
3.3	4.77	9.29

The second and third situations simulated were for a three memory load. Normally, drive mode 10 should be used to drive three memories and ensure the specified rise and fall times. However, if slower rise and fall times are acceptable, then the drive mode can be reduced to either drive mode 00 or drive mode 01. Table 8 shows the rise and fall times when the drive mode 00 is used to drive three memories, and Table 9 shows the rise and fall times when drive mode 01 is used to drive three memories.

Table 8. Derating for Drive Mode 00 Driving 3 Memories

VDDE (V)	Rise (ns)	Fall (ns)
1.8	15.74	11.80
2.5	9.70	12.35
3.3	7.09	14.19

Table 9. Derating for Drive Mode 01 Driving 3 Memories

VDDE (V)	Rise (ns)	Fall (ns)
1.8	7.63	4.90
2.5	4.72	5.21
3.3	3.25	7.06

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