Freescale Semiconductor
Application Note

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EMC Guidelines for MPC5500-Based Systems

by: Stevan Dobrasevic
TECD Design Engineering

This application note describes recommended EMC guidelines for reducing electromagnetic emissions in MPC5500-based systems.

Table of Contents

1 Disclaimers

This document contains information on a new product. Specifications and information herein are subject to change without notice.

2 Introduction

An increasingly important consideration in the design of embedded 32-bit systems is Electromagnetic Compatibility (EMC). EMC consists of four sub-groups: Radiated Emissions, Conducted Emissions, Radiated Susceptibility, and Conducted Susceptibility. This application note focuses on guidelines for reducing Radiated Emissions from MPC5500-based systems. These guidelines are not a complete set of all known EMC techniques, but rather they are some specific recommendations for MPC5500-based systems. This

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application note should be used in conjunction with other more general sources of EMC guidelines; many such sources are suggested Section 6, “References”.

In general, the MPC5500 family of MCUs have four primary sources of noise: CLKOUT, ENGCLK, V_{DD} power supply, and the external bus. This application note will focus on reducing emissions from the V_{DD} power supply. Application note AN2705 titled “Signal Integrity Considerations with MPC5500-based systems” provides guidelines for improving signal integrity and reducing emissions from the external bus.

To ensure EMC compliance for expanded mode applications, the guidelines from both application notes (AN2705 and AN2706) should be followed. For single chip applications with CLKOUT and ENGCLK disabled, the guidelines in this application note (AN2706) alone are sufficient.

Measurements have shown that emissions from the MPC5500 devices are lower than emissions from MPC500 devices. The MPC5500 devices have reduced emissions, because several EMC improvements were made to this family of devices.

The EMC improvements made to the MPC5500 devices include:

1. Increased on-chip decoupling capacitance
2. Reduced package inductance
3. FMPLL allows spread spectrum
4. More isolated power supplies
5. Gated clock feature on external bus and nexus
6. More on-chip memory means less need for external memory devices
7. Increased I/O drive strength selectability allows better matching to application load

Even though MPC5500 devices have reduced emissions, it is important to follow the board level guidelines to ensure system level EMC compliance.

3 Software Guidelines

The software guidelines presented in this section describe what to do in general terms. For actual implementation details, refer to the *MPC5500 Reference Manual*.

3.1 System Frequency

There are two important topics to address when determining the system frequency.

First, the system frequency should be selected such that it and its harmonics do not fall within “bands of interest,” such as the FM and TV bands. Avoiding the “bands of interest” will reduce the likelihood of interfering with communications in those bands.

Second, the MPC5500 uses an FMPLL. The FMPLL has selectable modulation up to 2%. The FMPLL should be configured for 2% modulation for best EMC performance; however, system timing requirements may dictate a lower setting of 1% or 0.5%. Modulating the system frequency spreads energy among more receiver bands during an emissions measurement; this results in lower measured emissions.

3.2 I/O Configuration

In general, the I/O should be configured such that they drive as slow as possible while still ensuring performance requirements. Driving the I/O stronger than necessary creates additional emissions. Each I/O type has multiple drive strengths options. Use the weakest drive strength required for the application load and application timing requirements.

The output buffer should be disabled for any I/O that is not needed.

If possible, the gated clock feature for the external bus and the nexus port should be enabled. The gated clock feature turns on the clock only when it is needed and turns it off at all other times. Since the clock is not running all the time during an emissions test, less average emissions are measured.

3.3 Module Configuration

The individual modules on MPC5500 devices can be disabled. Disabling modules results in lower current drawn through the supply, which reduces emissions. Any unused module should be disabled.

4 Hardware Guidelines

4.1 V_{DD} Decoupling

This section provides guidelines for decoupling of the V_{DD} supply. For guidelines on decoupling of the VDDE2 (bus) and VDDE5 (CLKOUT) supplies, refer to AN2705. Recommendations for decoupling of the QADC supplies can be found in EB643. For decoupling suggestions concerning all other supplies, refer to the *MPC5500 Reference Manual*.

4.1.1 Capacitor Selection

The decoupling capacitor requirements for the V_{DD} supply are outlined in Figure 1.

Capacitor Value	Number of Capacitors Required	Suggested Package Size	Is Layout Critical?
10 nF	8	0306	Yes
100 nF	1	0612	No
10 µF[1]	1	7343-31	No

Figure 1. Decoupling Capacitor Requirements for the V_{DD} Supply

[1] Use 2.2 µF if internal VRC voltage regulator is used

The number of capacitors specified in Figure 1 is the minimum requirement. More capacitors are better. Three different capacitor values are used. The smallest capacitors, which have a value of 10 nF, are the high frequency decoupling capacitors. These capacitors should have a low Equivalent Series Inductance (ESL) package, such as the 0306 package. It is also important that the connection of these capacitors to the MPC5500 device is a low inductance connection; this is why the layout of these capacitors is critical. The

eight 10-nF capacitors should be placed near the corners of the MPC5500 device, two capacitors per corner. The layout of the 100-nF and 10-µF bulk decoupling capacitors is not critical.

4.1.2 Capacitor Layout

The layout and connection to the 10-nF decoupling capacitors is critical. The goal is to reduce the effective inductance from the MPC5500 device to the 10-nF capacitors.

Some guidelines for reducing the inductance are:

1. Place the capacitors as close as possible to the V_{DD} balls on the MPC5500 device.
2. Distribute the capacitors evenly around the MPC5500 device. The MPC5500 devices have V_{DD} balls in each of the four corners, so it is a good idea to place one-fourth of all the capacitors in each of the four corners. For example, if there are eight 10 nF capacitors, then two of them should be placed in each corner.
3. Use power planes or wide traces to connect from the MPC5500 device to the capacitor.
4. Use as many vias as possible in the connections from the MPC5500 device to the capacitors. For example, use at least two vias to connect the positive side of the capacitor to the power plane.

Some boards allow placement of components on both sides of the board, whereas other boards only allow placement of components on one side of the board. Use double sided component placement boards if possible.

Figure 2 shows an example layout for a double-sided component placement board. In this example, ten 10-nF capacitors are used and they are placed very close (~1 mm) to the V_{DD} balls and are distributed around each of the four corners. The MPC5500 device is mounted on the backside of the board; the vias from the MPC5500 balls can be seen in the figure and the V_{DD} vias are indicated. There are a total of fourteen V_{DD} vias. All capacitors in the figure are shown in gray.

There are a total of ten 10-nF capacitors, all of which are in the 0306 package. Two vias are used to connect each V_{DD} connection of the capacitor to the power plane. One via per ball is used to connect the MPC5500 device to the power plane. The total effective inductance from the die inside the MPC5500 device to the 10-nF capacitors is approximately 400 pH for this specific layout.

In addition to the ten 10 nF capacitors, there is also one 100-nF and one 10-µF capacitor. In this example, the 100-nF and 10-µF capacitors are located relatively close to the MPC5500 device and connect directly to the power plane. However, the connection to the 100-nF and 10-µF capacitors is not critical; higher inductance in these connections is acceptable. Therefore, the 100-nF and 10-µF capacitors can be moved further away from the MPC5500 device.

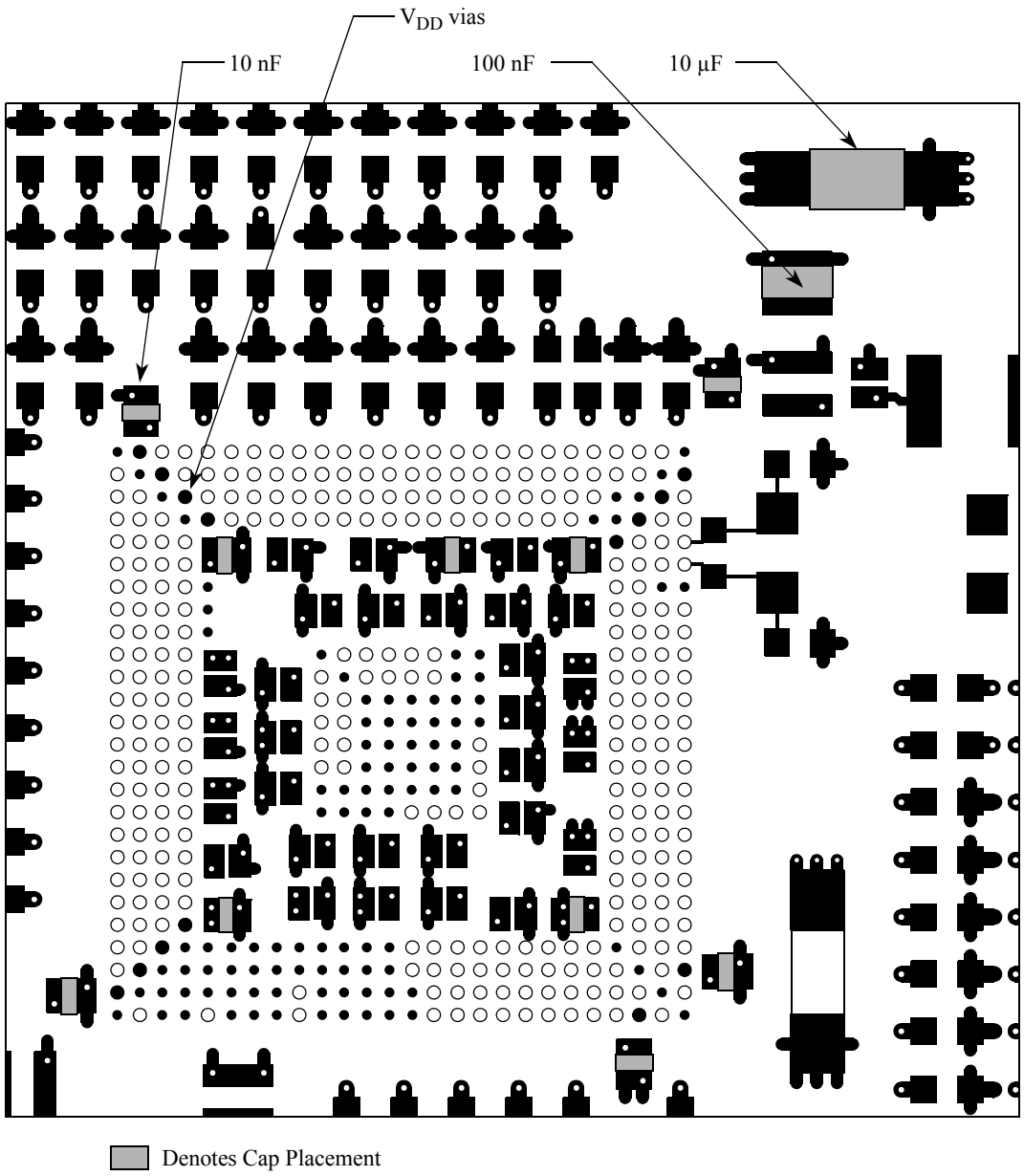

Figure 2. Example Capacitor Layout for a Double-Sided Component Placement Board

For single-sided component placement boards, the connection from the MPC5500 V_{DD} balls to the 10-nF decoupling capacitors will have typically two to three times the inductance compared to the double-sided component placement board. This may be acceptable depending on the overall application configuration and emissions target.

There are several ways to minimize the inductance in a single-sided component placement application. The 10-nF capacitors should be placed near the corners of the MPC5500 device where the V_{DD} balls are located. It is important to get the 10-nF caps as close as possible (within 4-5 mm) to the MPC5500 device. Connection of the V_{DD} balls on the MPC5500 device to the capacitors should ideally be made with a power plane. If a power plane is used, then the V_{DD} balls should be connected to the power plane with at

least one via per ball. Also, the V_{DD} connection from the power plane to the capacitor should be made with at least two vias. If a power plane is not available, then the connection from MPC5500 device to capacitor should be made with wide traces on the topside of the board.

4.1.3 Advanced Decoupling Techniques

4.1.3.1 Embedded Board Decoupling

When a power plane is placed on an adjacent layer to a ground plane, a metal-to-metal capacitor is formed. Embedded decoupling capacitors enhance this plane-to-plane capacitance by providing very thin dielectrics with high dielectric constants. Many manufacturers sell embedded decoupling capacitor laminates; one example is Dupont's Interra HK10 laminate which provides 2.2 nF per square inch. Using embedded decoupling capacitors reduces the need for discrete decoupling capacitors; however, in some cases, discrete decoupling capacitors may still provide an additional benefit even when embedded decoupling capacitors are used.

4.1.3.2 Determine Supply Impedance

The board power supply impedance is complex. It is very useful to be able to determine the supply impedance over a broad frequency range so that the impedance can be optimized for the particular application and serious resonance problems can be avoided. The supply impedance can be determined by simulation or measurement. Several board level tools are available for power supply analysis. Measurements can also be taken on actual boards using either an impedance analyzer or a network analyzer.

4.2 Grounding

Most microcontroller-based systems will partition different classes of circuits with isolated grounds. The isolated grounds are then connected together at a single point as shown in Figure 3. The different classes of circuits include digital, analog, high-current switching circuitry, I/O, and the main power supply.

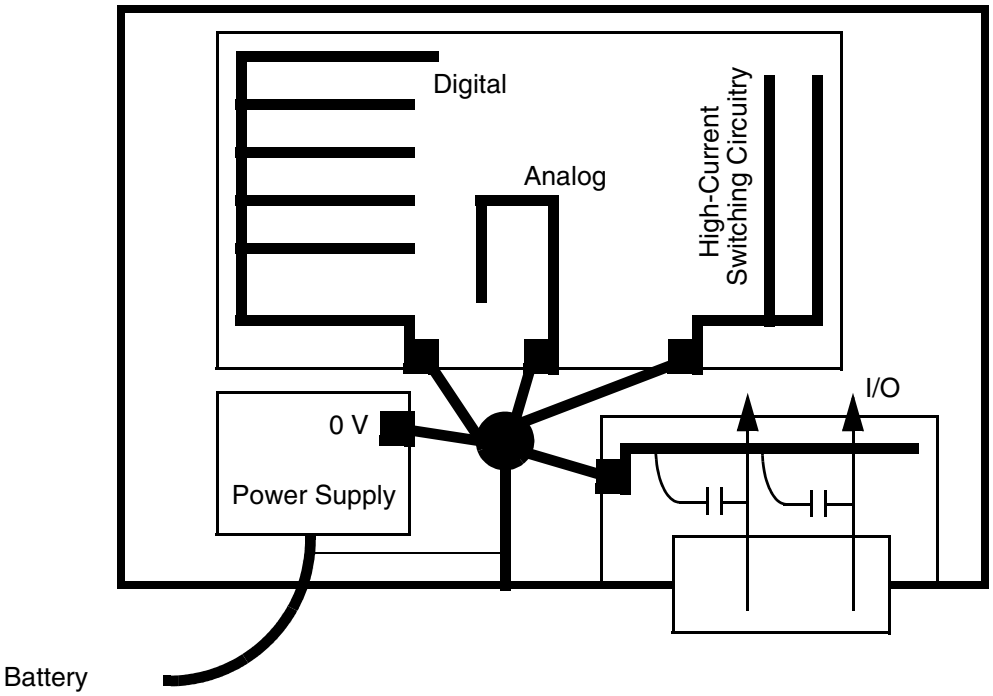

Figure 3. Typical MCU Application Grounding Example

4.3 Other Hardware Techniques

4.3.1 Layer Stack Up and Vias

Most MPC5500 family applications will require the use of a multi-layer board; four layer boards are the most common for single-chip applications, and six layer boards are normal for expanded mode applications. For multi-layer boards, dedicated power and ground planes should be used. An example of a good four-layer stack up is shown in Figure 4. The power plane is often a mixed voltage power plane.

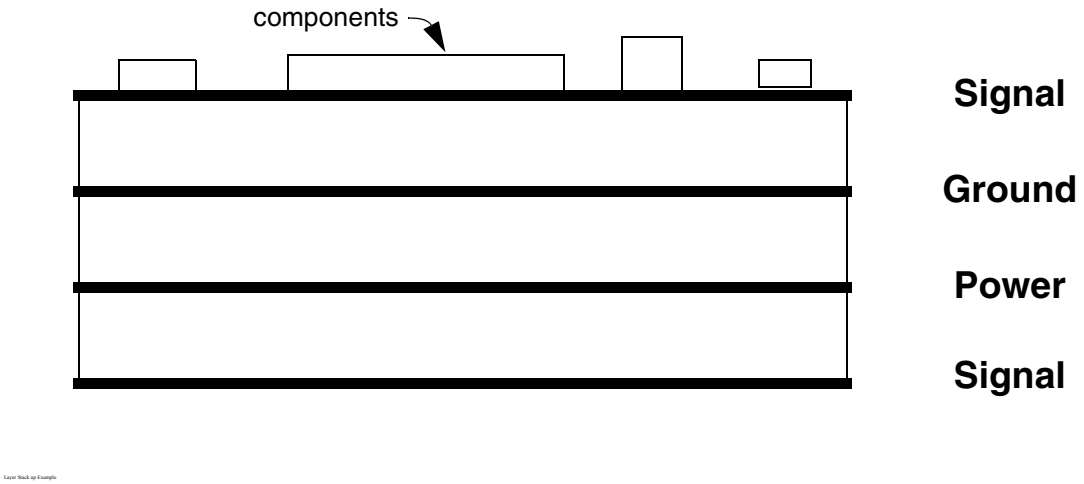

Figure 4. Four-Layer Stack Up Example

The use of many vias for power and ground connections is stressed throughout this document. However, care must be taken to avoid degradation of the power and ground planes by too many via holes obstructing the flow of current in the plane. A general rule of thumb is to not allow three via anti-pads to merge (see Figure 5). Also, vias should be staggered whenever possible because aligned vias create slots.

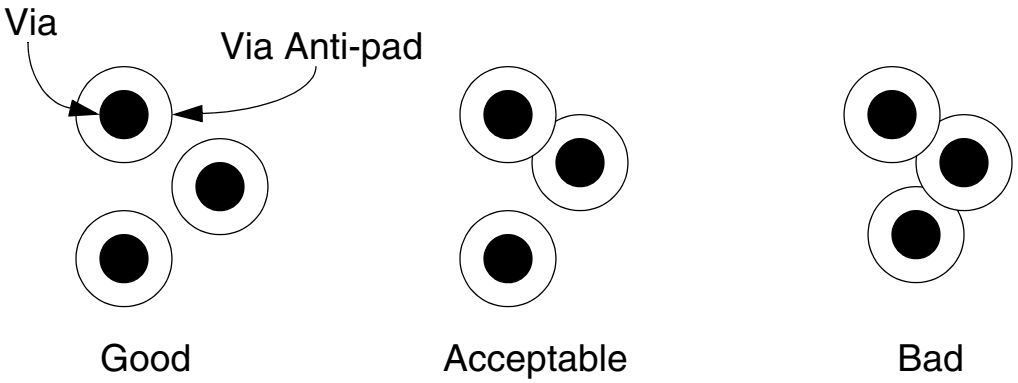

Figure 5. Via Example

4.3.2 Oscillator

The oscillator circuit consists of a bias resistor, the crystal, and two capacitors. The external bias resistor may not be needed because there is an internal bias resistor. However, it is recommended to leave room for an external bias resistor. The oscillator circuit provides a reference clock signal to the on-chip PLL. Use the lowest frequency crystal possible and set the multiplication factor bits to obtain the proper system operating frequency which is generated from the PLL. The oscillator circuit has currents flowing at the crystal's fundamental frequency. Also, if the oscillator is clipped, then higher order harmonics will be present as well. In order to minimize the amount of emissions generated from these currents, the oscillator circuit should be kept as compact as possible (see Figure 6). Also, VSSSYN should be connected directly

to the ground plane so that return currents can flow easily between VSSSYN and the two capacitors (C_x and C_y).

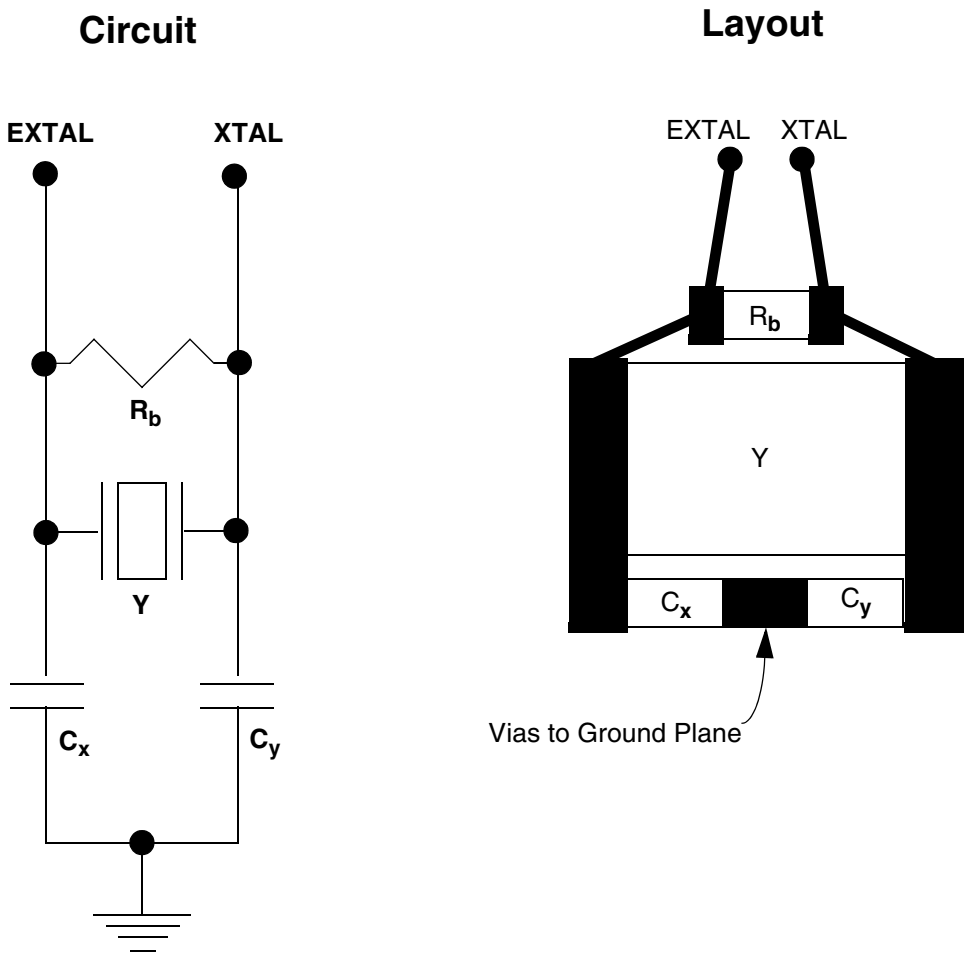

Figure 6. Oscillator CIrcuit and Layout

4.3.3 Micro-Island Approach

The micro-island approach to decoupling and grounding is the premier solution for high-speed digital noise isolation, and as such it tends to cost more to implement than standard decoupling and grounding. The micro-island technique aggressively seeks to isolate all high-speed digital noise to a micro-island instead of allowing it to propagate throughout the entire system. All high-speed digital components such as the microcontroller, crystal, and memory are grouped together in an isolated island, and a moat surrounds the entire island. There are isolated power and ground islands which are also surrounded by moats; the ground island extends out further than the power island. Power entry to the micro-island is filtered using a three-terminal EMI chip capacitor or a Π-filter consisting of a low-Q inductor or ferrite bead in combination with some capacitors. The micro-island is decoupled with 22 0306 style, 10-nF

decoupling capacitors that are evenly distributed throughout the micro-island area. Any signal line leaving the micro-island area is filtered using resistors or ferrite beads. Figure 7 contains additional details.

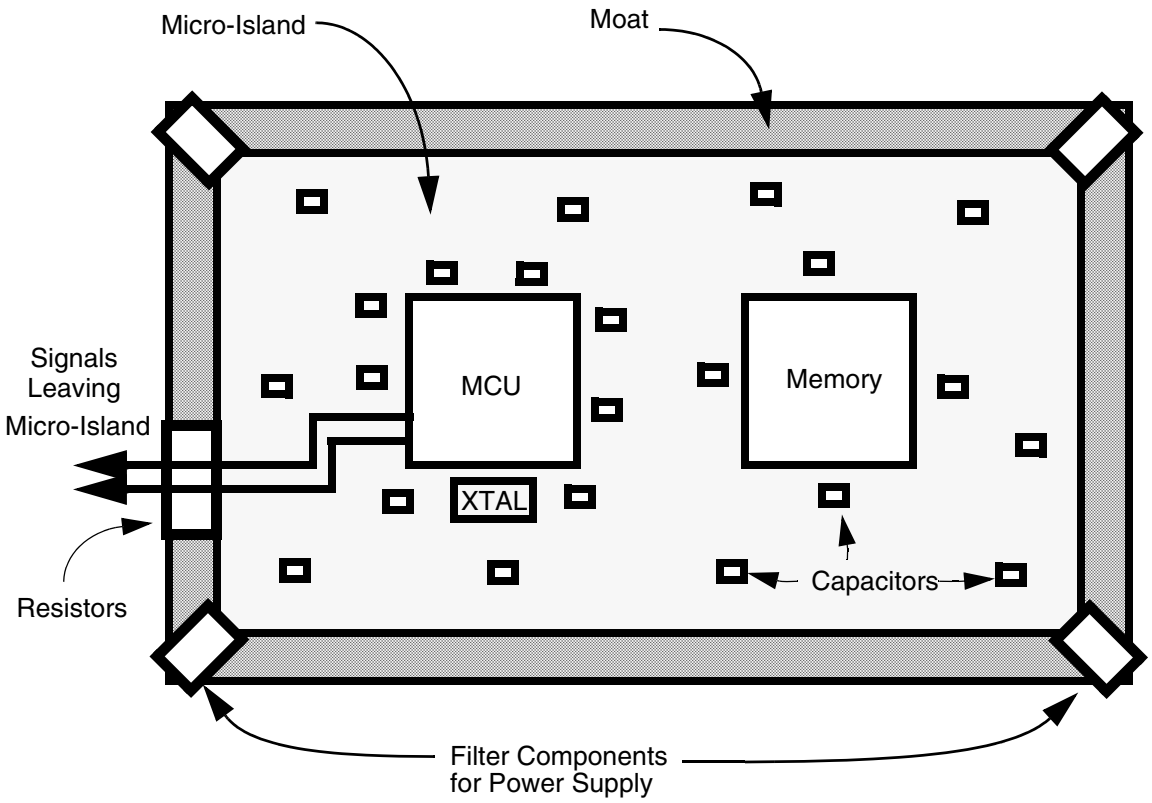

Figure 7. Typical Micro-Island Approach to Decoupling and Grounding

5 Checklist

The following checklist can be used to make sure that all EMC guidelines have been considered. For expanded mode applications, the checklist in AN2705 should also be used.

5.1 Software Checklist

1. All frequency “bands of interest” have been identified and the system frequency has been selected such that the harmonics avoid the “bands of interest” as much as possible.
2. Modulation had been enabled for the FMPLL.
3. The weakest drive strength has been selected for each I/O given the application load and timing requirements.
4. All unused I/O have been disabled.
5. If the nexus or external bus are used, then the gated clock feature has been enabled.
6. All unused modules have been disabled.

5.2 Hardware Checklist

1. The correct number and size of decoupling capacitors have been used on the V_{DD} power supply.
2. The 10-nF capacitors are in low ESL packages such as the 0306 package.
3. The 10-nF capacitors are located as close as possible to the MPC5500 V_{DD} balls.
4. The 10-nF capacitors are distributed evenly around the MPC5500 device (for example, two capacitors per corner).
5. The V_{DD} balls on the MPC5500 device are connected to the 10-nF capacitors using a power plane or wide traces including many vias.
6. Isolated grounds are used.
7. For single-chip applications, a minimum of four layers are used. For expanded mode applications, a minimum of six layers are used.
8. There is at least one ground plane.
9. There is at least one power plane; mixed voltage power plane is acceptable.
10. The power and ground planes have been checked for structures which obstruct the flow of current, such as via anti-pads and embedded slots or traces.
11. The oscillator circuit has a compact layout.

6 References

6.1 Freescale References

1. Dees, Randy. *Bypassing the Analog Power Supplies on the MPC5500 eQADC*. Freescale Engineering Bulletin EB643. 2004.
2. Dobrasevic, Stevan. *EMC Guidelines for MPC500-Based Automotive Powertrain System*. Freescale Application Note AN2127. 2002.
3. Dobrasevic, Stevan. *Signal Integrity Considerations with MPC5500-Based Systems*. Freescale Application Note AN2705. 2004.
4. *MPC5500 Reference Manual*

6.2 General EMC References

1. Clayton, Paul. *Introduction to Electromagnetic Compatibility.* Wiley series.
2. Johnson, Howard. *High-Speed Digital Design: A Handbook of Black Magic*. Prentice Hall, 1993.
3. Ott, Henry. *Noise Reduction Techniques in Electronic Systems*. Wiley and Sons, 1976.
4. Kimmel Gerke Associates website, http://www.emiguru.com/

7 Document Revision History

Table 1 provides a revision history table for this document.

Table 1. Document Revision History

Rev. No.	Substantive Change(s)
0	Initial release.
0.1	Formatting and editorial changes; replaced Figure 2 with black and white version

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Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
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Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
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+46 8 52200080 (English)
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+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
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