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Application Note

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Flash Architectures for i.MX Applications Processors

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1 Abstract

The purpose of this document is to briefly describe the differences of Flash memory available on the market and to discuss the specific design considerations when determining their use in the i.MX family of application processors.

This document applies to the following i.MX devices, collectively called i.MX throughout, unless specifically identified:

- MC9328MX1
- MC9328MXL
- MC9328MXS
- MC9328MX21

1.1 Flash Memory Comparisons

Primarily, there are two types of technology for Flash memory, NOR and NAND Flash. The technologies differ by the type of logic gate used in the storage cell. A hybrid memory based on the NAND technology is the DiskOnChip® (DoC). The differences among these technologies are as follows:

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NOR Flash:

- Non-volatile memory based on NOR cells
- Larger cells compared to NAND cells, therefore a larger chip for the same density
- Large die size with parallel access, thus fast and reliable, although a higher cost memory
- Data correction not required
- Bootable and XIP (eXecute In Place)
- Primary manufacturers: Intel, AMD

Table 1. NOR Flash Attributes

NOR-Flash 256 Mbytes	Rand R: 84 ns Sync R: 66 MHz Blk erase: 200 ms Word prg: 2–4 µs	Op (rand. R): 12 mA Op (sync. R): 20 mA Erase: 25 mA Prog: 35 mA Stdby: 50 µA	$9.00

Note: This document will focus primarily on burst NOR Flash which is the most commonly used flash memory.

NAND Flash:

- Non-volatile memory based on NAND cells
- Cells are small compared to NOR, thus a smaller chip
- Small die size with serial access, thus slow and unreliable although a lower cost memory
- Need ECC (Error Correction Code) to make reliable data storage.
- Block read memory and therefore cannot be used for XIP
- Non-bootable without a capable controller, and no ability for code execution
- Primary manufacturers: Samsung, Toshiba

NOTE

There is not a NAND Flash controller in i.MX processors.

1.2 NAND Flash Sub-Types

Two sub-types of NAND Flash are available for different uses, they are Single Layer Cell (SLC) and Multi Layer Cell (MLC) Flash. A variation of the MLC Flash, is the DiskOnChip (DoC). The SLC, MLC, and DoC are discussed in the following sections.

1.2.1 Single Layer Cell NAND Flash (SLC):

Single Layer Cell NAND Flash memory uses a single layer cell structure. This memory is the more common NAND Flash and corresponds to the generic definition given above. Primarily available from Samsung and Toshiba.

Table 2. NAND SLC Flash Attributes

NAND-Flash SLC (256 Mbytes)	Rand R: 10–25 µs Serial R: 50 ns Blk erase: 2 ms Page prg: 200 µs	Op (serial. R): 10 mA Erase: 10 mA Prog: 10 mA Stdby: 50 µA	$3.50

1.2.2 Multi Layer Cell NAND Flash (MLC):

Multi Layer Cell NAND Flash memory uses a multi layer cell structure. MLC designs allow increased storage capacity on the same die size as compared to an SLC NAND (usually double density). MLC memory typically is the least reliable and has the least speed performance.

NOTE

The i.MX21 processor's NAND Flash controller does not support MLC Flash.

Table 3. NAND with MLC Flash Attributes

NAND-Flash MLC (256 Mbytes)	Rand R: 25 µs Serial R: 50 ns Blk erase: 10 ms Page prg: 1 ms	Op (serial. R): 30 mA Erase: 30 mA Prog: 30 mA Stdby: 50 µA	$2.8

1.2.3 DiskOnChip NAND Flash (DoC):

DoC is an MLC-NAND Flash memory that uses an SRAM interface with its own Flash controller with error correction. Other features include DMA request capability and an internal RAM for use as cache to increase transfer speed and to make it bootable. DoC does not have XIP capability. M-Systems is the only manufacturer of this type of memory.

Table 4. DoC Flash Attributes

DiskOnChip P3-G3 (256 Mbytes)	Rand R: N/A Serial R (N): 55 ns Serial R (T): 33 ns Serial R (MB): 25 ns Blk erase: 2.5 ms Page prg: 300 µs	Op (rand. R): N/A Op (serial. R): 25 mA Erase: 25 mA Prog: 25 mA Stdby: 10 µA	$4.20

DiskOnChip summary:

- Cost: DoC G3 die is almost half the size of a SLC NAND, thus results in less PCB space.
- Reliability: DoC G3 has the same level of reliability as NOR Flash.
- Performance: the access time for DoC is half the access time of NAND Flash.
- This translates to rates of up to 80 Mbytes/sec MultiBurst Read rate and up to 4 Mbytes/sec Sustained Read. It enables extremely fast boot for large open OS such as Microsoft and Symbian. It also means fast performance for linear files such as all multimedia files. Currently measured on an i.MX1 system at 14.5 Mbytes/sec.
- TrueFFS® (Flash File System) specific drivers.

1.3 Summary Table

Table 5. Flash Memory Summary Table

	NOR	DoC	NAND
Reliability	HIGH	HIGH	LOW (without ECC)
Cost	HIGH	MED	LOW
Capacities Available	LOW	HIGH	HIGH
Write Performance	VERY LOW	HIGH	MED
Read Performance	VERY HIGH	HIGH	MED
Ease of integration	HIGH	HIGH	LOW
Boot Capability	YES	YES	YES (i.MX21 only)
XIP Capability	YES	NO	NO

Note: The NAND Flash controller of the i.MX21 provides a high level of ease of integration.

2 Recommended Architectures for i.MX Processors

The first consideration for i.MX processors is that they do not contain a NAND Flash controller. As we discussed previously, this means that the i.MX processors cannot connect to NAND Flash memory. Therefore, only systems based on NOR or DoC are considered for use.

2.1 NOR Flash + RAM

The first recommended memory architecture for use in the i.MX processor is a NOR Flash associated to a RAM memory. The code and data are stored into the Flash where the code is executed. The RAM is only used for volatile data (variables, buffers, and so on), and not for code execution therefore it will be as small as possible. For cost effectiveness, a SRAM or PSRAM is recommended when fewer bytes are required and a SDRAM is recommended when larger bytes are required.

As the cost-per-byte ratio for a NOR Flash is high, that assumes the amount of user's data will be as small as possible. Typically, applications for such architecture must not target devices with high requirements of embedded user data—such as, payment terminals, card readers, security devices, and so on.

In multimedia applications, consideration must be given to the addition of an external memory device for mass storage—such as, Multimedia card, Secure Digital card, Compact Flash, and even a PCMCIA hard drive.

Typical memory requirements depend on whether an OS is required:

- NOR Flash contains between 2 Mbytes to 32 Mbytes
- RAM contains between minimal Kbytes to 16–32 Mbytes

If the design targets applications such as, USB key MP3 player, with a large requirement for mass storage, this solution is not cost effective and therefore is not appropriate.

If the design targets applications that require Flash memory sizes above 32 Mbytes, it is strongly recommended to use a NAND Flash memory. A solution is the DoC, as its bootable SRAM interface and NAND Flash is compatible with any of the i.MX processors.

As this is the most powerful architecture, it can be designed for use in high performance systems, even with mass storage, however cost will not be considered as an issue.

TARGETED SYSTEMS: Payment terminals, card readers, security devices, multimedia memory card readers, and so on.

2.2 DiskOnChip Flash + SDRAM

In applications where an extremely large amount of data space is required, the DiskOnChip is the best solution in terms of cost. Advantages are the die size compared to the density that reduces the price per bytes (commonly used in DiskOnKey®).

NAND memory does not allow executing code in place, therefore an SRAM design is cost prohibitive if the code is large because a complete copy of the code is required in a RAM.

The typical solution is then a DoC (32 Mbytes to 256 Mbytes) + SDRAM (at least 16 Mbytes for most of the OS).

It is possible to use a small SRAM for a small amounts of code, for example if only used for an MP3 player.

TARGETED SYSTEMS: Multimedia-entertainments devices, PDAs, features phones, or even smartphones, and so on.

3 Recommended Architectures for i.MX21 Processors

3.1 NOR Flash + RAM

Please refer to Section 2.1, “NOR Flash + RAM” on page 4.

3.2 DiskOnChip Flash + SDRAM

Please refer to Section 2.2, “DiskOnChip Flash + SDRAM” on page 5.

This is a possible solution for a design, however with the i.MX21 processor consideration must be given to the NAND Flash controller. From a cost perspective, the DoC is more expensive than a NAND Flash because of the controller attached to the MCL NAND of a DoC.

For applications requiring more than 64 Mbytes, DoC is competitive and design decisions depend on the customer’s requirements. NAND Flash technology with the appropriate controller is still in its infancy and anticipated to be improved over the next few years.

3.3 NAND Flash + SDRAM

In applications where an extremely large amount of data space is required, the NAND Flash is recommended for the i.MX21 processor which is able to manage this type of memory. Advantages are the die size compared to the density that reduces the price per bytes.

NAND flash memory does not allow executing code in place, therefore an SRAM design is cost prohibitive if the code is large because a complete copy of the code is required in a RAM.

The typical solution is therefore a NAND Flash (32 Mbytes to 256 Mbytes) + SDRAM (at least 16 Mbytes for most of the OS).

It is possible to use a small SRAM for a small amounts of code, for example if only used for an MP3 player.

TARGETED SYSTEMS: Most systems as the cost is the lowest possible, however, primarily used for multimedia-entertainments devices, PDAs, features phones, smartphones, and so on.

4 Conclusion – Summary

From a performance perspective, i.MX solutions based on NOR Flash are better. From a cost perspective, NAND or DoC based architectures are recommended. Table 6 provides a summary of the Flash architecture recommendations.

Table 6. i.MX Flash Architecture Recommendations

	COST EFFECTIVE	PERFORMANCE	MASS STORAGE	CODE ONLY
NOR	X	XXXX	PDA, smartphones, and so on	Card readers, payment terminals, security, …
DoC	XXX	XX	Multimedia, entertainment applications	Card readers, payment terminals, security, … (i.MX)
NAND (i.MX21 only)	XXXX	XX	Multimedia, entertainment applications	Card readers, payment terminals, security, … (i.MX21)

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