Freescale Semiconductor
Application Note

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PowerQUICC III Bring-Up Guideline

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This document provides recommendations for designs based on the MPC8540 and the MPC8560 devices from the PowerQUICC III family of integrated communications processors (collectively referred to throughout this document as PowerQUICC III). This document may also be useful in debugging newly designed systems by highlighting those aspects of a design that merit special attention during initial system startup. The MPC8540 and the MPC8560 both contain a Power Architecture processor core.

Contents

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1 Getting Started

This section outlines recommendations to simplify the first phase of design. Before designing a system with a PowerQUICC III device, it is recommended that the designer be familiar with the available documentation, software, microcodes, models, and tools.

1.1 References

Please note that some items below may only be available under a nondisclosure agreement (NDA). For those documents, please contact your local field applications engineer or sales representative to obtain a copy.

- Collateral
  - *MPC8560 PowerQUICC III Integrated Communications Processor Reference Manual* (MPC8560RM)
  - *MPC8540 PowerQUICC III Integrated Host Processor Reference Manual* (MPC8540RM)
  - *MPC8560 Device Errata* (MPC8560CE)
  - *MPC8540 Device Errata* (MPC8540CE)
  - *MPC8560 Integrated Processor Hardware Specifications* (MPC8560EC)
  - *MPC8540 Integrated Processor Hardware Specifications* (MPC8540EC)
- Available Tools
  - CPM Performance Tool
  - Boot Sequencer Generator Tool
  - Pin Mux Tool
  - UPM Programming Tool
- Models
  - IBIS
  - SWIFT (Verilog)
  - BSDL, Rev 2 silicon

1.2 Device Errata

The device errata documents (MPC8540CE, MPC8560CE) describe the latest fixes and workarounds for the PowerQUICC III family of devices. The errata documents should be thoroughly researched prior to starting a design with the respective PowerQUICC III device.

1.3 Communications Processor Module (CPM) Performance and Bus Utilization Tool (MPC8560 Only)

The PowerQUICC III CPM runs by time-sharing multiple communication protocols. To estimate the CPM load factor for a particular combination of protocols, designers are encouraged to use the CPM Performance Evaluator tool, which is available on the MPC8560 device web site.

Note that at startup the tool initializes all parameters with default values that may not be the optimal values for your design. For example, the tool initializes with transmit and receive rates of ‘0’. These values must be changed according to each particular application.

1.4 Boot Sequencer Tool

The PowerQUICC III features the boot sequencer to allow configuration of any memory mapped register before the completion of power-on reset (POR). The register data to be changed is stored in an I^2C EEPROM. The PowerQUICC III requires a particular data format for register changes as outlined in the MPC8540RM and the MPC8560RM. The boot sequencer tool is a C code file. When compiled and given a sample data file, it will generate the appropriate raw data format as outlined in the MPC8540RM and the MPC8560RM as well as an s-record file that can be used to program the EEPROM.

1.5 Pin Mux Tool (MPC8560 Only)

The on-chip serial communications peripherals use four 32-bit parallel ports to exchange data with the physical interfaces. On each pin of the parallel ports several signals are multiplexed. If none of the signals available on a certain pin are necessary in a certain application, the pin can be used for a general purpose I/O.

To verify the availability of the I/O functions chosen through pin multiplexing, designers are encouraged to use the MPC8560 Parallel Ports Pin Mux Tool. After selecting the signals required by your application, this utility assists in defining the pin configuration of each parallel port. A report can then be generated that includes all your selections and C-initialization code for the registers associated with the parallel ports.

The Pin Mux Tool can be found on the MPC8560 device website.

1.6 UPM Programming Tool

The UPM Programming Tool features a GUI for a user friendly programming interface. It allows programming of all three of the PowerQUICC III’s UPM machines. The GUI consists of a wave editor, a table editor, and a report generator. The user can edit the waveform directly or the RAM array directly. At the end of programming, the report generator will print out the UPM RAM array that can be used in a C-program.

The UPM Programming Tool can be found on the MPC8560 or the MPC8540 device website.

1.7 Available Training

Our 3rd party partners are part of an extensive Design Alliance Program. Our current training partners can be found on our external website under the Design Alliance Program.

In addition to this, training material from past Smart Network Developer’s Forums is available. The training material is a valuable resource for understanding the PowerQUICC III and is also available on the website.

2 Power

This section provides design considerations for the PowerQUICC III power supplies. For information on AC and DC electrical specifications and thermal characteristics for the PowerQUICC III, refer to the MPC8540EC and the MPC8560EC.

2.1 Power Supply

The PowerQUICC III has a core voltage V_{DD} which operates at a lower voltage than the I/O voltages GV_{DD}, LV_{DD}, and OV_{DD}. It is recommended that the core voltage V_{DD} of PowerQUICC III be supplied through a variable switching supply or regulator to allow for future compatibility with possible core voltage changes on future silicon revisions. The core voltage, 1.2 V (±5%), is supplied across V_{DD} and GND.

The I/O blocks of the PowerQUICC III are supplied with 2.5 V (±5%) across GV_{DD} and GND, 2.5 V (±5%) or 3.3 V (±5%) across LV_{DD} and GND, and 3.3 V (±5%) across OV_{DD} and GND. Typically, these are supplied by simple linear regulators. This increases the complexity of the system because multiple voltage supplies and PCB power planes are required for the design. No external signals on PowerQUICC III are 5 V tolerant. All input signals need to meet the $G/L/OV_{IN}$ DC specification of the respective I/O block. Table 1 describes the power supplies.

Table 1. Power Supplies

Type	Name	Block	(V)
Core	V_{DD}	—	1.2
PLL	AV_{DD}	Core PLL, Platform PLL, CPM PLL (MPC8560 only)	1.2
I/O	GV_{DD}	DDR	2.5
I/O	LV_{DD}	TSEC	2.5/3.3
I/O	OV_{DD}	CPM, PCI, LBIU, DMA, MII-mgt, RapidIO, PIC, I^2C	3.3

2.2 Power Consumption

The MPC8540EC and the MPC8560EC Hardware Specification documents provide estimated power dissipation for various frequency configurations of the core complex bus (CCB) clock and the e500 core frequencies. Suitable thermal management is required to ensure the junction temperature does not exceed the maximum specified value.

Keep in mind that the numbers provided in the hardware specification include dissipation for all blocks except the PLL supplies and the I/Os. Both must be added to the typical number in order to accurately determine whether a heat sink or other form of chip cooling mechanism is required.

To estimate the I/O power consumption for the PowerQUICC III, designers are encouraged to use the MPC8560 Power Consumption Calculator Tool. Users are required to enter valid clock frequencies and a valid V_{DD} voltage. Even though the tool recognizes individual invalid parameter values, it does not recognize combinations of invalid parameters. To ensure valid combinations, users should refer to the relevant hardware specification document. All fields are required.

2.3 Power Sequencing

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. These rates depend on the nature of the power supply, the type of load on each power supply, and the manner in which different voltages are derived. The MPC8555E and MPC8541E require the power rails to be applied in a specific sequence to ensure proper device operation. The requirements for power-up are as follows:

- V_{DD}, AV_{DD}
- GV_{DD}, LV_{DD}, OV_{DD} (I/O supplies)

Items on the same line have no ordering requirements with respect to one another. Items on separate lines must be ordered sequentially so that voltage rails on a previous step reach 90 percent of their value before the voltage rails on the current step reach 10 percent of theirs. If the items on line 2 must precede items on line 1, take care to ensure that the delay does not exceed 50 mS and that the power sequence is not performed more than once per day in a production environment.

NOTE

To guarantee MCKE low during power-up, GVDD should be the last power supply to come up. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing is not required.

NOTE

From a system standpoint, if the I/O power supplies ramp prior to the V_{DD} core supply, the port pins on the MPC8560 CPM may drive a logic one or zero during power-up.

Table 2 lists the current maximum ratings for the power supplies. Supplies must not exceed these absolute maximum ratings. However, during normal operation, use of the recommended operating conditions given in the hardware specification is recommended. Any information in the relevant hardware specification supersedes information in Table 2.

Table 2. Maximum Voltage Ratings

Type	Name	Block	(V)	(Vmax)
Core	V_{DD}	—	1.2	1.32
PLL	AV_{DD}	Core PLL, Platform PLL, CPM PLL (MPC8560 only)	1.2	1.32
I/O	GV_{DD}	DDR	2.5	3.63
I/O	LV_{DD}	TSEC	2.5 / 3.3	2.75 / 3.63
I/O	OV_{DD}	CPM, PCI, LBIU, DMA, MII-mgt, RapidIO, PIC, I^2C	3.3	3.63

2.4 Power Planes

Each V_{DD} pin should be provided with a low-impedance path to the board's power supply. Each ground pin should likewise be provided with a low-impedance path to ground. The power supply pins drive

distinct groups of logic on chip.The capacitor leads and associated printed circuit traces connecting to chip V_{DD} and ground should be kept to less than half an inch per capacitor lead.

2.5 Decoupling

Due to large address and data buses, and high operating frequencies, the PowerQUICC III can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PowerQUICC III system, and the PowerQUICC III itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and pins of the PowerQUICC III. These decoupling capacitors should receive their power from separate V_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, GV_{DD}, LV_{DD}, and OV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF.

Simulation is strongly recommended to minimize noise on the power supplies before proceeding into the PCB design and manufacturing stage of development.

2.6 PLL Power Supply Filtering

Each of the PowerQUICC III PLLs is provided with power through independent power supply pins ($AV_{DD}1$ and $AV_{DD}2$ for the MPC8540; $AV_{DD}1$, $AV_{DD}2$, and $AV_{DD}3$ for the MPC8560). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages will be derived directly from V_{DD} through a low frequency filter as shown in Figure 1.

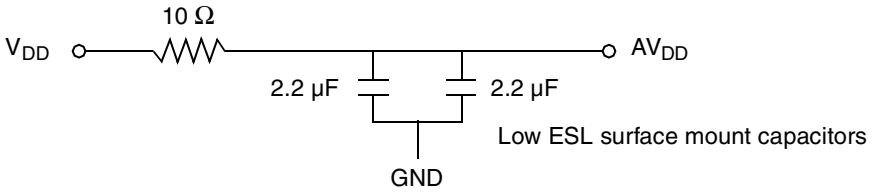

Figure 1. PLL Power Supply Filter Circuit

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide three independent filter circuits, one to each of the three AV_{DD} pins. By providing independent filters to each PLL the opportunity to cause noise injection from one PLL to the other is reduced.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum effective series inductance (ESL).

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 783 FC-PBGA footprint, without the inductance of vias. If possible, a separate plane for each PLL filtering circuit is recommended.

3 Clocking

3.1 System Clock

The system clock SYSCLK input is the primary clock source for all synchronous blocks on the PowerQUICC III and must always be provided. The SYSCLK input is multiplied up by a phase-lock loop (PLL) to generate the core complex bus (CCB) clock. The CCB clock is used by the L2 cache, RapidIO, CPM and DMA. It is divided by two to generate the DDR clocks MCK[0:5]. It is divided by 2/4/8 (in the LCRR[CLKDIV] register) to generate local bus clocks LCLK[0:2]. It is also multiplied up by a second PLL (by the power-on reset setting LALE, LGPL2) to generate the e500 core clock. As there are no default settings for the two PowerQUICC III PLLs, power-on reset configuration of them within the system design is a must. See Figure 2 and Table 3 for more information.

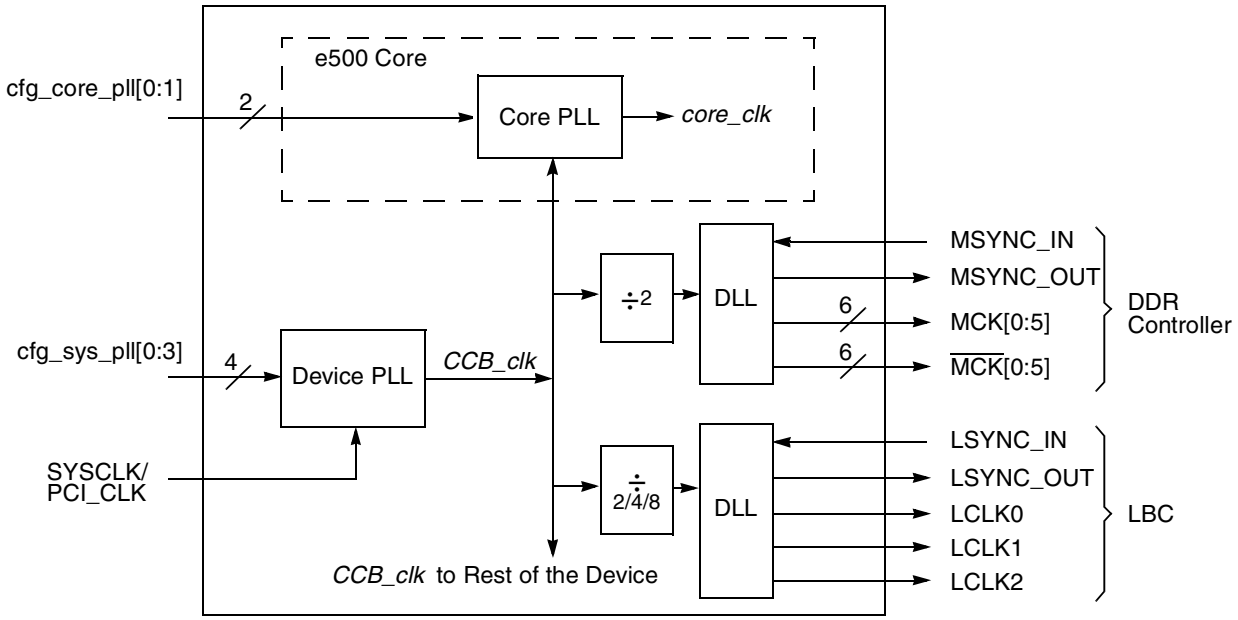

Figure 2. Clock Subsystem Block Diagram

Table 3. Clocking Quick Reference

Functional Block	Clock Derivation
Core (including L1)	CCB * [2, 2.5, 3, 3.5]
DDR	CCB / 2
I^2C	CCB / (I2CFDR ratio)
L2 cache, CPM	CCB

Table 3. Clocking Quick Reference (continued)

Functional Block	Clock Derivation
Local Bus	CCB / [2,4,8]
PCI, PCI-X	SYSCLK
RapidIO	CCB, Rx_CLK, or External Source
TSEC	125MHz from PHY or External (certain modes)

3.2 Clocking Example

Assume that the frequencies of certain key interfaces should be maximized. Then use the following inputs:

- SYSCLK = 66 MHz
- CCB multiplier = 5 (cfg_sys_pll)
- Core multiplier = 2.5 (cfg_core_pll)
- Local bus divider = 2 (LCRR[CLKDIV])

The resulting frequencies for the following interfaces are:

- Core = SYSCLK * cfg_sys_pll * cfg_core_pll = 833 MHz
- CPM = SYSCLK * cfg_sys_pll = 333 MHz
- DDR (MCK*n*) = SYSCLK * cfg_sys_pll/2 = 167MHz = 333 MHz data rate
- PCI = SYSCLK = 66 MHz
- Local Bus (LCLK*n*) = SYSCLK * cfg_sys_pll / CLKLDIV = 167 MHz

These frequencies are the maximum frequencies supported today. Please check the relevant product website for updated options.

3.3 Core Clock

The frequency of the core is determined at POR through the LALE and the LGPL2 pins. Below in Table 4 are the options for configuring the core clock as a multiple of the CCB clock. This information can be found in the MPC8540RM or the MPC8560RM.

Table 4. Core Clock POR Configuration

LALE, LGPL2	Core: CCB
00	2:1
01	2.5:1
10	3:1
11	3.5:1

3.4 DDR SDRAM Clock Outputs

The DDR SDRAM clock outputs MCK[0:5] and MCK[0:5] are derived from the CCB clock. No configuration pins or register settings are required to generate the MCK/$\overline{\text{MCK}}$*n* frequencies as they are by default one-half the CCB clock frequency.

3.5 I^2C Clock

The I^2C clock rate is determined by a ratio set in the I^2C frequency divider register (I2CFDR). Refer to the MPC8540RM or the MPC8560RM for more information.

3.6 L2 Cache and CPM Clocks

The clock rate for the L2 Cache and the CPM is the same as the CCB clock frequency.

3.7 Local Bus Clock Outputs

The local bus clock outputs LCLK[0:2] are derived from the CCB clock. By default the LCLK*n* frequency is CCB clock frequency divided by eight. However, by appropriately setting the system clock divider parameter in the clock ratio register (LCRR[CLKDIV]), the LCLK*n* frequency can be configured as shown in Table 5.

Table 5. Local Bus Clock Divider Options

LCRR[CLKDIV]	LCLKn Frequency
0010	CCB Clock / 2
0100	CCB Clock / 4
1000 (Default)	CCB Clock / 8
All other values	Reserved

3.8 PCI and PCI-X Clock Input

The input clock for the PCI and PCI-X interfaces on the PowerQUICC III is the system clock SYSCLK input; there is no separate PCI clock input on PowerQUICC III. When the PowerQUICC III PCI/PCI-X interface is used, the SYSCLK input serves dual function as both the system clock and the PCI clock.

3.9 RapidIO Transmit Clock Input

The power-on reset configuration allows the designer to select the source of the RapidIO transmit clock RIO_TCLK. One of the clock source selections is an external clock source supplied on the RapidIO transmit clock input pin RIO_TX_CLK_IN. This option should be utilized when the option to use the CCB clock as the source does not match the frequency of the RapidIO network to which the PowerQUICC III interfaces.

The option to use the RapidIO receive clock (RIO_RCLK) as the transmit clock should only be used in debug. The transmit clock has tighter timing requirements than the receive clock. Therefore, if the receive clock is used, the timings may not be met for the transmit clock.

3.10 TSEC Reference Clock Input

The EC_GTX_CLK125 signal is not used for MII mode.

When any other mode is used in the TSEC interface, the gigabit transmit 125 MHz reference clock EC_GTX_CLK125 must be supplied. This signal must be generated externally with a crystal or oscillator, or it can sometimes be provided by the PHY. In GMII, RGMII, RTBI or TBI mode, EC_GTX_CLK125 is a 125 MHz input into the TSEC and is used to generate all 125 MHz related signals and clocks.

4 Debug

The following sections describes the PowerQUICC III reset sequence and recommendations for the system.

4.1 $\overline{\text{TRST}}$

$\overline{\text{TRST}}$ is the reset pin for the JTAG/COP interface. It must be held at a low level during the assertion of $\overline{\text{HRESET}}$ in order to completely reset all logic on the PowerQUICC III.

For compatibility with third party tools, it is required that $\overline{\text{TRST}}$ and $\overline{\text{HRESET}}$ have the ability to independently assert. Figure 3 demonstrates one example of circuity that can be used to accomplish this.

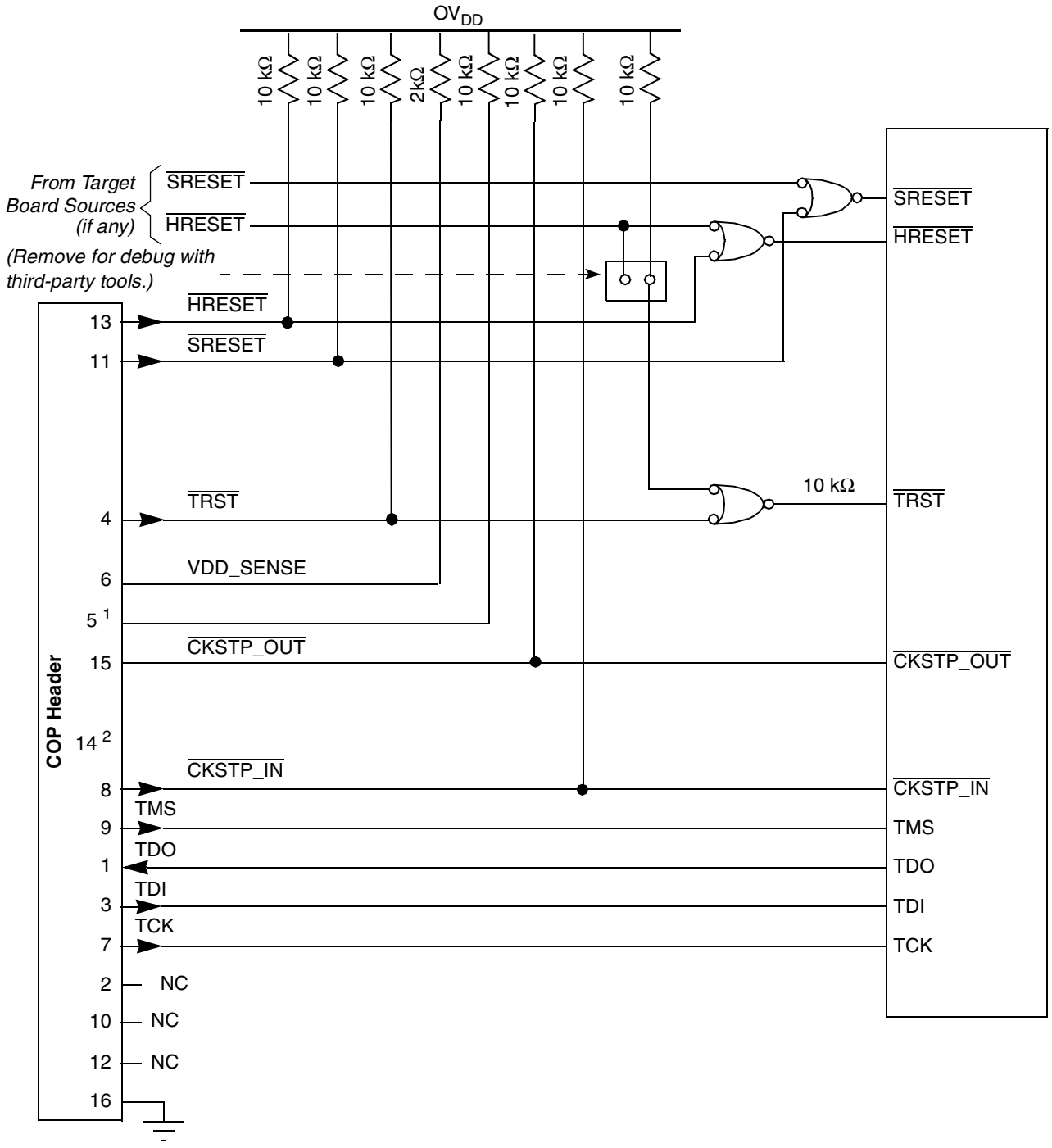

Figure 3. COP Connections to PowerQUICC III

The COP header is fully described in Figure 4 and Table 6.

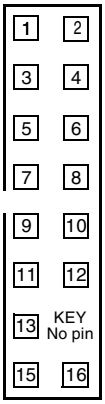

Figure 4. COP Header Pinout

Table 6. COP Header Definition

Header Position	Name	Description
1	TDO	Test Data Output
2	NC	
3	TDI	Test Data Input
4	TRST	Test Reset
5	Not implemented. Connect to OV_{DD} with a 10 KΩ resistor.	
6	VDDS	VDD Sense
7	TCK	Test Clock
8	CKI	Checkstop In
9	TMS	Test Mode Select
10	NC	
11	SRST	Soft Reset
12	NC	
13	HRST	Hard Reset
14	KEY	
15	CKO	Checkstop Out
16	GND	Ground

4.2 Recommended Test Points

For easier debug, it is recommended that the test points on the board include the following pins:

- CLK_OUT (This helps to verify the CCB clock.)
- TRIG_OUT (This helps to verify the end of the reset sequence.)

- ASLEEP (This helps to verify the end of the reset sequence.)
- SENSEVDD (This helps to verify power plane $V_{DD.}$)
- SENSEVSS (This helps to verify ground plane $V_{SS.}$)
- $\overline{\text{HRESET\_REQ}}$ (This helps to verify proper boot sequencer functions and reset requests.)

5 Power-On Reset and Reset Configurations

5.1 Configurable Options

Various device functions are initialized by sampling certain signals during the assertion of $\overline{\text{HRESET}}$. These inputs are either pulled high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while $\overline{\text{HRESET}}$ is asserted. $\overline{\text{HRESET}}$ must be asserted for a minimum on 100 µs. When $\overline{\text{HRESET}}$ de-asserts, the configuration pins are sampled and latched into registers and the pins then take on their normal output circuit characteristic from an input circuit during $\overline{\text{HRESET}}$.

Most of the configuration pins have an internally gated 20 KΩ pull-up resistor, enabled only during $\overline{\text{HRESET}}$. For those configurations in which the default state is desired, no external pull-up is required. Otherwise, a 4.7 KΩ pull-down resistor is recommended to pull the configuration pin to a valid logic low level. In the case where a configuration pin has no default, 4.7 KΩ pull-up or pull-down resistors are recommended for appropriate configuration of the pin. Table 7 summarizes all the power-on reset configurations possible on the device.

Table 7. Power-On Reset Configurations

Type of Configuration	Configuration Pins	Default State
CCB Clock PLL Ratio	LA[28:31]	**No default state;** pins must be configured at $\overline{\text{HRESET}}$
e500 Core PLL Ratio	LALE, LGPL2	**No default state;** pins must be configured at $\overline{\text{HRESET}}$
Boot ROM Location	TSEC1_TXD[6:4]	Local Bus GPCM, 32-bit ROM
Host/Agent	$\overline{\text{LWE}}$[2:3]	Device acts as the host processor for PCI/PCI-X and RapidIO
CPU Boot	LA27	The core is allowed to boot without waiting for configuration from any external master
Boot Sequencer	LGPL3, LGPL5	Boot sequencer is disabled
TSEC Width	EC_MDC	Ethernet interfaces operate in standard GMII or TBI modes
TSEC1 Protocol	TSEC1_TXD7	TSEC1 operates using the TBI (or RTBI) protocol
TSEC2 Protocol	TSEC2_TXD7	TSEC2 operates using the TBI (or RTBI) protocol
RapidIO Transmit Clock Source	LGPL0, LGPL1	The CCB clock is the source of the transmit clock
RapidIO Device ID	TSEC2_TXD[2:4]	The 3 LSBs of the device ID are [111]
PCI Width	$\overline{\text{PCI\_REQ64}}$	PCI/PCI-X operates as a 32-bit interface
PCI I/O Impedance	$\overline{\text{PCI\_GNT1}}$	42Ω drivers are used on the PCI interface
PCI Arbiter	$\overline{\text{PCI\_GNT2}}$	The on-chip PCI/PCI-X arbiter is enabled

Table 7. Power-On Reset Configurations (continued)

Type of Configuration	Configuration Pins	Default State
PCI Debug	PCI_GNT3	PCI operates in normal mode
PCI-X	PCI_GNT4	PCI mode is used
Memory Debug	MSRCID0	DDR debug information is driven on MSRCID and MDVAL
DDR Debug	MSRCID1	No debug information is driven on the ECC pins
PCI/PCI-X Output Hold	LWE[0:1]	PCI: Two added buffer delays to meet 2ns hold time PCI-X: No added buffer delays to meet 0.7ns hold time
Local Bus Output Hold	TSEC2_TXD[6:5]	One added buffer delay
General Purpose POR	LAD[0:31]	No default state; pins must be configured at HRESET if GPPORCR is intended to be accessed by a user system

An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device which drives the configuration signals when HRESET is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of HRESET (PLL configuration inputs must meet a 100 ms set-up time to HRESET), hold their values for at least 2 SYSCLK cycles after the de-assertion of HRESET, and release the pins to high impedance afterward for normal device operation.

For a more detailed description on the power-on reset configurations and their definitions, refer to the MPC8540RM and the MPC8560RM.

The POR configuration settings can be read in the POR PLL status register (PORPLLSR), the POR boot mode status register (PORBMSR), the POR I/O impedance status and control register (PORIMPSCR), the POR device status register (PORDEVSR), the POR debug mode status register (PODBGMSR), and the general-purpose POR configuration register (GPPORCR). See the MPC8540RM or the MPC8560RM for details of these registers. (Note that all of these registers are read-only registers except for PORIMPSCR.)

The general purpose POR configuration register (GPPORCR) can be used to pass any information on the local bus address/data pins LAD[0:31] to software. For instance, we can pass information about a circuit board's revision number to software by driving the pins in any order. The information is automatically sampled from LAD[0:31] during POR. Then software can at any time read this register and process the data accordingly. There is no default settings for this register. If it is not used, it is not necessary to drive the pins high or low.

5.2 Internal Manufacturing Test Modes

A few pins on the PowerQUICC III device have a secondary function of enabling internal manufacturing test modes on the device. These modes are enabled during the HRESET sequence by driving the respective pin to a logic zero state.

NOTE

If any of these modes are enabled during normal operation of the device, the device will not come out of reset, and the system will hang.

To avoid accidentally enabling these internal test modes, care should be taken to make sure that these pins are either floating (as they implement an internal weak pull-up resistor), or are pulled high during the reset sequence in the event that they are connected to a device which pulls these pins low.

There are some additional test pins which must be pulled up by a resistor connected to OV_{DD} during all normal operation of the device. If any of these pins are pulled low, the system may hang. (Please refer to the MPC8540EC or the MPC8560EC).

Table 8. Internal Test Mode and Debug Pins

Pin	Pin Type	Comment
ASLEEP	Internal test mode	Pull up or leave floating during reset only
L1_TSTCLK	Internal debug	Pull up to OV_{DD}
L2_TSTCLK	Internal debug	Pull up to OV_{DD}
LBCTL	Internal test mode	Pull up or leave floating during reset only
$\overline{\text{LSSD\_MODE}}$	Internal debug	Pull up to OV_{DD}
TRIG_OUT/READY	Internal test mode	Pull up or leave floating during reset only
TSEC1_TXD[0:3]	Internal test mode	Pull up or leave floating during reset only

5.3 Boot Sequencer

The boot sequencer allows configuration of any memory mapped register prior to running the boot-up code. When enabled, it will load code from an EEPROM located on the I^2C bus. For example, this code can be used to configure the port interface registers if the device is booting from PCI, PCI-X, or RapidIO.

The boot sequencer is enabled during power-on reset by the [LGPL3, LGPL5] pins. These two signals can also enable extended boot sequencer mode.

Please refer to the MPC8540RM or the MPC8560RM for the complete data format for programming the I^2C EEPROM.

The CRC algorithm used is:

$$1 + x^1 + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$$

The start value is 0xFFFF_FFFF. The final XOR value is 0x0000_0000.

The boot sequencer contains a basic level of error detection. If a preamble or CRC fail is detected, the external $\overline{\text{HRESET\_REQ}}$ will assert. The I^2C pins will continue to be pulled low during a fail until a hard reset occurs.

5.4 Boot Hold-off Mode

The PowerQUICC III can be put into slave mode in a system. In this situation, an external master on the PCI, PCI-X, or the RapidIO bus will need to configure the device. Boot hold-off mode, when enabled during power-on reset, allows any external master on these buses to configure the device.

To enable this mode during power-on reset, use the LA27 pin. During this mode, the core is suspended from fetching boot code. To exit this mode, the EEBPCR[CPU_EN] must be set.

6 Functional Blocks

The following sections discuss the recommendations and guidelines for designing with the various functional blocks on PowerQUICC III.

6.1 Global Utilities

The PowerQUICC III provides a global utilities block which controls power management, I/O device enabling, power-on reset configuration monitoring, and other debug functions. Refer to Section 5.1, "Configurable Options." Below is information about the device disable register (DEVDISR) and low-power modes of which the designer should be aware.

6.1.1 Device Disable Register (DEVDISR)

After the PowerQUICC III comes out of reset, all functional blocks are enabled. However, there are situations where all interfaces of the PowerQUICC III may not be used. In this case, it would be more power efficient to disable these interfaces.The DEVDISR contains disable bits for the PCI, LBC, L2, RIO, DDR, e500, Time Base, CPM, DMA, TSEC1, TSEC2, and the I^2C interface. If desired, these blocks may be disabled by setting these bits to a logic 1 by the core or an external master.

When a block is disabled with this register, all clocks are disabled to the block, thereby saving power. However, a result of not having clocks to an interface is that the interface will not respond to any interrupts or accesses. A programming error will occur when trying to access configuration or status registers of a block while disabled.

These interfaces may not be re-enabled without asserting $\overline{\text{HRESET}}$. Without asserting $\overline{\text{HRESET}}$, the results will be undefined.

Disabling the e500 core through this register is equivalent to nap mode. This is not recommended since any interface disabled through DEVDISR requires an $\overline{\text{HRESET}}$ to re-enable it. Use the low-power nap mode instead.

6.1.2 Low-Power Modes

In addition to the DEVDISR, the PowerQUICC III allows you to further reduce the power consumption through the low-power modes. There are three low-power modes: doze, nap, and sleep. Detailed information about these modes can be found in the relevant user's manual.

Putting the device into nap mode is equivalent to disabling the e500 core through the DEVDISR register. However, since waking up the device is not possible when using the DEVDISR except through an $\overline{\text{HRESET}}$, it is recommended that nap mode be used instead.

6.2 Core

Multiprocessor functionality is not implemented in the PowerQUICC III e500 core:

- There are no shared (S) states in the L1 or L2 cache.
- The memory coherence bit, M, controlled through MAS2[M] / MAS4[MD] and MAS2[SHAREN] / MAS4[SHAREND], has no effect.

- HID1[MSHARS] and HID1[SSHAR] are not implemented
- HID1[ABE] is only used to ensure (when set) that cache and TLB management instructions operate properly with respect to the L2 cache.
- There is no dynamic bus snooping. If the PowerQUICC III is in a nap or sleep state, the core is not wakened to snoop global transactions.

The PowerQUICC III does not implement double-precision floating point. If needed, it can be emulated through software. The PowerQUICC III supports single-precision scalar and single-precision vector floating point only through various APUs on-chip. In addition, 64-bit operands are not supported because the e500 is a 32-bit implementation of Book E.

The SPE APU and SPFP APU functionality will be implemented in the MPC8540, the MPC8560 and their derivatives (that is, in all PowerQUICC III devices). However, these instructions will not be supported in devices subsequent to PowerQUICC III. Freescale strongly recommends that use of these instructions be confined to libraries and device drivers. Customer software using SPE or SPFP APU instructions at the assembly level or using SPE intrinsics will require rewriting for upward compatibility with next generation PowerQUICC devices. Freescale offers a lib_moto_e500 library that uses SPE and SPFP APU instructions and will provide future libraries to support next generation PowerQUICC devices.

6.3 DDR SDRAM

Please refer to *AN2582 Hardware and Layout Design Considerations for DDR Memory Interfaces* for detailed information on signal integrity and layout considerations.

Configuration of the DDR bus should not be done while running from it, but rather by executing code from another interface (that is, the local bus).

6.3.1 Termination of DDR Signals During Normal Operation

Parallel termination is optional for DDR signals and should be simulated to verify necessity. Differential termination is included on DIMM. It is only required for discrete memory applications.

Refer to the application note AN2582 for more detail on termination schemes.

It is strongly recommended that with any termination scheme, signal integrity analysis be performed using the respective device IBIS model.

6.3.2 Termination of Unused DDR Signals

Termination is not needed on output signals. For I/Os, tie signals high or low through a resistor. Recommended resistor values are 2–10 kΩ. For inputs, tie signals to their inactive state through a resistor; clock inputs may be tied high or low. Recommended resistor values are 2–10 KΩ.

6.4 I^2C Unit

6.4.1 Termination of I^2C Signals During Normal Operation

Tie both SDA and SCL high through a 1 kΩ resistor.

6.4.2 Termination of Unused I²C Signals

When this interface is not used, it is recommended to individually tie the signals high through a resistor. Recommended resistor values are 2–10 KΩ.

6.5 Local Bus Interface Unit

The local bus frequency can be adjusted through the LCRR[CLKDIV] register. If modified, the DLL requires a re-lock time prior to use. The lock time can vary between ~7680 to 122880 CCB clock cycles. It is a ratio between the LBC clock and the CCB clock. The 2:1 ratio corresponds to the minimum lock time and the 8:1 ratio corresponds to the maximum lock time.

The PowerQUICC III features adjustable drive strengths for the local bus. The PORIMPSCR configures most local bus signals to either a 25 or 42 Ω. This configurable drive strength can help improve signal integrity by matching the load on the I/O. Some applications will have heavy loading on the bus. In this case, the stronger drive strength of 25 Ω is recommended. If there is light loading on the bus, the weaker drive strength of 42 Ω is recommended. A driver / I/O impedance mismatch can cause noise issues on the signal. The decision as to which driver to use should be based on signal integrity analysis with the available IBIS models.

Reconfiguration of the local bus clock should not be done while executing from the local bus, but rather by executing code from another interface (that is, DDR).

The PowerQUICC III local bus features a multiplexed address and data bus, LAD[0:31]. An external latch is required to de-multiplex these signals to the connecting device. Figure 5 shows the local bus connection to SDRAM.

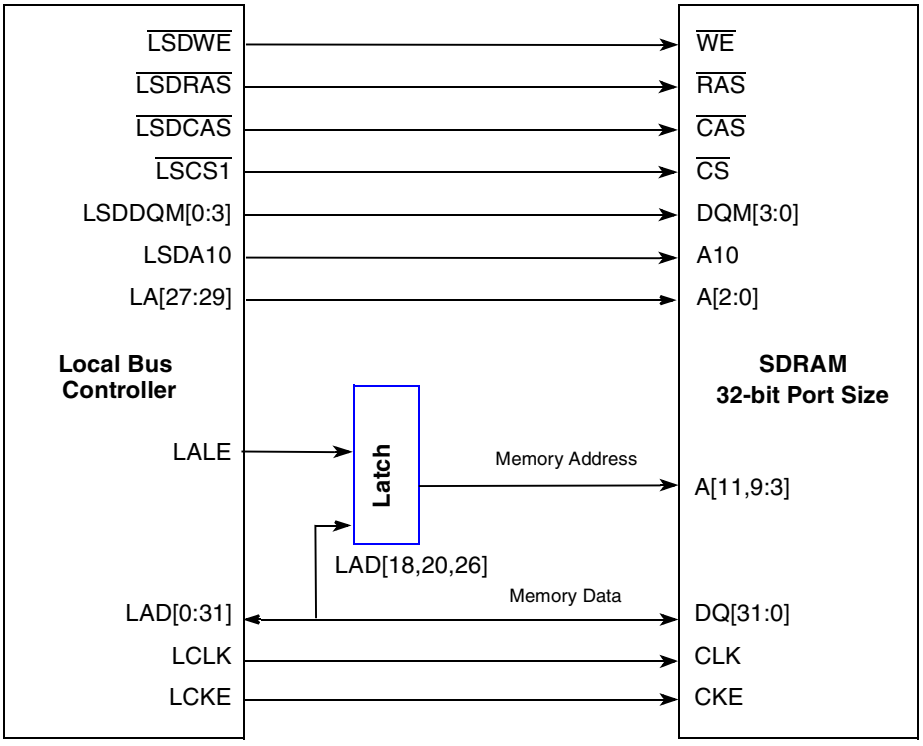

Figure 5. Local Bus Connection to SDRAM

6.5.1 Termination of Local Bus Signals during Normal Operation

A pull-up on the $\overline{\text{LGTA}}$ signal is recommended. Please see the device errata for more information. It is recommended to verify signal integrity by simulating with the current IBIS model.

6.5.2 Termination of Unused Local Bus Signals

Termination is not needed on output signals. For bidirectional I/Os, tie signals high or low though a resistor. Recommended resistor values are 2–10 kΩ. For inputs, tie signals to their inactive state through a resistor. Recommended resistor values are 2–10 kΩ.

6.5.3 Timing

Local bus output valid, hold and tri-state timings can be adjusted at reset by the POR pins TSEC2_TXD[6:5]. These pins directly affect local bus AC-timing by adding up to three buffer delays to the output path. The default configuration is a single buffer delay. Fewer buffer delays are needed in cases where the connection is to a faster external device.

In the case of the address latch hold time t_{LBOTOT}, the LBCR[AHD] bit is used to further adjust t_{LBOTOT}. It removes part of the hold time for LAD with respect to LALE in order to lengthen the LALE pulse. It can remove either a half or a full CCB clock period. Table 9 describes how t_{LBOTOT} is programmed.

Table 9. Programming t_{LBOTOT}

LBCR[AHD]	TSEC2_TXD[6:5]	t_{LBOTOT}
0	00	CCBCLK
0	01	CCBCLK + 3BDs
0	10	CCBCLK + 2BDs
0	11	CCBCLK + 1BD
1	00	CCBCLK/2
1	01	CCBCLK/2 + 3BDs
1	10	CCBCLK/2 + 2BDs
1	11	CCBCLK/2 + 1BD

6.6 PCI and PCI-X

6.6.1 Termination of PCI Signals During Normal Operation

It is recommended to verify signal integrity by simulating with the current IBIS model. For standard operation of the PCI port, pull-ups are necessary to guarantee the state of control signals when no agent is driving the bus. The PCI local bus specification requires a pull-up on the $\overline{\text{PCI\_FRAME}}$, $\overline{\text{PCI\_TRDY}}$, $\overline{\text{PCI\_IRDY}}$, $\overline{\text{PCI\_DEVSEL}}$, $\overline{\text{PCI\_STOP}}$, $\overline{\text{PCI\_SERR}}$, $\overline{\text{PCI\_PERR}}$, $\overline{\text{PCI\_REQ64}}$, and $\overline{\text{PCI\_ACK64}}$ pins. Weak pull-ups of 2–10 KΩ are recommended for these pins.

When in 32-bit PCI mode the PowerQUICC III enables weak internal pull-ups on PCI_AD[63:32], $\overline{\text{PCI\_C\_BE}}$[7:4], and PCI_PAR64. These internal pull-ups are not enabled in 64-bit mode. If there is concern that in 32-bit mode these inputs may see noise that would cause unwanted power consumption, external pull-up resistors may be placed on them to further guarantee their logic-one state when in 32-bit mode.

The $\overline{\text{PCI\_REQ64}}$ pin functionally requires a pull-up resistor according to the PCI local bus specification; however, during reset it is a configuration input for PowerQUICC III that determines 32- or 64-bit PCI operation. If the PowerQUICC III is to be configured as a 64-bit PCI device, it must be actively driven low during reset by reset logic. Because PowerQUICC III does not implement an override to this specified protocol for selecting 64-bit operation, the signal would have to be driven low with a driver that can be released to high impedance or similar logic during reset, and then release it to select 64-bit PCI operation.

If the PowerQUICC III is the host which initiates PCI transactions, it is recommended to pull the IDSEL pin low. This will guard against the PowerQUICC III replying to one of its own bus transactions.

6.6.2 Termination of Unused PCI Signals

Termination is not needed on output signals.

For bidirectional I/Os, tie signals high or low though a resistor. Recommended resistor values are 2–10 kΩ. If the PCI arbiter is disabled by the power-on reset configuration settings, these signals may be tied together to a common resistor.

If the PCI interface is used in 32-bit mode, PCI_AD[63:32] should be left floating. No termination is needed.

For inputs, tie signals to their inactive state through a resistor. Recommended resistor values are 2–10 kΩ.

6.6.3 Specific PCI Pin Usage

The PowerQUICC III does not implement for the PCI interface specific CLK and $\overline{\text{RST}}$ pins separate from the rest of the device pins. Instead, the PCI CLK is realized on the SYSCLK input, and the PCI $\overline{\text{RST}}$ is realized on the $\overline{\text{HRESET}}$ input.

6.7 RapidIO

6.7.1 Termination of RapidIO Signals During Normal Operation

The PowerQUICC III family of devices does meet the RapidIO specification of having source termination within the driver and differential termination within the receiver. Hence, no additional termination is required external to the device.

6.7.2 Termination of Unused RapidIO Signals

If the system application does not utilize the RapidIO bus interface, it is recommended that all of the RapidIO receivers have between 0.5 and 0.6 V across each differential pair. Examples of how this can be

achieved, taking advantage of the 100 Ω differential termination within the receivers, are shown in Figure 6.

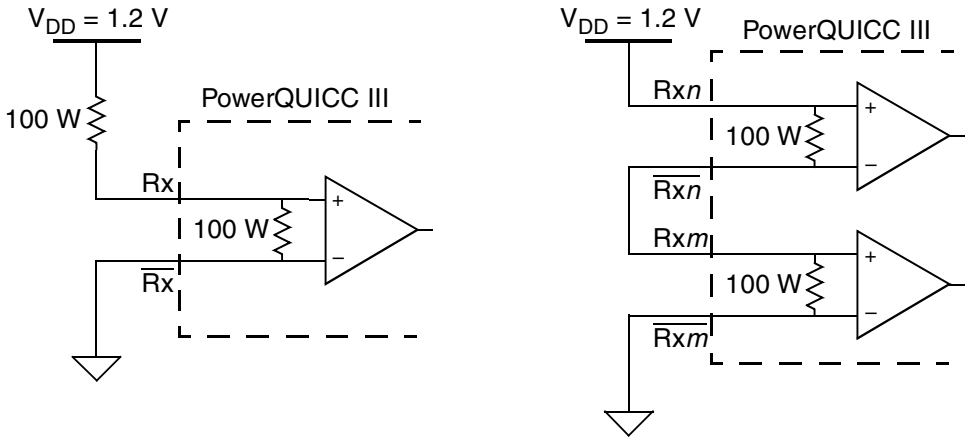

Figure 6. Examples of Terminating an Unused RapidIO Receiver

In the above examples, 0.6 V would be applied across the differential receiver pairs. These are not intended to be recommendations, only examples. Another existing on-board power supply with either an appropriate external resistor or another receiver in a daisy-chain configuration would suffice, for example.

In addition, the device RapidIO controller should then be disabled in software by setting the DEVDISR[RIO] bit to a value of 1. This turns off the clock to the RapidIO controller.

6.7.3 Transmit Clock Options

As referenced in Table 7, the source of the RapidIO transmit clock can be configured at $\overline{\text{HRESET}}$. The three options for the source of the transmit clock are the CCB clock, the RapidIO receive clock, and an external clock source. The receive clock option should not be used in normal operation of the RapidIO port; however, it may be useful in debugging the port itself. If the CCB clock frequency is the desired transmit clock frequency, then the default configurations can be used to select this option; otherwise an external clock source can be input to the PowerQUICC III on the RIO_TX_CLK_IN/$\overline{\text{RIO\_TX\_CLK\_IN}}$ pins at the desired frequency.

While the PowerQUICC III hardware specification quote only AC timings for 500 Mbps, 750 Mbps and 1 Gbps data rates, the RapidIO controller can be run at slower speeds.

6.8 Three Speed Ethernet Controller (TSEC)

6.8.1 Management Interface

The TSEC has one management interface that controls all external PHYs. The management interface of TSEC1 controls the TBI PHY from TSEC1 as well as all external PHYs. The management interface of TSEC2, shown in Figure 7 below, controls the TBI PHY from TSEC2 only.

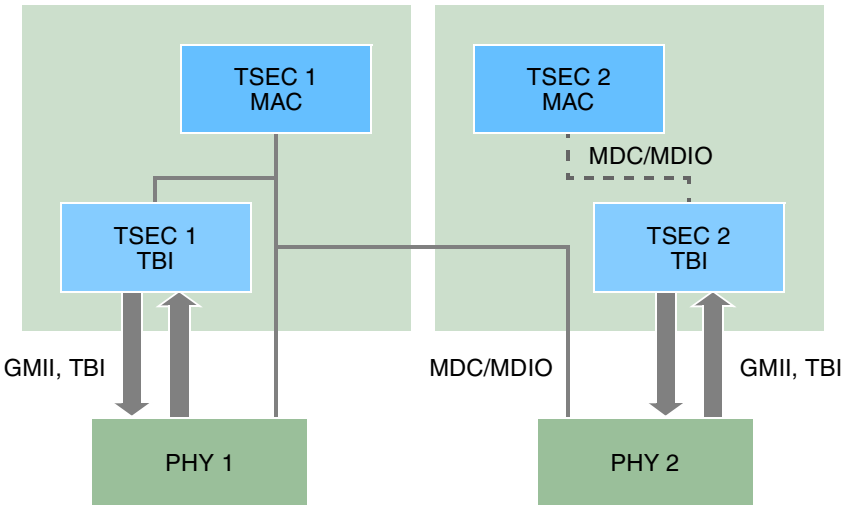

Figure 7. TSEC Management Interface

6.8.2 Graceful Stop

The TSEC interfaces must be properly stopped by the graceful stop mechanism. Stopping the transmit and receive buffers without using graceful stop can yield unpredictable results. The processor needs to first gracefully stop the transmitter by setting the DMACTL[GTS] bit and confirming that it has been completed by polling the IEVENT [GTSC] bit. Only then should the transmitter be disabled by clearing the MACCFG1[TxEN] bit.

For the TSEC receive, first turn off the receiver to prevent any additional data from coming in. Then the graceful stop should be enabled by setting the DMACTL[GRS] bit. Wait for confirmation by polling the IEVENT[GRSC] bit.

6.8.3 Termination of TSEC Signals During Normal Operation

It is recommended that the signal integrity be verify by simulating with the current IBIS model.

6.8.4 Termination of Unused TSEC Signals

Termination is not needed on output signals. For I/Os, tie signals high or low through a resistor. Recommended resistor values are 2–10 kΩ. For inputs, tie signals to their inactive state through a resistor; clock inputs may be tied high or low. Recommended resistor values are 2–10 kΩ.

6.9 Termination Summary for Unused Signals

Table 10 summarizes the recommended terminations for unused interfaces or unused pins. Termination is not need on outputs, only inputs. Suggested resistor values are between 2–10 KΩ. In general, inputs may be tied together to a single resistor. I/O's must be tied off with a single resistor per I/O except on the PCI interface. See Section 6.6, "PCI and PCI-X."

Note that if the local bus or the TSEC are not being used, the appropriate power-on reset signals must be configured for these interfaces. However, these particular power-on reset pull-ups and pull-downs can be left during normal operation because the interfaces are not used.

Table 10. Termination of Unused Signals Summary

Block	Termination Needed on Unused Inputs	Exceptions
CPM	If Port A–D pins are not re-programmed as outputs, then: Tie I/Os High or Low through resistor Tie inputs to inactive state through resistor	—
DDR	Tie pins High or Low through resistor	—
I^2C	Tie pins High through resistor	—
PCI, PCI-X	Tie I/Os High or Low through resistor Tie inputs to inactive state through resistor	POR pins $\overline{\text{PCI\_GNT}}[1:4]$, and $\overline{\text{PCI\_REQ64}}$
RapidIO	NONE needed: Source terminated within driver	—
TSEC	Tie I/Os High or Low through resistor Tie inputs to inactive state through resistor	POR pins TSEC1_TXD[4:7], TSEC2_TXD[2:7]; manufacturing test pins TSEC1_TXD[0:3]
Local Bus	Tie I/Os High or Low through resistor Tie inputs to inactive state through resistor	POR pins LA[27:31], LALE, LGPL[0:3], LGPL5, LWE[0:3]

7 Documentation History

Table 11 provides a revision history for this application note.

Table 11. Document Revision History

Rev. Number	Date	Changes
1	06/2010	Modified Section 2.3, "Power Sequencing."
0.1	10/2004	• Added note to Section 2.3, "Power Sequencing" • Updated Figure 3 in Section 4.1, "TRST" • Corrected $\overline{\text{HRESET}}$ assertion time in Section 5.1, "Configurable Options" • Updated Section 6.3.2, "Termination of Unused DDR Signals" • Revised Section 6.7.2, "Termination of Unused RapidIO Signals" • Updated Section 6.8.4, "Termination of Unused TSEC Signals"
0	08/2004	Initial release

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