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Connecting the i.MX to a Hard Drive

MC9328MX1, MC9328MXL,MC9328MXS and MC9328MX21

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1 Abstract

Consumer electronics products require an increasing amount of capacity to store digital content. This is especially true for applications that the MC9328MX1 and MC9328MXL, MC9328MXS, (i.MX1/L/S) processors address, such as:

- Digital video players/recorders
- Video game consoles
- Portable digital audio players
- Multimedia portable players

The goal of this document is to present the best solution to connect a standard ATA Hard Disk Drive to the i.MX processors. A full description of the different standards for Hard Disk Drives is found in the Appendices. Within the appendices, the discussion justifies the choice of the most commonly used ATA standard.

Despite the dedicated PCMCIA/CF controller of the MC9328MX21 (i.MX21), this application note provides an alternative to the PCMCIA/CF controller. As the External Interface Module (EIM) is similar for the entire

Contents

1 Abstract 1
2 Connecting a Hard Drive to i.MX1/L 3
3 i.MX1/L Configuration and ATA Hard Drive Timing Requirements 4
4 EIM Configuration 7
5 Physical Connection and Interface 8
6 Software Aspect 12
Appendix A: SODIMM Daughter Board Schematic 16
Appendix B: Standards for Hard Disk Devices . . 18
Appendix C: Connection Issues Summary 25
Appendix D: Other Modes of Read/Write Operations 27
Appendix E: Glossary 28
7 References 31

i.MX processor family, the primary changes are within the memory map and GPIO configurations.

1.1 Different Hard Disk Standards for Different Applications

Table 1 and Table 2 provide a comparison of the hard disk standards discussed in this document.

Table 1. Hard Disk Standards

Hard Disk Standards	Maximum Transfer Rate	Voltage	Applications
HDD (ATA)	100 Mbytes/s	3.3V, 5V, or 5V and 12V	Mass storage for embedded applications or common PC.
HDD (SATA)	600 Mbytes/s (planned)	3.3V, 5V, or 5V and 12V	Mass storage for embedded applications or common PC.
HDD (SCSI)	640 Mbytes/s	5V	Mass storage for servers and area networks.
Microdrive (CompactFlash)	16.7 Mbytes/s	3.3V or 5V	Removable mass storage for handheld devices with low-power—PDA, digital camera.
PC Card ATA (PCMCIA)	20 Mbytes/s	3.3V or 5V	Removable mass storage with low-power primarily notebooks.

Table 2. Comparison of Several Hard Disks Features (Q2, 2004)

Type	Disk size	Capacity (up-to)	Price in $/Gbyte	Manufacturers
HDD (ATA and SATA)	3.5"	300 Gbyte	1 $/Gbyte	Toshiba, Hitachi, Seagate Western Digital, Maxtor
	2.5"	80 Gbyte	4 $/Gbyte	Hitachi, Fujitsu
	1.8"	40 Gbyte	7 $/Gbyte	Toshiba, Hitachi
HDD (SCSI)	3.5"	150 Gbyte	6 $/Gbyte	IBM, Western Digital, Seagate, Acer, Fujitsu, Maxtor
Microdrive	1.0"	4 Gbyte	100 $/Gbyte	IBM, Hitachi
PC Card ATA	1.0"	5 Gbyte	70 $/Gbyte	Kingston, HP

1.2 Standard Summary

Only the ATA standard includes the required features to optimize use with the i.MX1/L/S processor—that is:

- Low cost
- Small physical size
- Large storage capacity
- Low-powered

Table 3. Standards Summary

Standard	Low Cost Units (< 10 $/Gbyte)	Small Size Units (< 2.5")	Large Capacity Units (> 10 Gbyte)	Low-Power Consumption (< 5 V)	Available
SCSI	No	No	Yes	No	Yes
SATA	Yes	Yes	Yes	Yes	No
ATA	Yes	Yes	Yes	Yes	Yes
CE-ATA	Yes	Yes	Yes	Yes	No
CompactFlash	No	Yes	No	Yes	Yes
PCMCIA	No	Yes	No	Yes	Yes

2 Connecting a Hard Drive to i.MX1/L/S

Three main standards of ATA hard drives are available. Only the common ATA drive is considered in this application note (See Appendices).

2.1 Connecting a PC ATA Card (PC Card Standard)

The application note: *PCMCIA and Compact Flash Interface for the MC9328MX1 and MC9328MXL Application Processors* (order number AN2417/D), also describes the implementation of a PCMCIA interface on an i.MX1/L/S processor application development system. This is the simplest way to connect PC ATA card device or Microdrives (with a PCMCIA adapter) to a i.MX1/L/S processor, however, software and hardware issues must be tested and validated on a real implementation. The PCMCIA bus does not support TrueIDE and ATA modes.

The scope of this paper is to present the best hard drive solution to connect i.MX processors (c.f. 4.7 Standard summary), which are ATA drives, therefore, a PC ATA card solution is not analyzed further in this document.

2.2 Connecting Microdrive (CompactFlash Standard)

Application note AN2417 gives a description of a hardware connection between a CompactFlash and the i.MX1/L/S processor. Memory and I/O modes are supported therefore a Microdrive can be connected in I/O mode to the i.MX1/L/S processor. Software and hardware issues must be tested and validated on a real implementation. TrueIDE is not implemented, however, PIO 0 transfer timings are the same as I/O mode transfer timings, therefore software glue TrueIDE mode for PIO 0 must be available.

The scope of this paper is to present the best hard drive solution to connect i.MX processors (c.f. 4.7 Standard summary), which are ATA drives, therefore, the Microdrive solution is not analyzed further into this document.

2.3 Connecting an ATA Drive (ATA-4 and Above Standards)

There are five sizes for an ATA hard drive:

- 3.5"—Standard hard drive size for home personal computers. Electrical requirements (5 and 12 V) and dimensions are not adapted for embedded system.
- 2.5"—Standard hard drive size for notebook computers. Electrical requirements (3.3 V) are adapted for embedded system, however, dimensions are not acceptable.
- 1.8"—New hard drive generation for embedded systems. This is actually the best choice for small and low-power consumption system (3.3 V power supplied). The hard drive that is to be tested and certified for connection to the i.MX1/L/S processor is the Toshiba MK2004GAL.
- 1"—Hard drive inside Microdrive CompactFlash card.
- 0.85"—This is the future for embedded systems. Currently, the maximum size of the drive is approximately 2–3 Gbyte, and they are expected to be used in cell phones as well as other mobile devices. The drives will be ready for sale in 2005 to OEM manufacturers.

As the i.MX1/L/S processor targets low-power embedded applications, a hard drive in 0.85", 1", or 1.8" is suitable. Referring to the details given previously, and from a cost and capacity effectiveness, a 1.8" size hard drive remains the best choice.

3 i.MX1/L/S Configuration and ATA Hard Drive Timing Requirements

In this section we describe the hardware and driver development with a Toshiba MK2004GAL hard drive.

The ATA standard specifies several input and output modes. These operations need different timings and signals to be performed. The following sections only describe the PIO mode used to communicate between the i.MX1/L/S processor and the hard disc. Multiword DMA and UDMA modes are available in the Section Appendix D, “Other Modes of Read/Write Operationson page 27.

3.1 Read/Write Operations in PIO Mode

PIO operations are performed by the system CPU—that is, the i.MX1/L/S processor; the i.MX1/L/S processor must execute the instructions that transfer the data to and from the drive. This is the first mode that is going to be implemented on the i.MX1/L/S processor as it is the most simple. The i.MX1/L/S processor’s EIM ensures compliant timings with this mode without external glue logic adaptation.

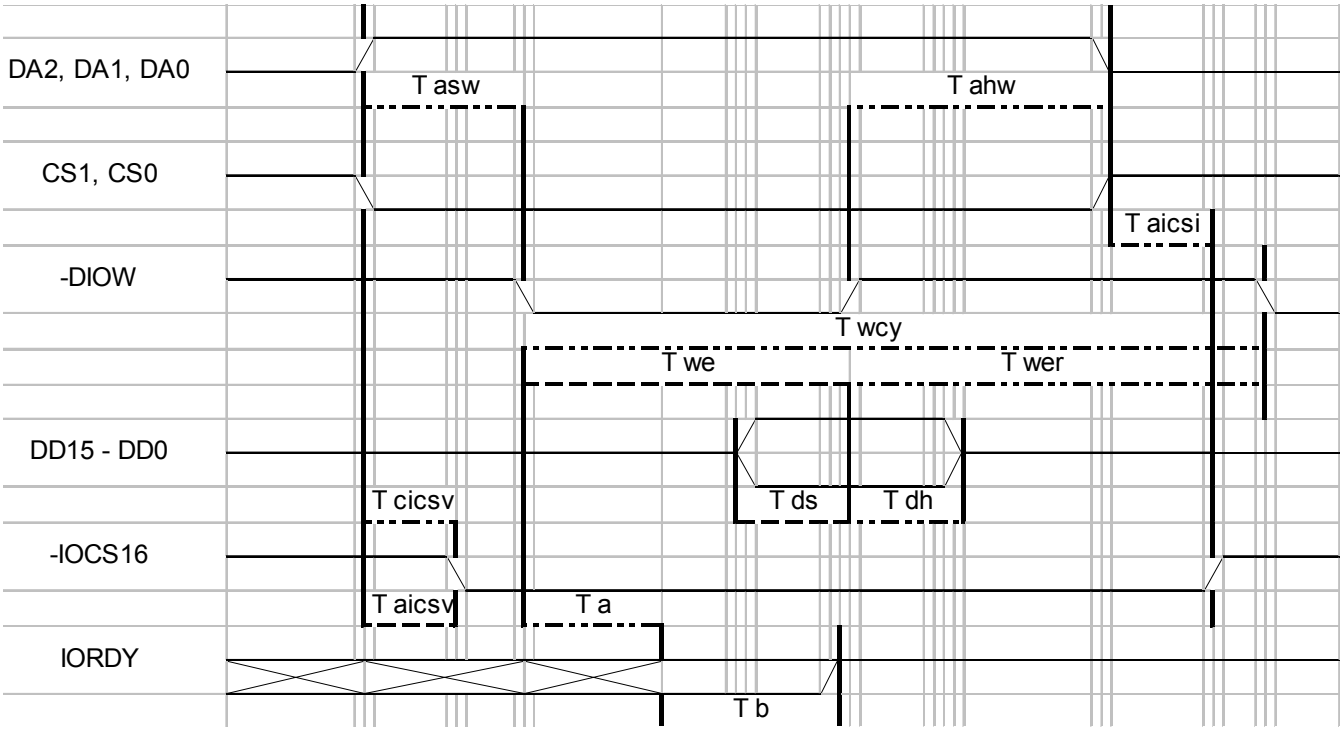

Figure 1. PIO Hard Drive Write Cycle

Table 4. PIO Write Operation Timings for Hard Drive

			PIO Transfert mode				
Symbol	Meaning	min / max ns	0	1	2	3	4
T asw	Address setup to -DOW Low	min	70	50	30	30	25
T ds	Data setup to -DOW High	min	60	45	30	30	20
T w e	-DOW pulse w idth	min	165	125	100	80	70
T dh	Data hold from -DOW high	min	30	20	15	10	10
T ahw	ADDR hold from -DOW high	min	20	15	10	10	10
T w er	-DOW inactive	min	none	none	none	70	25
T w cy	Write cycle time	min	600	383	240	180	120
T cicsv	-IOCS16 valid from -CS	max	90	50	40	NOT USED	NOT USED
T aicsv	-IOCS16 valid from address	max	90	50	40	NOT USED	NOT USED
T aicsi	-IOCS16 inactive from address	max	60	45	30	NOT USED	NOT USED
T a	IORDY setup time	max	35	35	35	35	35
T b	IORDY pulse w idth	max	1250	1250	1250	1250	1250

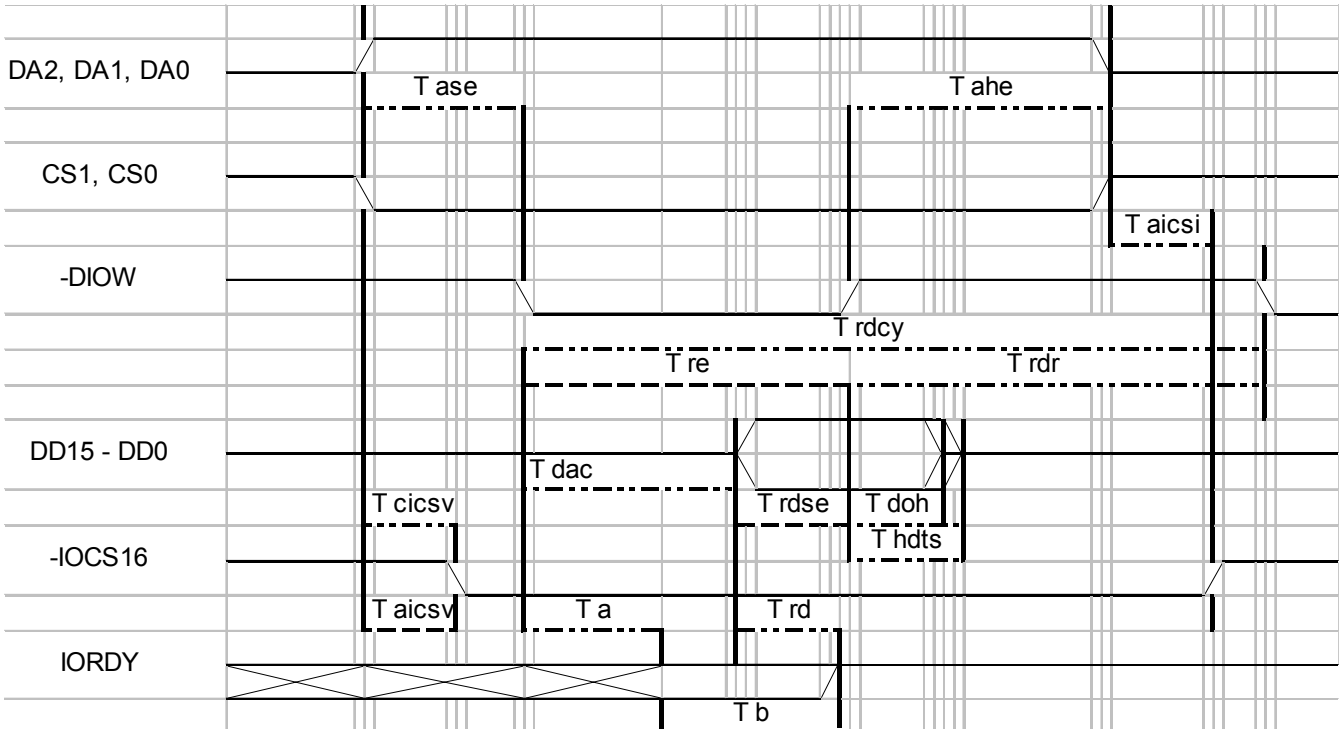

Figure 2. PIO Hard Drive Read Cycle

Table 5. PIO Read Operation Timings for Hard Drive

			PIO Transfert mode				
Symbol	Meaning	min / max ns	0	1	2	3	4
T ase	Address setup to -DIOR Low	min	70	50	30	30	25
T re	-DIOR pulse w idth	min	165	125	100	80	70
T rdse	-DIOR data setup	min	50	35	20	20	20
T doh	Data hold from -DIOR high	min	5	5	5	5	5
T hdts	Data tri-state from -DIOR high	max	30	30	30	30	30
T ahe	ADDR hold from -DIOR high	min	20	15	10	10	10
T rdr	-DIOR inactive	min	none	none	none	70	25
T rdcy	Read cycle time	min	600	383	240	180	120
T cicsv	-IOCS16 valid from -CS	max	90	50	40	NOT USED	NOT USED
T aicsv	-IOCS16 valid from address	max	90	50	40	NOT USED	NOT USED
T aicsi	-IOCS16 inactive from address	max	60	45	30	NOT USED	NOT USED
T rd	Read data valid to IORDY	min	0	0	0	0	0
T a	IORDY setup time	max	35	35	35	35	35
T b	IORDY pulse w idth	max	1250	1250	1250	1250	1250

Note: Multiword DMA mode is described in the Appendix D, “Other Modes of Read/Write Operations.

4 EIM Configuration

The i.MX1/L/S processor's External Interface Module can be configured to ensure correct ATA timings. Two registers are involved in this configuration. Physically, OE signal is used for read operation cycles and EB3 signal is used for write operation cycles (c.f. 6.5 Connection issues for ATA drive).

The calculations for the different signal settings are based on a clock cycle of 10.4 ns corresponding to the maximum bus frequency of 96 MHz. The timings defined above are also used as a reference for the specified timings.

Figure 3 shows the different timings that must be calculated to match the ATA PIO 4 mode timings.

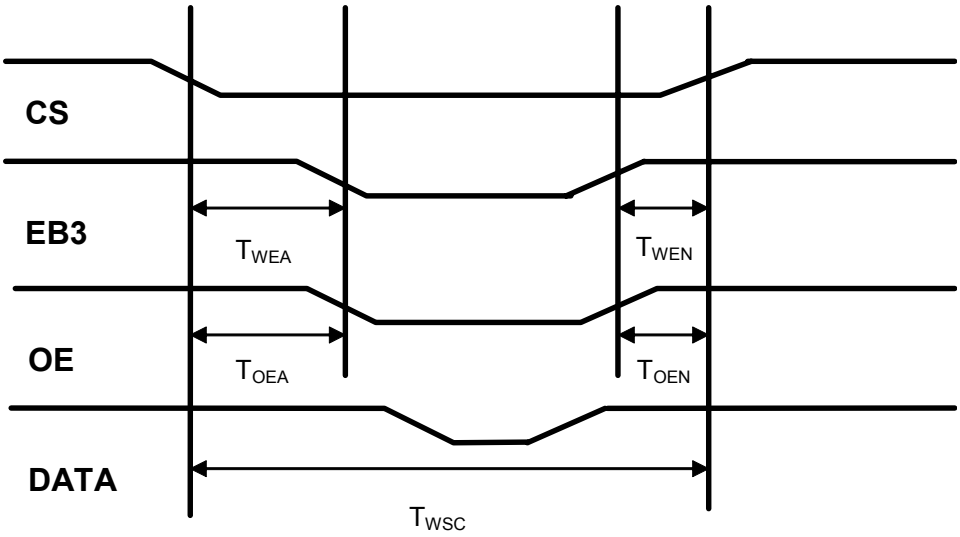

Figure 3. EIM Register Fields

Each of the i.MX chip selects can be customized for many parameters—such as timing, bus size, mode, protection, and so on. Most of the parameters can be dismissed, and kept at their default values—that is, no protection, synchronous functions, and the bus at 16-bit width.

To comply with the ATA standard PI04, the EIM controls five timing parameters that are calculated as follows: (See also the respective register in the i.MX reference manual.)

EIM_CS5H (Chip Select 5 Upper Control Register) = **0xB00** (field WSC):

- Field WSC (Wait State Control): permit to control the CS5 assertion time.

$T_{WSC} = T_{WE} + T_{ASW} + T_{AHW} = T_{RE} + T_{ASE} + T_{AHE}$ = 70ns + 25ns + 10ns = 105ns ≥ 12 clock cycles including a margin ≥ WSC = 0xB

EIM_CS5L (Chip Select 5 Lower Control Register) = **0x63630D01** (fields WEN, WEA, OEN, OEA):

- Field OEA (OE signal Assert): to determine when OE is asserted during read cycle.

$T_{OEA} = T_{ASE}$ = 25ns ≥ 6 half clock cycles including a margin ≥ OEA = 0x6

- Field OEN (OE signal Negate): to determine when OE is negated during read cycle.

$T_{OEN} = T_{AHE}$ = 10ns ≥ 3 half clock cycles including a margin ≥ OEN = 0x3

- Field WEA (EBx signals Assert): to determine when EBx are asserted during write cycle.

$T_{WEA} = T_{ASW}$ = 25ns ≥ 6 half clock cycles including a margin ≥ WEA = 0x6

- Field WEN (EBx signals Negate): to determine when EBx are negated during write cycle.

$T_{WEN} = T_{AHW}$ = 10ns ≥ 3 half clock cycles including a margin ≥ WEN = 0x3

CSCR (Clock Source Control Register) **= 0x2F008003** (field BCLK_DIV)

- Field BLCK_DIV (BClock divider): To ensure maximum clock speed, BCLK is divided by 1.

NOTE

For optimal connection, the user should recalculate the previous values according to its system BCLK.

5 Physical Connection and Interface

5.1 i.MX1/L/S to Hard Drive Pin Mapping

Table 6 describes the connections between the i.MX1/L/S processor's External Interface Module and the ATA device.

Table 6. ATA Hard Drive Direct Connections to i.MX1/L/S Summary

PIN	HDD	i.MX1/L/S	Function	Direction of Signal for the Device
1	$\overline{\text{RESET}}$	GPIO PB 17	Reset signal from the host system; it shall be active low when system is powered-up or when voltage fault is detected.	I
2	Ground	Ground	Ground.	X
3	DD7	D7	16 bit bidirectional data bus between the host system and the drive. All 16 bits are used for data transfer in the data register. The lower 8 bits, DD0–DD7, are used during register and ECC access.	I/O
4	DD8	D8	–	–
5	DD6	D6	–	–
6	DD9	D9	–	–
7	DD5	D5	–	–
8	DD10	D10	–	–
9	DD4	D4	–	–
10	DD11	D11	–	–
11	DD3	D3	–	–
12	DD12	D12	–	–
13	DD2	D2	–	–
14	DD13	D13	–	–

Table 6. ATA Hard Drive Direct Connections to i.MX1/L/S Summary (continued)

PIN	HDD	i.MX1/L/S	Function	Direction of Signal for the Device
15	DD1	D1	–	–
16	DD14	D14	–	–
17	DD0	D0	–	–
18	DD15	D15	–	–
19	Ground	Ground	Ground.	X
20	OPEN	NOT USED	Pin position 20 has no connection pin, clipped on the drive and plugged on the cable to ensure correct orientation of the cable and avoid wrong insertion.	X
21	DMARQ	DMA REQ	DMA request signal is set by the drive to indicate that the DMA data transfer is ready. The direction of the data transfer is controlled by $\overline{\text{DIOR}}$/$\overline{\text{DIOW}}$ strobe signal. This signal is used to handshake with $\overline{\text{DMACK}}$.	O
22	Ground	Ground	Ground.	X
23	$\overline{\text{DIOW}}$	$\overline{\text{EB3}}$	Write strobe. The rising clock data from the host data bus, DD0–DD15 to a register or data register of the drive.	I
24	Ground	Ground	Ground.	X
25	$\overline{\text{DIOR}}$	$\overline{\text{OE}}$	Read strobe. When active low, this signal enables data from a register or the data of the drive onto the host data bus, DD0 through DD15. The rising edge of $\overline{\text{DIOR}}$ latches on the data on the bus from the drive.	I
26	Ground	Ground	Ground.	X
27	IORDY	NOT USED	This signal reports to the host that the bus is available.	O
28	CSEL	Ground	When grounded, the drive recognizes itself as a Master.	I
29	$\overline{\text{DMACK}}$	PULL DOWN	Responding to DMARQ, this signal indicates that the host is ready to receive or send the data in DMA mode.	I
30	Ground	Ground	Ground.	X
31	INTRQ	GPIO PA 18	Interrupt to the host system, enabled only when the drive is selected and the host activates the $\overline{\text{EN}}$ bit in the Device Control register. When the $\overline{\text{IEN}}$ bit is inactive or the drive is not selected, this output is in a high impedance state, whether an interrupt is set or not. The interrupt is set when the IRQ bit is set by the drive CPU. IRQ is reset to zero when host reads the status register or a write to the command register or when DRQ is negated.	O
32	$\overline{\text{IOCS16}}$	NOT USED	Indication to the host system that the 16 bit data register has been addressed and that the drive is ready to send or receive a 16 bit data word (open drain)	O
33	DA1	A2	Address line from the host system to select the registers of the drive	I
34	$\overline{\text{PDIAG}}$	NOT USED	In Master/Slave mode, this signal reports the presence of slave drive to master drive and enable transmitting of diagnostic result between master drive and slave drive.	I/O

Table 6. ATA Hard Drive Direct Connections to i.MX1/L/S Summary (continued)

PIN	HDD	i.MX1/L/S	Function	Direction of Signal for the Device
35	DA0	A1	Address line from the host system to select the registers of the drive	I
36	DA2	A3	–	–
37	$\overline{CS0}$	A5	Chip select signal generated from the host address bus. This signal is used to select one of the two groups of host accessible registers.	I
38	$\overline{CS1}$	A4	–	–
39	$\overline{DASP}$	LED	This is a signal from the drive used either to drive an external LED whenever the drive is being accessed, or to report presence of the slave drive to the master when the drive is in master/slave mode.	O
40	Ground	Ground	Ground.	X
41	+ 3.3 V	Connect to Power Supply Circuit	Supply voltage	I
42	+ 3.3 V	Connect to Power Supply Circuit	Supply voltage	I
43	Ground	Ground	Ground.	X
44	RESERVED	NOT USED	Reserved for future use. No connection.	X

5.2 i.MX1/L/S ATA SODIMM Daughter Board

See Appendix A page 16 to compare the i.MX1/L/S processor's ATA daughter board schematic.

The ATA SODIMM reference design board, can be used to connect any ATA hard drive from a standard perspective. However, from a physical perspective, any hard drive can be connected using an adapted ribbon cable. Because there is no management of the master and slave typical in a PC, only one hard drive at a time should be used and physically connected.

In summary, acceptable connections:

- Any +5V I/O hard drive—that is, all common PC hard discs
- Any +3.3 V I/O hard drive—that is, consumer hard discs
- Ribbon cable with a 2 × 20 pins in 2.54 mm connector, any hard drive size—that is, 3.5", 1.8", …
- Using a dedicated connector any hard drive from the embedded 1.8 inch series from Toshiba (driver developed with the MK2004GAL, which is a 20 Gbyte disc)

5.2.1 Specific Signals Description

The following signals are used to connect an i.MX processor to a hard disk.

- CS5—All the signals need to be isolated when the drive is not accessed, that is why the CS5 is used to enable the tri-stated buffers.

- RW—Signal used to select the buffer direction. When using mono voltage buffers, this signal can be used directly. When using dual voltage buffers, refer to the component's specification to determine whether to invert this signal.
- OE—Signal used for DIOR, as the behavior is similar and it can be controlled in assertion and negation.
- EB3 or EB2—Signal used for DIOW, as the behavior is similar and it can be controlled in assertion and negation.
- A[3:1]—Address bus used for DA[2:0], as the EIM must be aligned to 16-bit words.
- A[5:4]—For CS0 and CS1 of the hard drive, that must act as address signal.
- DMARQ—Signal not used at this time, as the DMA request function as not been tested. Must be pulled down.
- RESET—Signal to reset the hard drive during boot up or protocol crash. Internal hard drive pull up.
- INTRQ—Signal used as an interrupt line from the hard drive. Must be pulled down.

5.2.2 Components Description

- U3, U4, U5—Dual voltage tri-state buffers (P/N=MC74LVXC3245): Isolates the hard drive when it is not used, so as not to disturb the rest of the system.
- U2—Triple inverter (P/N=NL37WZ04): Used as an inverter for RW (if dual voltage buffers are required) and DMARQ (not implemented, however, the DMA_REQ signal must be active low). The signal INTRQ uses the inverter as a level shifter, which avoids extraneous external components.
- VR1—Zener diode (P/N=MMSZ5223BT1): Prevents power up sequence issues for dual voltage buffers by simultaneously polarizing both sides of the buffers in case the two requested power supplies (on the ADS side and hard drive side) are not set at the same time. Not mandatory and can be dismissed with mono voltage buffers.
- VR2—Transil diode (P/N=1SMB5919BT3): Used to protect the global circuit from over voltages of an external power supply with too high voltage. Not required when caution is used in selecting the power supply. See Section 5.2.3, "Power Supply Requirements".
- U1—+3.3V linear voltage regulator (P/N=NCP1086ST-33T3): For voltage regulation if a higher than +3.3V power supply is used.
- R14 or R15—Shunt resistor: Allows selection of method used to supply the board and the hard drive. See Section 5.2.3, "Power Supply Requirements".
- LED D1—Displays hard drive activity.

5.2.3 Power Supply Requirements

The power supply must be plugged into a connector whose internal plug has a diameter of 1 or 1.3 mm. This internal plug is the VCC and external plug the ground.

- Using a +3.3V power supply—Only the R15 resistor is populated and R14 is not.

- Using a +5V power supply—Only the R15 resistor is populated and R14 is not if the hard drive works with under +5V. Only the R14 resistor is populated and R15 is not if the hard drive works under +3.3V (a regulator is used in this case).
- Using any other voltage power supply—If the transil diode is not used, as it protects the circuit from voltage higher than +5.6V, the board can use a multiple of voltages. The regulator has to be used in this case and the R14 resistor is populated and R15 is not, however only +3.3 V drives can be connected.

6 Software Aspect

6.1 Development Environment

To validate the hardware daughter board and to provide an interface to use the hard drive, the block device driver is required. Linux can support FAT, Ext2, and several others file systems. The file system management is completely handled by the operating system; the only software component missing for Linux is the hard drive driver. The purpose of the driver is to provide an interface to high-level functions and programs (such as primitive file system, shell commands) and to transform Linux kernel request into ATA commands.

The global environment to develop the block device driver is the following:

- GNU GCC crosstools chain for ARM9™ with:
  gcc 2.95.3 20010315 (release); permits user to compile the driver for the i.MX1/L/S processor
- Linux i.MX1/L/S kernel header 2.4.18; required to compile the driver
- i.MX1/L/S ADS with Linux operating system BSP 0.3.6 and linux kernel 2.4.18
- i.MX1/L/S ADS daughter board for ATA hard drive
- ATA hard drive

Linux driver programming requires advanced software knowledge (C.f. Linux device drivers 2nd edition, Alessandro RUBINI and Jonathan CORBET and driver listing).

Basically, only two operation modes are involved in ATA PIO protocol and must be programmed. These are:

- Read operations
- Write operations

This driver is ready to support partition table and classic hard drive operations. To resume, this driver implements:

- ATA PIO read operation
- ATA PIO write operation
- Interrupt mechanism
- Partition support

NOTE

The driver is available in the software package.

6.2 Driver Structure

The block device driver uses two sequences to make a read or a write command as illustrated in Figure 4 and Figure 5.

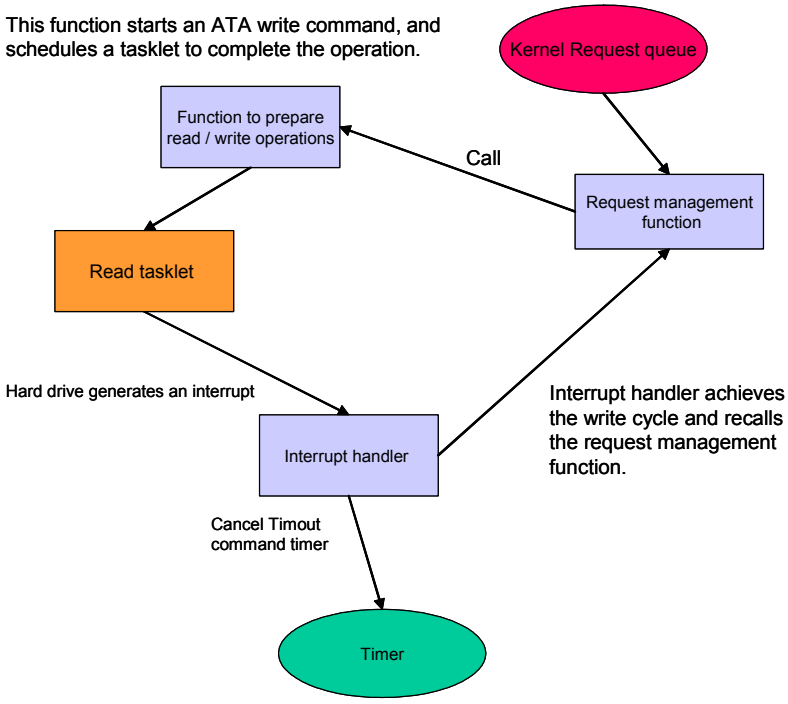

Figure 4. Driver Read Sequence

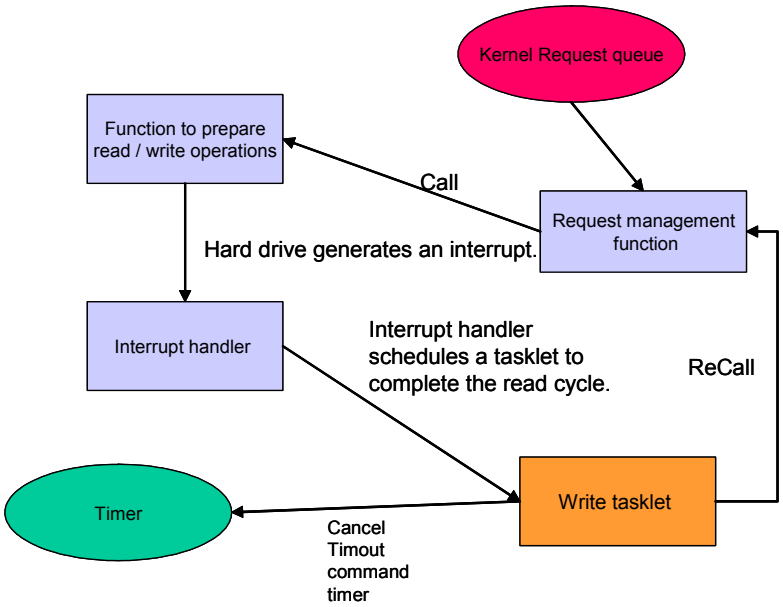

Figure 5. Driver Write Sequence

All functions in read and write sequences are the same (except for the tasklet). For more information, please refer to Section 7, "References."

6.3 Basic Commands to Start with a Hard Drive Under Linux

This section provides the instructions to start a PC hard drive using Linux.

6.3.1 Step 1: Driver Installation

The first step to use a hard drive with eLinux, is to install the driver that will initialize the communication with the drive, considering it as a module:

insmod hdd_driver_name.o (the available driver has developed under the name of mx1_IDE.o)

Many hard drives can be referenced by eLinux, using a devfs, and they will be found as following:

/dev/discs/disc0
/dev/discs/disc1
…

In the context of this application note, only one hard drive will be considered—that is, /dev/discs/disc0.

6.3.2 Step 2: Partition Creation

To use the space in a hard disk, it must be *partitioned*. Partitioning is the process of dividing the hard disk's space into chunks, so they can be prepared for use, or even dedicated to different uses. Even if the entire disk is intended to be used as a whole, it must be partitioned so that the operating system knows that it is intended to be used as a whole.

Primary, extended, and logical partitions:

- A maximum of four partitions can be placed on any hard disk. These are sometimes called primary partitions. The limitation of four partitions is imposed by the operating system according to the structure of the master boot record.
- One of the four partitions may be designated as an extended partition. This partition may then be subdivided into multiple logical partitions. This method allows two or more logical volumes to be placed on a single hard disk.

A software utility is commonly used: *fdisk* with the common usage:

../fdisk /dev/discs/disc0/disc

With this program, partitions are created, either primary or extended (+ logical partitions), and appear as:

/dev/discs/disc0/part1/part1
/dev/discs/disc0/part1/part2
…

6.3.3 Step 3: Partition Formatting

After the partitions are created, they must be formatted into a defined file system. Two options follow:

mke2fs /dev/discs/disc0/part1/part1(partition 1 is formatted into an ext2 file system)

or,

mkdosfs /dev/discs/disc0/part1/part1(partition 1 is formatted into an FAT file system)

6.3.4 Step 4: Mounting Partitions

As most devices, used under Linux, the hard drive must be mounted to be visible by a user:

mkdir /tmp/hdd0 (creates the mounting point if it does not exist under /mnt)

mount –t ext2 /dev/discs/disc1/part1 /tmp/hdd0(Partition 1 is linked to the mounting point as an ext2 file system. The default is "–t ext2", so it can be dismissed.)

or,

mount –t vfat /dev/discs/disc1/part1 /tmp/hdd0(partition 1 is linked to the mounting point as a FAT file system)

The hard drive is now accessible as a common directory at: /tmp/hdd.

6.3.5 Unmounting Partitions

When disconnecting the hard drive (for a shut down of the board, or during a long stop mode, …), the partitions must be unmounted as follows:

umount /tmp/hdd0

NOTE

Repair and integrity verification of the partitions can be checked, when unmounted, with the "e2fsck" command (for ext2) or dosfsck (for FAT).

Appendix A SODIMM Daughter Board Schematic

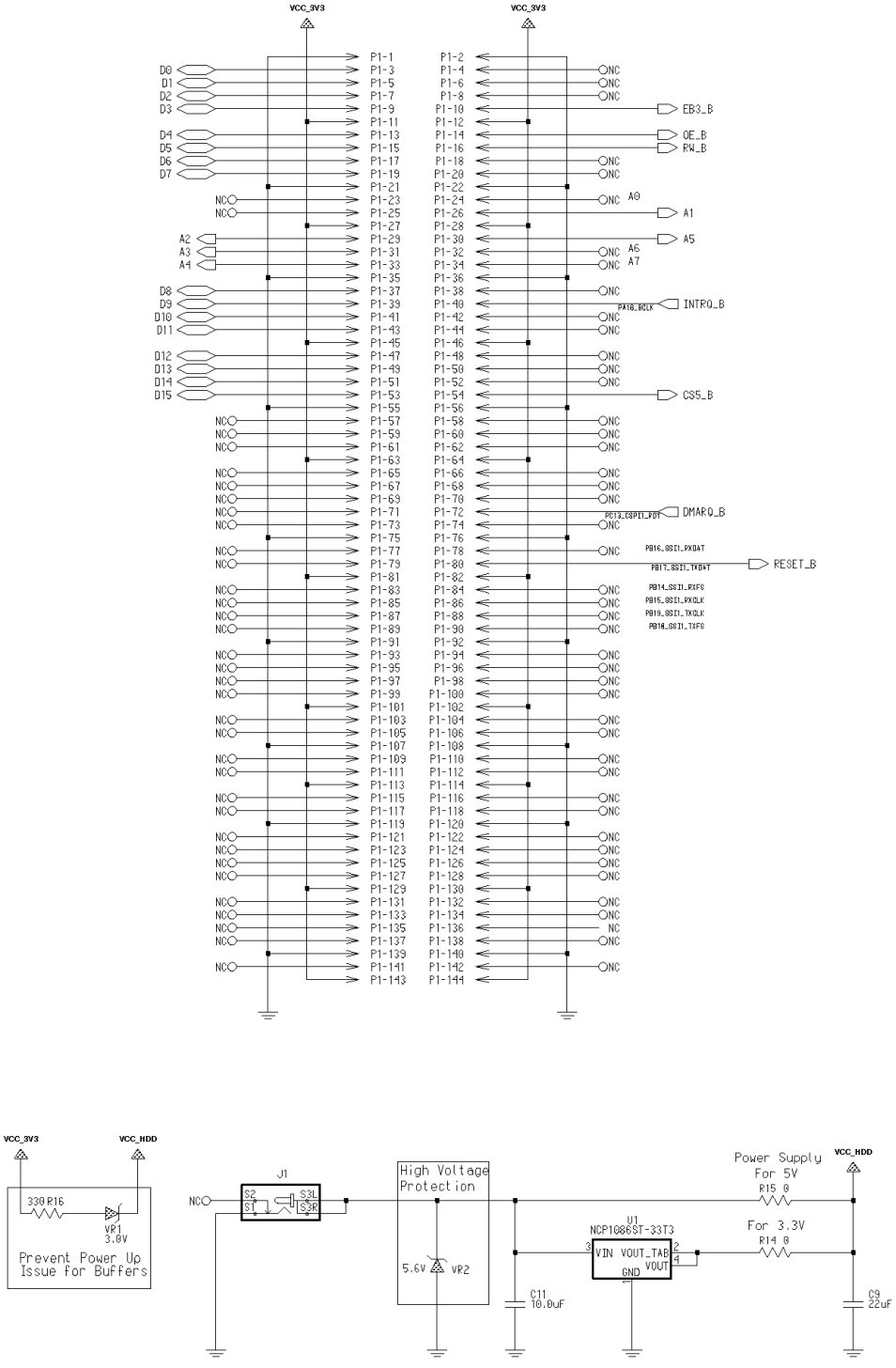

Figure 6. SODIMM HDD DB for i.MX1/L/S (Sheet 1 of 2)

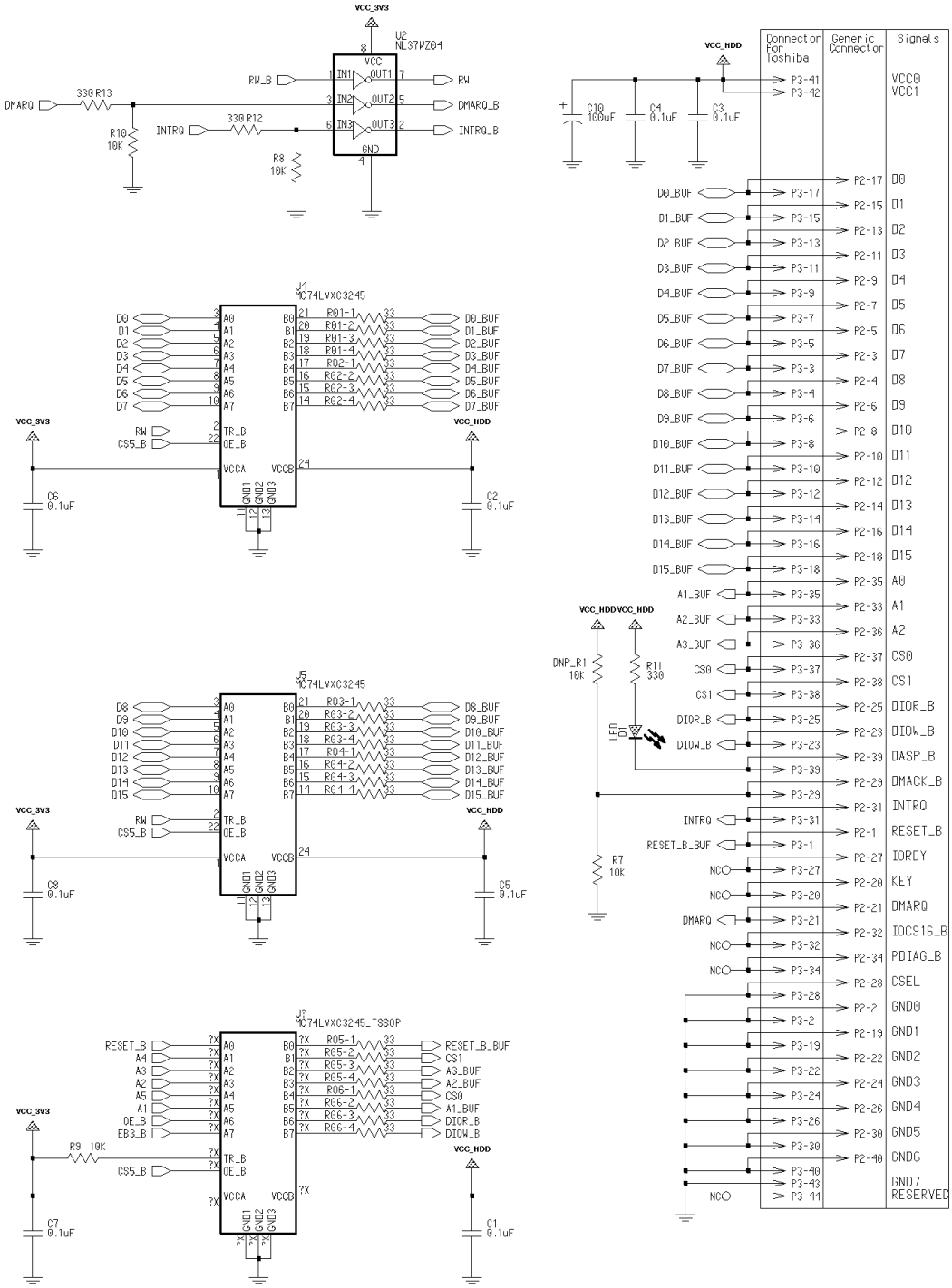

Figure 7. SODIMM HDD DB for i.MX1/L/S (Sheet 2 of 2)

Appendix B Standards for Hard Disk Devices

Small Computer System Interface Standard (SCSI)

SCSI interfaces provide for faster data transmission rates (up to 640 megabytes per second) than standard serial and parallel ports. In addition, you can attach many devices to a single SCSI port, therefore the SCSI is more of an I/O bus rather than simply an interface.

Although SCSI is an ANSI standard, there are many variations such that two SCSI interfaces may be incompatible. For example, SCSI supports several types of connectors.

The SCSI standard is not adapted for embedded environments (too fast, high cost, big unit size, high power consumption). As a consequence, this solution is not analyzed further in this document.

Advanced Technology Attachment Standard (ATA)

The ATA standard specifies the ATA interface between host systems and storage devices (typically for hard drives, CD-ROMs, and DVD-ROMs). It provides a common attachment interface for systems manufacturers, system integrators and software suppliers. The ATA standard has evolved over the years and the current version of this standard is ATA-6 (ATA-7 is in progress). These standards are backward compatible, and ATA-4 and above are the reference standards for the hard disk drives. ATA is the most widely used standard (Personal Computer market, work stations, and small server markets).

ATA standard defines several modes and communication speeds between the host and the device. Those modes are:

- PIO—Programmed Input/Output. This mandatory data transfer mode is performed by the host processor using accesses to Data registers. The maximum transfer rate using this mode is 16.7 Mbytes/s. This kind of transfer is managed directly by the CPU, therefore resource intensive.
- Singleword DMA—First DMA implementation. This mode is unreliable and not very powerful, therefore is not recommended.
- Multiword DMA—Data transfer protocol used with specific commands. It is specifically designed to exchange packets of data between the host memory and the hard disk drive. The maximum data transfer rate with this mode is 16.7 Mbytes/s.
- Ultra DMA—A mandatory data transfer protocol that uses the same commands as Multiword DMA. The maximum data transfer rate with this mode is 133 Mbytes/s. This is a very specific mode that uses the rising and falling transitions of the DSTROBE signal (double transition clocking) generated by the hard disk and bus mastering technology.

Table 7 on page 19 provides a summary of the ATA Standards and transfer protocols.

Table 7. ATA Standard Summary

Protocol		Standard	ATA-1	ATA-2	ATA-3	ATA-4	ATA-5	ATA-6	ATA-7
PIO Mode	0	3.3 MB/s	X	X	X	X	X	X	X
	1	5.2 MB/s	X	X	X	X	X	X	X
	2	8.3 MB/s	X	X	X	X	X	X	X
	3	11.1 MB/s		X	X	X	X	X	X
	4	16.7 MB/s		X	X	X	X	X	X
Singleword DMA Mode[1]	0	2.1 MB/S	X	X	X	X	X	X	X
	1	4.2 MB/s	X	X	X	X	X	X	X
	2	8.3 MB/s	X	X	X	X	X	X	X
Multiword DMA Mode	0	4.2 MB/S	X	X	X	X	X	X	X
	1	13.3 MB/s		X	X	X	X	X	X
	2	16.7 MB/s		X	X	X	X	X	X
Utra DMA Mode	0	16.7 MB/s				X	X	X	X
	1	25 MB/s				X	X	X	X
	2	33.3 MB/s				X	X	X	X
	3	44.4 MB/s					X	X	X
	4	66.7 MB/s					X	X	X
	5	100 MB/s						X	X
	6	133 MB/s							X

1 Singleword DMA is obsolete and is not necessary implemented in latest hard drive.

Table 8 for a definition of the terms and the commercial names of the ATA standard (for example, ATA-2 is referred to as Fast ATA).

Table 8. ATA Standards Additional Information

Standard	Introduced technologies	Commercial Name	Standard Status
ATA-1	+Master Slave issues	IDE	Obsolete
ATA-2	+LBA +Block transfers	E-IDE PIO Mode 3: • Fast ATA PIO Mode 4: • Fast ATA 2	Obsolete
ATA-3	+SMART +Secure lock	–	Obsolete
ATA-4	+ATAPI +CRC	Ultra DMA Mode 2 (33.3 Mbytes/s): • Ultra+ATA 33 • UDMA33	In use

Table 8. ATA Standards Additional Information (continued)

Standard	Introduced technologies	Commercial Name	Standard Status
ATA-5	+80 wire connector	Ultra DMA Mode 4 (66.7 Mbytes/s): • Ultra+ATA 66 • UDMA66	In use
ATA-6	+Extended LBA +Automatic Acoustic Management +CF compatibility	Ultra DMA Mode 5 (100 Mbytes/s): • Ultra+ATA 100 • UDMA100	In use
ATA-7	+Continuous read	Ultra DMA Mode 6 (133 Mbytes/s): • Ultra+ATA 133 • UDMA133	Under development

Consumer Electronics ATA Standard (CE – ATA, Planned for 2005)

This standard interface is for small form factor disk drives that address the requirements of the handheld and consumer electronics (CE) market segments, including low pin count, low voltage, power efficiency, cost effectiveness and integration efficiency.

CE-ATA is being developed separately from SATA because handheld and portable consumer applications do not have the same requirements for high interface transfer rates as mainstream computing, requiring instead modest transfer rates at maximum power efficiency.

The specification is scheduled to be completed in the first half of 2005. The first end products supporting the new technology could be available several months thereafter.

Currently, CE-ATA units are not available. As a consequence this solution is not analyzed further in this document.

Serial-ATA Standard (SATA)

The SATA specification is the latest generation of PC disk drive (hard drive, CD-ROM, and DVD-ROM) interface and will replace ATA protocol (2004–2006). However, several working groups like “T13” or “The SerialATA workgroup” that include Intel, Dell, Maxtor, and Seagate, developed SATA. Furthermore, there are small differences between the group specifications. SATA I specification v 1.0a has been published on July 2003 and “The SerialATA workgroup” is developing version 2.0.

Main features of SATA:

- Low voltage differential (500mv, +/- 125mv) signaling methods, which reduce induced noise.
- 1.5 GHz (SATA I) up to 6 Ghz (SATA III) bus frequency.
- Increased bus speed (150Mbytes/s-SATA I, 300Mbytes/s-SATA II, 600Mbytes/s-SATA III).
- 7 wires (4 data, 3 ground), point-to-point, one device per controller connection.
- One meter serial cable that is very thin and flexible.
- No master/slave issues.
- No shared bandwidth.
- Hot plugging.

- SATA designed to be transparent to host system software layer which allows existing OS, device driver and application to run without modification.
- Improved airflow (due to thin cable).

Hard drive manufacturers supply customers with half SATA 3.5" drives—that is, an ATA drive with a parallel to a serial bridge, with the exception of Seagate who provides full SATA hard drives.

SATA bus frequency is too high for a direct connection with the i.MX1/L/S processor and there is no controller able to provide differential signals with 125mv magnitude on the i.MX1/L/S processor. Therefore, a SATA controller is required between the i.MX1/L/S processor and the SATA device. As a consequence, this solution is not analyzed further in this document. However, analysis of the SATA bus electrical consumption may be useful because drive manufacturers indicate that SATA drives require less power than an ATA drive which implies better autonomy for embedded systems.

Currently, 2.5" and 1.8" SATA units are not available. As a consequence this solution is not analyzed further in this document.

CompactFlash Standard (for Microdrive)

CompactFlash is a standard for a new class of advanced, small lightweight, low-power mobile products. CompactFlash card devices use a 50 pins connector and have three communication protocols with hosts:

- Memory mode—In this mode, the host configures the card using the card information structure (CIS) and the configuration registers. Communication between the host and the card are conducted by the task file registers mapped in the 2-Kbyte window in the memory address space. Memory mode is faster than I/O mode.
- I/O mode—In the I/O mode, configuration is conducted in the same way as in the memory mode and the task file registers are mapped to the I/O address space.
- TrueIDE mode—True IDE mode has only an I/O address space, so no memory address space is available. The task file registers are assigned to the I/O address space and the configuration registers and card information structure (CIS) cannot be seen from the host.

NOTE

Memory and I/O modes are the same for both CompactFlash PCMCIA.

Microdrive is a type of CompactFlash card, which contains a hard disk drive inside. The protocol to access to this HDD is the TrueIDE mode, which is electrically compatible with the ATA standard. Microdrive hard disks are manufactured by IBM and Hitachi. Several others manufacturers also provide CompactFlash cards containing Flash memory inside and operate in TrueIDE mode. Microdrive cards have a greater capacity than common Flash cards.

Table 9. Differences between ATA-4 and CompactFlash TrueIDE Mode Standards

Features	ATA-4	CF TrueIDE
Connector	40-pin (needs a cable)	50-pin (no cable)
Signals	26 common and 2 dedicated to DMA transfers	26 common
Voltage	+3.3V or +5V (depending of the model)	+3.3V or +5V (both supported by each device)

Table 9. Differences between ATA-4 and CompactFlash TrueIDE Mode Standards (continued)

Features	ATA-4	CF TrueIDE
Modes	PIO (0, 1, 2, 3, 4) Multiword DMA (0, 1, 2) Ultra DMA (0, 1, 2)	PIO (0, 1, 2, 3, 4) Multiword DMA (0, 1, 2) Ultra DMA (0, 1, 2)
Maximum speed	33.3 Mbytes/s (16.7 Mbytes/s in PIO-4)	16.7 Mbytes/s theoretical (Between 3.3 and 13.3 Mbytes/s in real products)
Number of registers	9 (1 reserved for DMA transfers)	9
Commands	32 common and 15 specific (DMA, packet, removable devices)	32 common and 8 specific

PCMCIA Standard (PC Card ATA)

Difference between PC Card ATA and ATA standard:

PC Card ATA is a PCMCIA (Personal Computer Memory Card International Association) standard that specifically addresses data storage products. It combines the industry standard AT disk drive command set, registers and protocol with the PCMCIA interface registers and protocols. Together these standards define the PC Card ATA standard that is a technology independent interface. PC Card ATA is defined in the volume 7 of PC Card specification. This volume defines the standard method for incorporating an ATA mass storage protocol peripheral on a PC Card. The protocol is based on Memory and I/O modes (see 2.3 CompactFlash standard) defined into the other volumes of this standard. PC Card ATA can be plug into an ATA controller (and use True IDE protocol), however, an ATA drive cannot be directly connected to a PCMCIA slot.

Difference between PC Card ATA and CompactFlash Card:

CompactFlash is equivalent to a PC Card ATA from an electric perspective. CompactFlash cards can be inserted into PC Card Type II slots using a PCMCIA adapter. The primary differences between the two are card dimensions and the number of pins on the connector. The CompactFlash card uses a 50 pin connector while a PC Card ATA uses a 68 pin connector. Because both CompactFlash and PC Card ATA connectors use less than 50 signals, there is no reduction in features, therefore CompactFlash conforms to PCMCIA specifications. CompactFlash True IDE mode is not supported on a PCMCIA slot, however PCMCIA/CompactFlash memory mode and I/O mode protocols are the same.

Figure 8. Pin-Out Differences between PCMCIA ATA Card and CompactFlash Card

Pin Number	PC Card ATA	CompactFlash	Pin Number	PC Card ATA	CompactFlash
1	Ground	Ground	35	Ground	$\overline{\text{IOWR}}$
2	DD3	DD3	36	$\overline{\text{CD1}}$	$\overline{\text{WE}}$
3	DD4	DD4	37	DD11	$\overline{\text{RDY/BSY/IREQ}}$
4	DD5	DD5	38	DD12	VCC
5	DD6	DD6	39	DD13	$\overline{\text{CSEL}}$
6	DD7	DD7	40	DD14	$\overline{\text{VS2}}$
7	$\overline{\text{CE1}}$	$\overline{\text{CE1}}$	41	DD15	RESET
8	A10	A10	42	$\overline{\text{CE2}}$	$\overline{\text{WAIT}}$
9	$\overline{\text{OE}}$	$\overline{\text{OE}}$	43	$\overline{\text{VS1}}$	$\overline{\text{INPACK}}$
10	–	A9	44	IORD	$\overline{\text{REG}}$
11	A9	A8	45	IOWR	BVD2
12	A8	A7	46	–	BVD1
13	–	VCC	47	–	DD8
14	–	A6	48	–	DD9
15	$\overline{\text{WE}}$	A5	49	–	DD10

Figure 8. Pin-Out Differences between PCMCIA ATA Card and CompactFlash Card (continued)

Pin Number	PC Card ATA	CompactFlash	Pin Number	PC Card ATA	CompactFlash
16	$\overline{\text{RDY}}/\overline{\text{BSY}}/\overline{\text{IREQ}}$	A4	50	–	Ground
17	VCC	A3	51	VCC	–
18	–	A2	52	–	–
19	–	A1	53	–	–
20	–	A0	54	–	–
21	–	DD0	55	–	–
22	A7	DD1	56	CSEL	–
23	A6	DD2	57	$\overline{\text{VS2}}$	–
24	A5	WP/$\overline{\text{IOIS16}}$	58	RESET	–
25	A4	$\overline{\text{CD2}}$	59	$\overline{\text{WAIT}}$	–
26	A3	$\overline{\text{CD1}}$	60	$\overline{\text{INPACK}}$	–
27	A2	DD11	61	$\overline{\text{REG}}$	–
28	A1	DD12	62	BVD2/SPKR	–
29	A0	DD13	63	$\overline{\text{STSCHG}}$/BUDI	–
30	DD0	DD14	64	DD8	–
31	DD1	DD15	65	DD9	–
32	DD2	$\overline{\text{CE2}}$	66	DD10	–
33	WP/$\overline{\text{IOIS16}}$	$\overline{\text{VS1}}$	67	CD2	–
34	Ground	$\overline{\text{IORD}}$	68	Ground	–

Appendix C Connection Issues Summary

Table 10 shows all connection possibilities between a ATA hard drive, PC ATA card, or Microdrive and the i.MX1/L/S processor. For each connection, host and device modes are described with hardware requirement.

Table 10. Connection Issues Summary[1]

Hard Drive Device	Host Connector & Controller	Standard Transfer Mode Used between Device and Host	Device ATA/True IDE Mode (when available)	Required Hardware	Notes
PC ATA Card	PCMCIA controller	PCMCIA I/O	None	None	There is no ATA equivalent mode for PCMCIA I/O mode
	i.MX1/L/S PCMCIA daughter board	PCMCIA I/O	None	i.MX1/L/S PCMCIA daughter board with specific glue logic to ensure slow timings	There is no ATA equivalent mode for PCMCIA I/O mode. See AN 2417
	ATA controller	True IDE	PIO 0, 1, 2, 3, 4	PCMCIA to ATA adapter	PC ATA card must be True IDE compliant
Microdrive	CompactFlash controller	True IDE	PIO 0, 1, 2, 3, 4 Multiword DMA 0, 1, 2 UDMA 0, 1, 2	None	Multiword DMA and UDMA modes are performed by the latest Microdrives
		I/O	None	None	There is no ATA equivalent mode for CompactFlash I/O mode
	i.MX1/L/S CompactFlash daughter board	True IDE	PIO 0,1,2,3,4	i.MX1/L/S CompactFlash daughter board without specific glue to ensure slow timings.	Daughter board glue logic must be modified to permit PIO mode 1 to 4
		I/O	None	i.MX1/L/S CompactFlash daughter board with specific glue logic to ensure slow timings	There is no ATA equivalent mode for CompactFlash I/O mode. See AN2417
	PCMCIA controller	PCMCIA I/O	PCMCIA I/O	CompactFlash to PCMCIA adapter	There is no ATA equivalent mode for PCMCIA I/O mode. Microdrive must be PCMCIA compliant
	ATA controller	True IDE	PIO 0,1,2,3,4 Multiword DMA 0,1,2 UDMA 0,1,2	CompactFlash to ATA adapter	Multiword DMA and UDMA modes are performed by the latest Microdrives
ATA drive	i.MX1/L/S CompactFlash daughter board *	True IDE	PIO 0,1,2,3,4	Direct connection on CompactFlash glue logic. Driver to define. (Experimental)	This is the first option to connect ATA hard drive to i.MX1/L/S Only PIO 0 mode timings are glue logic compliant. For PIO mode 1 to 4 glue logic must be modified.

Table 10. Connection Issues Summary[1] (continued)

Hard Drive Device	Host Connector & Controller	Standard Transfer Mode Used between Device and Host	Device ATA/True IDE Mode (when available)	Required Hardware	Notes
	Direct to i.MX1/L/S **	ATA	PIO 0,1,2,3,4 Multiword DMA 0,1,2	Driver and new daughter board to define.	This is the second option to connect ATA hard drive to i.MX1/L/S. PIO modes and Multiword DMA must be tested. Glue logic is simple (i.MX1/L/S EIM ensures correct timings)
	ATA controller	ATA	PIO 0,1,2,3,4 Multiword DMA 0,1,2 UDMA 0,1,2,3,4,5	None	–

1

* First solution to be tested, specific drivers must be implemented; connection is possible from an electrical perspective, however TrueIDE mode must be implemented.

** Second solution, new glue logic must be created with specific drivers.

Appendix D Other Modes of Read/Write Operations

Read/Write Operations in UDMA Mode

UDMA mode requires a specific DMA transfer mode called first party DMA. It means that the device (hard drive) becomes the master of the bus and it itself does the work of transferring data to and from memory without relying on the i.MX1/L/S processor's DMA controller. This mode is not supported by the i.MX1/L/S processor, therefore UDMA mode is not analyzed further in this document or supported by the i.MX1/L/S processors.

Read/Write Operations in Multiword DMA Mode

This mode permits the transfer of data between a device and memory using an external DMA request. In this case, the CPU is free to perform other operations, as the DMA controller manages all the data transfers instead. From a datarate perspective, there is no major difference because the timings remain the same. For the i.MX1/L/S processor to be compliant with this mode, an external glue logic must be added for the DMA request and acknowledge signals management. In this version of the document, this mode is not implemented and not analyzed further in this document.

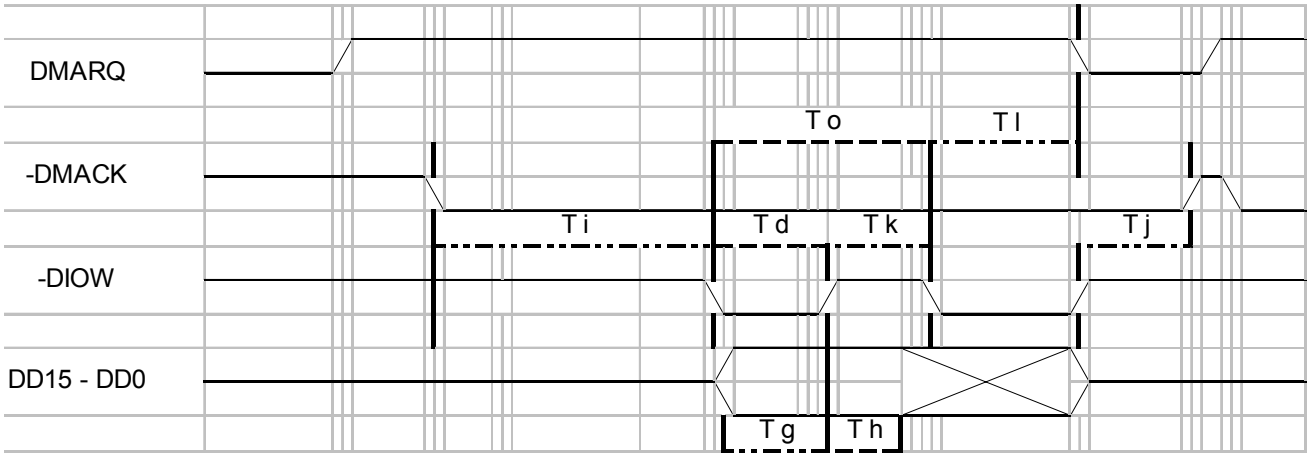

Figure 9. Multiword DMA Hard Drive Write Cycle

Table 11. Multiword DMA Write Operation Timings for Hard Drive

		Multiword DMA Transfert mode			
Symbol	Meaning	min / max ns	0	1	2
To	Cycle time	min	480	150	120
Td	-DIOW 16-bit	min	215	80	70
Tg	-DIOW data setup	min	100	30	20
Th	-DIOW data hold	min	20	15	10
Ti	DMACK to -DIOW setup	min	0	0	0
Tj	-DIOW to DMACK hold	min	20	5	5
Tk	-DIOW negated pulse width	min	215	50	25
Tl	-DIOW to DMARQ delay	max	40	40	35

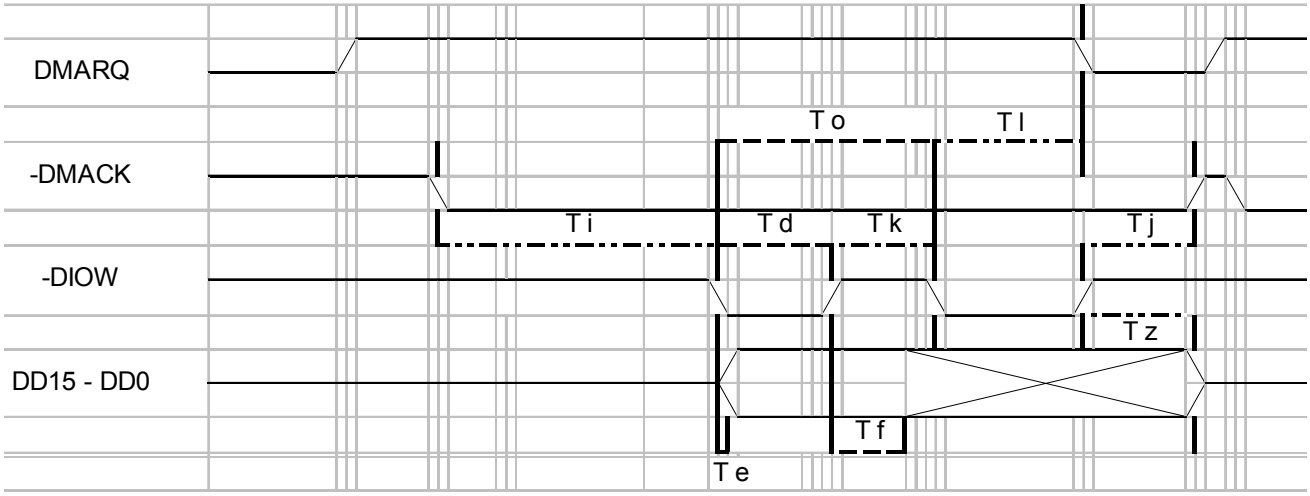

Figure 10. Multiword DMA Hard Drive Read Cycle

Table 12. Multiword DMA Read Operation Timings for Hard Drive

		Multiword DMA Transfert mode			
Symbol	Meaning	min / max ns	0	1	2
To	Cycle time	min	480	150	120
Td	-DIOR 16-bit	min	215	80	70
Te	-DIOR data access	max	150	60	50
Tf	-DIOR data hold	min	5	5	5
Tz	-DIOR to tristate	max	20	25	25
Ti	DMACK to -DIOR setup	min	0	0	0
Tj	-DIOR to DMACK hold	min	20	5	5
Tk	-DIOR negated pulse width	min	50	50	25
Tl	-DIOR to DMARQ delay	max	120	40	35

Appendix E Glossary

Automatic Acoustic Management—Hard disk technology to reduce mechanics noises.

ATA—Advanced Technology Attachment is a standard electronic interface and a communication protocol used between a computer motherboard's bus and the computer's disk storage devices.

ATAPI—ATA Packet Interface. Special set of commands specially designed to accommodate removable media devices like CD-ROMs, DVD-ROMs, CD writers, and tape drives. ATAPI is included in the ATA standard (as of ATA-4).

Bus—The bus (connections between and within the CPU, memory, and peripherals) used to carry data. Other connections are the address bus and control signals. The width and clock rate of the data bus determine its data rate (the number of bytes per second it can carry), which is one of the main factors determining the processing power of a computer. Most current processor designs use 32-bit bus, meaning that 32 bits of data can be transferred at once. Some processors have an internal data bus which is wider

than their external bus to make external connections cheaper while retaining some of the benefits in processing power of a wider bus.

Bus mastering—Refers to a feature supported by some bus architectures (like PCI) that enables a controller connected to the bus to communicate directly with other devices on the bus without using the CPU. Most modern bus architectures, support bus mastering because it improves performance. Bus mastering does not require a separate DMA channel because the DMA controller is contained on the device.

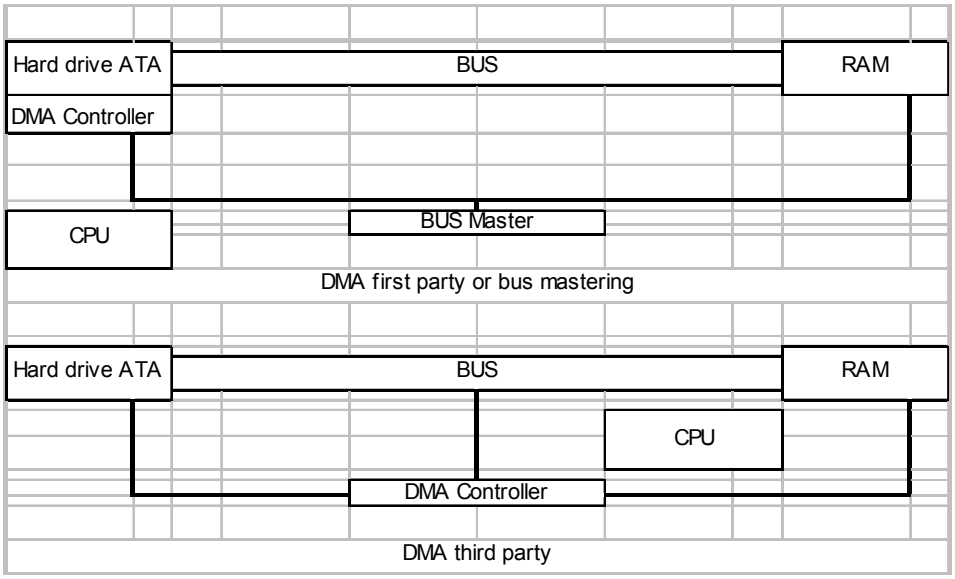

Figure 11. Difference Between DMA Third Party and Bus Mastering

CompactFlash—A very small-form factor removable mass storage device that relies on NAND Flash memory technology. CompactFlash was invented by SanDisk Corporation in 1994.

CIS—Stands for Card Information Structure. It is a data structure accessed through Card Service that contains configuration (data size, memory resources, …) and identification required for operations on the PC Card or CompactFlash Card. Card driver accesses the CIS during the initialization of the PC Card or CompactFlash Card.

CHS—Cylinder, Head, and Sector. Regular addressing of ATA drive is achieved by specifying a cylinder, head, and sector address where the required data resides.

CRC—Cyclic Redundancy Check. The CRC is one of the most commonly used techniques for error detection in data communications.

Double transition clocking—Signaling method (used for UDMA transfer) on the bus, data transfer occurs not once per clock cycle, but twice. This is implemented by having data transfer on both rising and falling edges of the clock.

DMA—Direct Memory Access is a hardware technology which improves programmed input/output operations. These operations are performed by an independent hardware subsystem (typically microcontrollers) or the device itself and not by the central processing unit. This allows for faster transfers, and takes the processing load off of the CPU. The DMA is called first party DMA or bus mastering when

the device supervises operations with its own DMA controller and is called a third party DMA when an independent microcontroller deals with DMA operations.

E-IDE—Enhanced-Integrated Drive Electronics is a commercial name used to indicate when a hard drive conforms to the ATA-2 specification.

EIM module—External Interface Module. This module permits to connect a memory module. EIM is enough flexible to connect other peripherals such as LCD, UART, Ethernet controller, or HDD ATA.

Fast ATA and Fast ATA 2—Commercial names to indicate specific transfer modes (respectively PIO 3 and PIO 4) in the ATA-2 specification.

IDE—Integrated Drive Electronics is a commercial name used to indicate first hard drives with integrated controller. This means that most of the control circuitry is built into your “IDE Drive”, and not on an external controller. IDE became ATA-1 in 1990. Most people consider any ATA drive to be an IDE Drive.

LBA—Logic Block Addressing, allows access to the hard drive sector without using CHS technology. Required to access all sectors for hard drives that are greater than 500 Mbytes. LBA is a new method of addressing sectors. Instead of referring to a cylinder, head and sector number, each sector is instead assigned a unique sector number.

Microdrive—A type of CompactFlash card containing a 1-inch hard disk inside.

PC Card ATA—A type of PCMCIA card containing a Hard Disk Drive or flash memory inside. The PCMCIA specification defines a special mode, close to the ATA specification, for those products.

PCMCIA—The Personal Computer Memory Card International Association, founded in 1989, which develops standards for PC Cards.

PIO—Programmed Input/Output is the basic transfer mode between a hard drive and computer motherboard. This mode must be handled by the central processing unit, contrary to DMA mode.

Sector—Hard drive data unit. One sector contains 512 bytes.

Secure lock—Hard drive special feature. Secure lock is a password data protection system. Without the password, users cannot access hard drive data.

Serial-ATA or SATA—SATA is an evolution of the ATA physical storage interface. SATA is based on serial signaling technology, unlike current IDE hard drives that use parallel signaling.

SMART—Self-Monitoring Analysis and Reporting Technology. It is a technology that enables the PC to predict the future failure of hard disk drives.

TrueIDE—A mode described in the CompactFlash specification. TrueIDE mode conforms to the ATA-4 specification. This mode is primarily used for Microdrive hard disk products.

ULTRA-DMA X, UDMA X or UTRA ATA X—Commercial names to indicate specific DMA transfer modes in ATA specifications. (See Table 3 on page 3 ATA Standard summary).

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The following Freescale Semiconductor Inc. documents were referenced to produce this document:

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(order number MC9328MX1/D)

MC9328MXL Integrated Portable System Processor Advance Information
(order number MC9328MXL/D)

The following additional sources were referenced to produce this document:

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