Freescale Semiconductor
Application Note

Document Number: AN2995
Rev. 0, 07/2005

PLL Restart Effect on SDRAM

MC9328MX1, MC9328MXL, and MC9328MXS

By: Michael Kjar

1 Abstract

This document applies to the following i.MX devices, collectively called i.MX throughout:

- MC9328MX1
- MC9328MXL
- MC9328MXS

This document describes the effect changing the System PLL frequency has on SDRAM memories connected to the i.MX microprocessors.

The Phase-Locked Loop (PLL) and Clock Controller chapter in the i.MX reference manuals describe the procedure for changing the System PLL frequency as follows:

1. Program the desired values of PD, MFD, MFI, and MFN into the SPCTL0.
2. Set the SPLL_RESTART bit in the CSCR (it will self-clear).
3. New PLL settings will take place.

The problem occurs when restarting the System PLL. The SDRAM Controller Clock signal (SDCLK) is fed

Contents

directly from the System PLL. When the PLL is restarted, the SDCLK signal goes low (stops toggling) for about 100 µs, then starts toggling at the new frequency. (The restart and lock time of the System PLL is ~100 µs, though this may vary depending on the frequency difference between the old and new PLL settings). Figure 1 illustrates the SDCLK waveform during the System PLL restart time. During this SDCLK low time, the problem is neither an auto-refresh command is issued nor self refresh mode being engaged. Figure 1 illustrates this as the SDCKE0, RAS, and CAS signals remains at logic high.

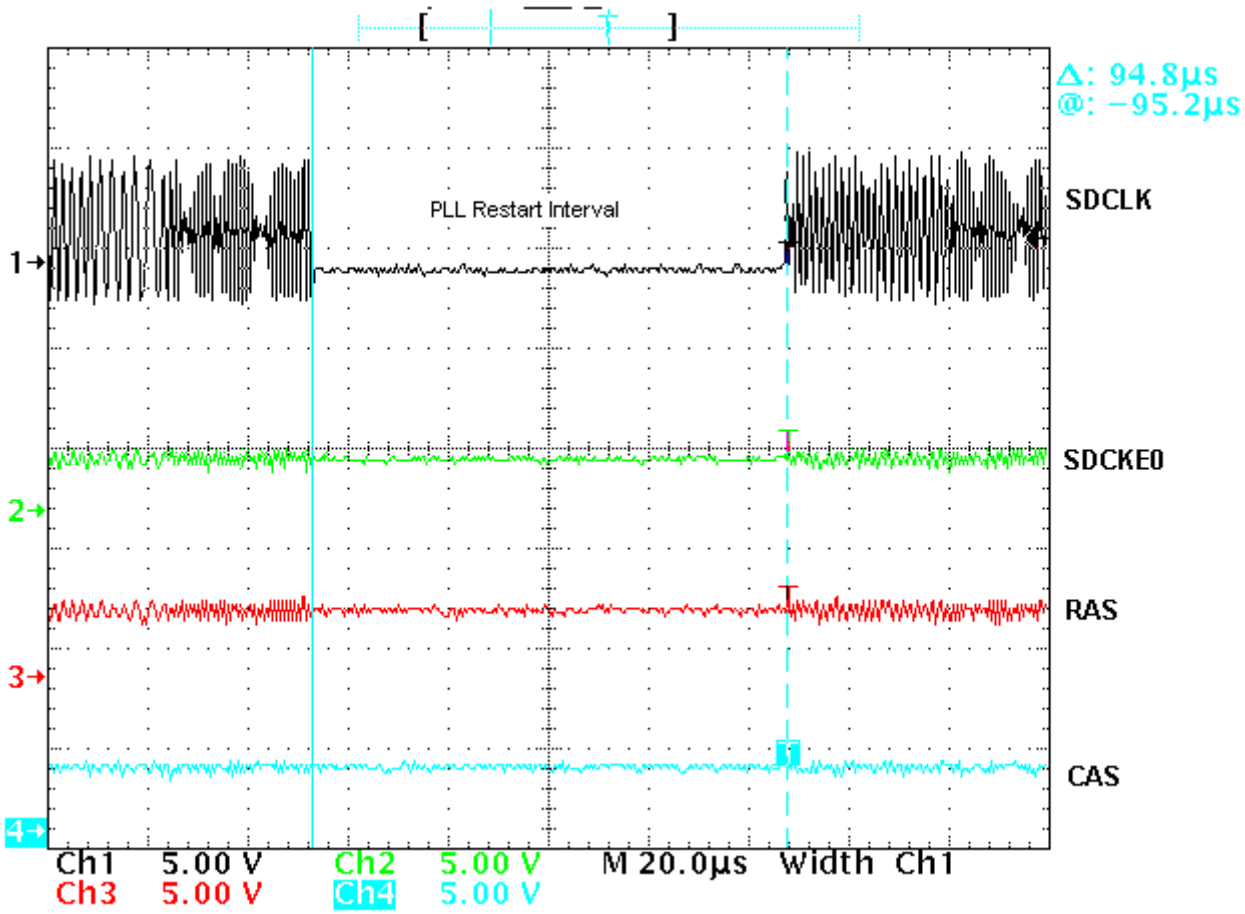

Figure 1. Visual Display of Problem Restarting the PLL

SDRAM memories require a certain number of refresh commands within a 64 ms time period. The number of refresh commands is congruous with the number of SDRAM row addresses. The i.MX supports 11, 12, and 13 row addresses, or SDRAM memories with 2048, 4096, and 8192 rows ($2^{\text{number of row addresses}}$ = number of rows). Thus, for an SDRAM memory with 2048 rows, 2048 refresh commands are required during a 64 ms time period to guarantee data integrity. The SDRAM Controller issues distributed refresh commands meaning that it distributes the required number of refresh commands throughout the 64 ms time period. To issue 2048 refresh commands in a 64 ms time period requires that the SDRAM Controller issue a refresh command every 31.25 µs (64 ms/2048 refresh cycles), which is the clock period of a 32 KHz clock. The SDRAM Controller refresh cycles are referenced to the (microprocessor) internal 32 kHz clock. When the SDRAM Controller is required to issue 4096 refresh commands, it will generate two refresh commands every 31.25 µs refresh cycle, and similarly when required to issue 8192 refresh commands, it will generate four refresh commands every 31.25 µs refresh

cycle. For example, a 64 Mbyte SDRAM with 13 row addresses and four refresh commands every 31.25 µs, the 100 µs SDCLK low time would mean that three refresh cycles or twelve refresh commands would not be issued. This could cause the data in non-refreshed rows in the SDRAM to be corrupted.

2 Recommended Approach to Changing System PLL Frequency

In most applications, the System PLL frequency would only be changed once during cold start up when the rest of the chip and system is being initialized. The Clock Controller features various dividers and clock gates to change the clock frequencies routed to various modules or gated off for additional power savings. Though cold start up is the preferred time to initialize the PLL, some applications may require the PLL frequency to change during system operation. Each method is discussed in the following sections.

2.1 Cold Start Up

Cold start up or power-on reset occurs when the processor is initially powered on. Most applications execute a type of boot code that initializes the chip and prepares it for loading and executing the operating system. The boot code initializes the system frequency and SDRAM memory. It is recommended to initialize and set up the PLLs before initializing the SDRAM. This procedure will ensure that the PLL restart time will not adversely affect the SDRAM memory.

2.2 During System Operation

Should the application require changing the System PLL frequency anytime after cold start up, the following sequence is recommended to maintain the data integrity of the SDRAM memory.

1. Program the System PLL Control Register 0 (SPCTL0) with the new desired System PLL Frequency.
2. Set up the Real Time Clock (RTC) module to interrupt at a desired time (either using one of the preset sampling timers or the one or two hertz timer).
3. Enable the RTC interrupt.
4. Immediately place the processor into STOP mode by disabling both the MCU and System PLLs.
5. Execute the Wait-For-Interrupt (WFI) instruction.

Entering STOP mode turns off the PLLs and forces the SDRAM Controller to issue a self refresh command to the SDRAM memory. When the RTC interrupt occurs, the PLL restarts at the new frequency and brings the SDRAM out of self refresh. For more information on entering STOP mode, please refer to *Power Network Design for i.MX1, i.MXL, and i.MXS* (order number AN2537).

3 References

These documents can be found at the Freescale Semiconductor World Wide Web site http://www.freescale.com/imx. These documents may be downloaded directly from the World Wide Web site, or printed versions may be ordered.

MC9328MX1 Data Sheet (order number MC9328MX1/D)

MC9328MX1 Reference Manual (order number MC9328MX1RM/D)

MC9328MXL Data Sheet (order number MC9328MXL/D)

MC9328MXL Reference Manual (order number MC9328MXLRM/D)

MC9328MXS Data Sheet (order number MC9328MXS/D)

MC9328MXS Reference Manual (order number MC9328MXSRM/D)

Power Network Design for i.MX1, i.MXL, and i.MXS (order number AN2537)

4 Revision History

Table 1 shows the revision history of this document.

Table 1. Revision History

Rev. Num	Author	Revisions
0	Michael Kjar	Initial version

NOTES

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

***For Literature Requests Only*:**
Freescale Semiconductor Literature Distribution Center
P.O. Box 5405
Denver, Colorado 80217
1-800-521-6274 or 303-675-2140
Fax: 303-675-2150
LDCForFreescaleSemiconductor@hibbertgroup.com

Document Number: AN2995
Rev. 0
07/2005

freescale™
semiconductor