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AC Timing Analysis Between SDRAM and the StarCore®-Based MSC8122 DSP

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This application note and the associated Excel spreadsheet assist in the analysis of AC timing for the interface between an SDRAM and the MSC8122 DSP. Such a timing analysis is necessary to select an appropriate SDRAM device and to derive board design guidelines for this interface.

The Excel file (AN3014SW) contains three sheets, each defined according to the MSC8122 core voltage and bus frequency. Each sheet includes a column defining the AC specifications of the MSC8122 device. In the sheet for your MSC8122 device, you must insert the appropriate SDRAM AC specifications according to the SDRAM device data sheet. In addition, there are options to adjust the board delay, clock skew, clock jitter, and board crosstalk. These values can be selected on the basis of PCB characterization. After you define these values, the spreadsheet calculates the maximum operating frequency for your configuration. If this frequency matches your desired target frequency, you can derive the guidelines for the PCB design.

This application note explains how to use the spreadsheet and describes the different fields you can modify.

Note: While this application note is specific for the MSC8122, the information also applies to the MSC8126 device, which uses the *MSC8126 Technical Data Sheet* as its specification reference.

Note: The revision number of the associated spreadsheet is Rev. 4, while this document is Rev. 1.

CONTENTS

1 Getting Started.

The AN_AC_timing_sdram_8122.xls Excel spreadsheet contains default values as a starting-point. A few standard SDRAM devices and their specifications are listed. Using the default values and the selected SDRAM device, you can perform initial timing analysis within a few minutes.

Some cells in the spreadsheet contain a scroll down menu with defined values for these options. Perform the following steps to add options to the scroll down menu:

1. Select the cell.
2. On the Data menu, click **VALIDATION**.
3. Add text to the source cell on the **SETTINGS** tab.
4. Click **OK**.

You can modify only a few cells; all others are protected. To modify a protected cell, remove the protections from the sheet by scrolling to the Tools menu **PROTECTION** option and selecting **UNPROTECT SHEET**.

Perform the following steps to use the Excel spreadsheet:

1. Make a copy of the AN_AC_timing_sdram_8122.xls file. Save the source file as read-only for future use, and use the copy for editing the spreadsheet fields.
2. Select the appropriate sheet in the Excel file by comparing your device selection/configuration with those listed in the following table:

MSC8122 Core Voltage	MSC8122 Device Frequency[1]	Your Spreadsheet Is:	Order Number
1.2 V	Core up to 400 MHz Bus up to 133 MHz	1_2v_133 MHz	MSC8122TVT6400 MSC8122TMP6400
1.2 V	More than 400 MHz Bus up to 166 MHz	1_2v_166 MHz	MSC8122VT8000 MSC8122MP8000
1.1 V	Up to 400 MHz Bus up to 133 MHz	1_1v_133 MHz	MSC8122TVT4800V MSC8122TMP4800V MSC8122TVT6400V MSC8122TMP6400V
Notes: **1.** Maximum bus frequency is *(core freq)/3*.			

3. Select the SDRAM type using the **G2** cell (column G, row 2) drop down menu. This field is used only for documenting the SDRAM type.
4. Select the SDRAM set-up time in **G3** and SDRAM delay time in G4 using the drop down menus in those cells. Comments for these cells appear when you point the cursor at each cell.
5. Select Sync method in cell **G5**. This field defines the clock synchronization method used between the MSC8122 and SDRAM. For more information, read the comment that appears when you point the cursor at the cell.
6. Review the resulting maximum frequency calculation in cells **L21** and **L33**.
   - **L21** presents the maximum bus frequency when the PCB load for every signal between the MSC8122 and SDRAM is 20 pF.

— **L33** presents the maximum bus frequency when the PCB load for every signal between the MSC8122 and SDRAM is calculated based on the load value defined in cell **B23**. You can change the value in **B23** to fit the specific PCB layout and characterization.

2 Spreadsheet Fields

This section describes all cells in the spreadsheet in detail.

2.1 SDRAM Parameter Settings

Many different SDRAM devices are available. Select a candidate SDRAM device that fits your application requirements, including physical dimensions, memory size, power, data width interface, price, temperature range, and so on. You must analyze the AC timing interface between the MSC8122 and the candidate SDRAM.

Cells **G2**, **G3**, **G4**, and **G6** in the spreadsheet should be set based on the specifications in the SDRAM data sheet. Enter the relevant values from the SDRAM data sheet into the spreadsheet cells. The examples in this document and some default values in the spreadsheet are taken from the data sheet of the MT48LC2M32B2-5 SDRAM device. A description of the spreadsheet cells follows:

- **G2**, *SDRAM type*. Has no impact on the excel calculation. It is used only to document the source of information for which SDRAM is used in the timing analysis. Refer to **Section 1**, *Getting Started.*, on page 2 for directions on how to add options to the scroll down menus.

  Select your SDRAM type from the drop down list. You can add a description of your candidate SDRAM to the **G2** cell comment, as follows:

  a. Select the cell and right click.

  b. Select **EDIT COMMENT** from the menu that appears.

  c. After you edit the comment, size the comment window so that all comment text appears. Then just click in another cell. The edit window disappears and the comment edit is complete.

- **G3**, *Setup time [nS]*. Defines how many nanoseconds that the SDRAM input must be valid before the clock rising edge. It is used for all SDRAM inputs (address, data, and control):

  Example (MT48LC2M32B2-5): Page 1, table: “Key Timing Parameters.”

  Column: Set-up Time = 1.5 nS.

  For details, see the table on page 32 of the MT48LC2M32B2-5 data sheet, entitled “Electrical Characteristics and Recommended AC Operating Conditions.” Different set-up lines: Address set-up time, data-in set-up time, $\overline{\text{CS}}$, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, DQM set-up time.

- **G4**, *Delay time [nS]*. Defines how many nanoseconds the SDRAM data outputs are valid after the clock rising edge.

  Example (MT48LC2M32B2-5): Page 1 of the MT48LC2M32B2-5 device data sheet, table: “Key Timing Parameters.”

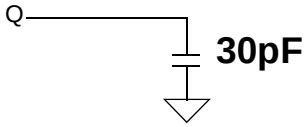
  Column: Access Time = 4.5 nS.

  For details, see the table on page 32 of the MT48LC2M32B2-5, entitled “Electrical Characteristics and Recommended AC Operating Conditions.” Line: Access time from CLK

- **G6**, *SDRAM AC spec load [pF]*. Defines the load used for the SDRAM device AC specification characterization, measured in pF.

  Example (MT48LC2M32B2-5): Page 35 of the MT48LC2M32B2-5 device data sheet, note 9.

  Outputs measured at 1.5 V with equivalent load: 30 pF



2.1.1 Output AC Specification Adaptation to Load

The MSC8122 and SDRAM AC specification for outputs is for a specific load on each pin. The PCB can be designed with a smaller or larger load than is specified. This adjustment requires adaptation of the timing to match the new load value. The updated timing is calculated on the basis of adding 0.06 ns for each additional 1 pF load or subtracting 0.06 ns for each decrease in the 1 pF load.

$$T_{update} = T_{AC\_spec} + 0.06 \times (Actual\_load - AC\_SPEC\_load)$$

The equation for the timing update was tested by comparing it with the MSC8122 IBIS model. There is no commitment for this equation to represent the update timing fully. For a more accurate calculation, you can run the IBIS model and override the updated AC timings in the spreadsheet.

For the example MT48LC2M32B2-5, delay time for data output is 4.5 ns measured on a 30 pF load. When the actual load on the board is 25 pF, the update delay time is as follows:

$$delay\_time_{update} = 4.5 + 0.06 \times (25 - 30) = 4.5 - 0.30 = 4.2nS$$

2.1.2 Spreadsheet Cells for Updated Timings

This section describes the cells affected by the timing and load values. It cites the relevant source cells for calculating the value of the described cell. If you choose different values, which can be retrieved from an IBIS simulation, you should update the cells by overriding the formula value with the calculated update value.

- **C32**, *Output delay time*. Calculated from the SDRAM AC spec delay time in cell **G4** and the SDRAM AC specification load in cell **G6** relative to the real load in cell **B23**.
- **I23**–**I31**, *Output delay time for MSC8122 output signals*. Calculated from the MSC8122 AC spec output delay time defined in cells **I11**–**I19** and the MSC8122 AC spec load in cell **B11** relative to the real load in cell **B23**.

2.2 Board Parameters

The spreadsheet cells containing parameters for board and clock distribution that affect the synchronous interface between the MSC8122 and SDRAM are as follows:

- **C2**, *Board delay [nS]*. Holds the propagation delay of the signal traces on the PCB. Placing the MSC8122 and SDRAM devices with a short physical distance between them decreases this value. This value is added to the total timing calculation for each signal.
- **C3**, *Clock skew [nS]*. Defines the maximum timing difference between the MSC8122 clock and the SDRAM clock. This difference may be caused by a nonequivalent load on the two clock lines or by skew inserted by a clock buffer. This value is used for the total timing calculation for each signal based on the synchronization method selected in the spreadsheet. For details, see the Sync method description in **Section 2.3.1**, *Sync Method in G5 Cell*, on page 6.
- **C4**, *Clock jitter [nS]*. An additional uncertainty of clock behavior that affects a synchronized interface. Clock jitter can be generated in oscillators or PLL devices as well as in the MSC8122 PLL. This value is added to the total timing calculation for each signal.
- **C5**, *Board Crosstalk [nS]*. Coupling capacitance between adjacent signals on the board can insert additional delay. The default value in the spreadsheet is 0.2 nS. You can update this value based on estimation or simulation results for crosstalk. Crosstalk can be reduced by using more restrictive rules for board layout to define the space between lines and interleaving lines. This value is added to the total timing calculation for each signal. Since this value can differ for different lines, you can manually override the values for relevant signals in cells: **H23**–**H32**.
- **B23**, *Pad driving load*. To meet interface requirements for high frequency, the board should be designed to reduce capacitive load on the interface signals. The SDRAM should be located close to the MSC8122 and with minimal routing. You must update this cell with the maximum expected capacitive load, including input driving capacitance. There is no need to include output capacitance because it is already included in the output AC specification. For a more specific definition of driving load per group of signals, you can override the values in cells **B24**–**B31**. The default values are equal to the setting in **B23** and are based on the assumption that the SDRAM output signals and MSC8122 output signals drive the same load.

For example, we connect two MT48LC2M32B2-5 SDRAM devices, each with a 32-bit data interface to get a 64-bit interface. The maximal input capacitance for an SDRAM address pin is 4pF (see page 32 of the SDRAM data sheet), in addition to the estimated 3pF PCB capacitance for the address wire. The total load for the address pin is *2 SDRAM devices* $\times$ *4pF + PCB 3pF equals 11pF.*

For the data pins, the SDRAM data sheet indicates 6.5pF maximum input capacitance. Since the data signal is not connected to two SDRAM devices, the total load is *6.5pF + 3pF = 9.5pF.* An additional slave on the MSC8122 system bus, such as Flash memory, increases the load on some signals.

2.3 MSC8122 Parameters

You select the correct synchronization method between MSC8122 and SDRAM device for their configuration. All other parameters in this section are driven from the MSC8122 data sheet. The default values included in the spreadsheet are taken from the MSC8122 technical data sheet Rev. 9, 7/2005.

2.3.1 Sync Method in G5 Cell

There are two options for synchronizing the SDRAM and MSC8122MSC8122:

- *CLKIN*. The recommended clock scheme in which MSC8122 CLKIN is driven at the bus frequency, and the SDRAM clock input is driven from the same source. The source can be different outputs from the same clock buffer. The two clocks are aligned because of equivalent loading on the signals. The MSC8122 PLL aligns the internal bus clock with the CLKIN input (PLL skew elimination). For details, refer to the chapter on clocks in the *MSC8122 Reference Manual*. The clocks chapter contains a section on “Single Master Mode Board-Level Clock Distribution.” Especially see the figure entitled “MSC8122 Clock Distribution in Single-Master Mode Using CLKIN.”
- *CLKOUT*. The MSC8122 CLKOUT pin is the source for the SDRAM clock input pin. It can be connected through a zero-delay buffer. For details, see the following two figures in the clocks chapter of the *MSC8122 Reference Manual*:
  - MSC8122 Clock Distribution In Single-Master Mode Using CLKOUT With Zero-Delay Buffers.
  - MSC8122 Clock Distribution And Synchronization In Single-Master Mode Using CLKOUT With No Zero-Delay Buffers.

If the AC specification is relative to the appropriate clock (CLKIN or CLKOUT), the skew for the calculation is based on the user-defined skew from cell **C3**. If needed, the clock skew between CLKIN and CLKOUT is added based on information in cell **I1**.

2.3.2 CLKOUT Characterization Table I1–K2

The values in the CLKOUT characterization table are taken from the MSC8122 data sheet. They represent the clock skew between MSC8122 CLKIN and CLKOUT. The value is used as the clock skew value when the synchronization method is defined as CLKOUT. A positive number indicates CLKOUT preceding CLKIN. The interface is synchronized on the basis of the clock rising edge. Therefore, the spreadsheet table includes only rise-to-rise (r2r) characterization though the data sheet also specifies a fall-to-fall characterization.

Note: For 166 MHz, the CLKOUT skew relative to CLKIN is not characterized. For a 166 MHz interface, use the CLKIN synchronization method.

2.3.3 MSC8122 AC Specification Timing I11–I20

Spreadsheet cells **I11**–**I20** include the MSC8122 AC spec timing for the interface signals:

- Output timing for output signals.
- Set-up time for input signals.

The timings are taken from the MSC8122 data sheet according to core voltage, target frequency, and reference clock (from **Table 2-13** and **Table 2-14** in the *MSC8122 Technical Data Sheet*). These timings are used as reference timings for the update timing calculation in cells **I23** to **I32**.

3 Results

The number in cell **L33**, MAX FREQ, presents the maximum frequency in MHz that the interface can attain. Cells **K23**–**K32** present the maximum frequency for each signal. The minimum value for this group of cells is presented in **L33**, MAX FREQ. If the value in **L33** is smaller than the planned bus frequency, you must adjust the MSC8122–SDRAM interface using one or more of the following options:

1. Reduce the pad driving load by placing the SDRAM as closely as possible to the MSC8122 DSP. Focus on the pins that are the source for the frequency limit.
2. Use more efficient oscillator/clock buffers to reduce clock skew and jitter from these sources.
3. Use a different candidate SDRAM with AC specifications that match the MSC8122 operating requirements.

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