Freescale Semiconductor
Application Note

AN3103
Rev. 0, 9/2005

56F8000 Clock Generation Guidelines to Insure Correct Functionality

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1. Introduction

The 56F8000 Digital Signal Controllers (DSCs) developed by Freescale include a 56800E hybrid core, associated memories, and a mixture of analog and digital components. Various product features are affected by and place restrictions on how the clock generation system is configured. This document provides guidance on these functional restrictions and how to configure the clock generation system accordingly. Unless these guidelines are followed, the feature may not be available, or may not work as intended.

We will first review the architecture and operation of the clock generation system. We then expand the discussion to other system components. The material presented for a module will focus either on features whose availability or correct operation imposes constraints on clock generation or on clock generation features within the module itself. We will present the restrictions as we go so that their purpose can be seen in context. A simple list of all restrictions is included in **Section 6.** for easy reference.

This document is limited to issues where restrictions must be applied to clock generation in order to use the chip's features. It does not go into power management, which is discussed in an application note, AN3104. Much more information on clock generation and product features is available in the Data Sheet for the specific device being implemented and the **56F8000 Peripheral Reference Manual**, especially in sections relating to the OCCS and SIM modules.

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2. Clock Generation System

The primary clock source (MSTR_OSC) can be either the output of the on-chip Relaxation Oscillator (ROSC) or an external clock applied to pad GPIOB6. MSTR_OSC is used in the On-Chip Clock Synthesis Module (OCCS) as the input clock to the PLL. Either MSTR_OSC or the PLL must then be selected to be used for master clock generation. Either source can be used to generate the master clock, MSTR_2X, which is used to derive all the normal system and peripheral clocks. The MSTR_3X master clock is only produced if the PLL is selected. MSTR_3X supports the high-speed mode of the TMR and PWM modules. Generation of system, core, and peripheral clocks from the master clocks occurs in the System Integration Module (SIM). In the SIM, the MSTR_2X clock (which runs at 2 times the system bus rate) is divided by 2 to produce all the system clocks and normal-speed peripheral clocks, while MSTR_3X (which runs at 3 times the system bus rate, provided the PLL is selected) is passed through to clock high-speed peripherals.

2.1 Relaxation Oscillator (ROSC)

The Relaxation Oscillator can be configured three ways. It resets to Normal mode, where it generates 8MHz. Setting the ROSB bit in the OCCS OSCTL register puts the ROSC in Standby mode, where it generates 400KHz. Setting the ROPD bit in the OCCS OSCTL register powers down the ROSC. ROPD takes precedence over ROSB.

Accuracy of the ROSC output frequency is maximized by setting the value of the TRIM field in the OCCS_OCTRL register. The part is delivered with a factory-provided trim value which is loaded during reset from the Flash IFR memory block into the FM_OPT1 register in the Flash Module (FM). Start-up code must transfer this trim value to the TRIM field of the OCCS_OCTRL register. The Freescale software development tools automatically include this in the start-up code. After TRIM is set this way, a ROSC frequency error will not exceed 0.3% at room temperature and will not vary by more than 2.8% over the allowed temperature range. This accuracy is sufficient for the correct operation of the part’s communication interfaces.

2.2 Clock Synthesis Module (OCCS)

The primary clock source (MSTR_OSC) is determined by the setting of the PRECS field in the PLLCR register of OCCS. When PRECS is 0, MSTR_OSC is the output of the ROSC and when PRECS is 1, MSTR_OSC is the external clock, which is taken directly from the GPIOB6 external pad. MSTR_OSC must be glitch free. This leads to the first restriction.

1. A valid external clock input signal must be applied to the GPIOB6 pad before and while it is selected as the primary clock source (PRECS = 1). A valid clock input will be 0-64MHz and glitch free.

The PLL uses MSTR_OSC as an input clock and requires that MSTR_OSC be 8MHz. The PLL is activated by setting PLLPD to 0 in the PLLCR register; appropriately setting the PLL postscaler divider (PLLCOD in the PLLDB register); and waiting for the PLL to lock. The locked PLL output frequency is 192MHz. Available settings of PLLCOD (/1, /2, /4, /8, /16, and /32) support PLL postscaler output frequencies from 6MHz to 192MHz. Lock status is observed at the LCK1 and LCK2 fields in PLLSR and can trigger interrupts using features in the same register. Once the PLL is locked, the PLL can be selected to generate the master clock outputs (ZSRC = 10) MSTR_2X and MSTR_3X. Otherwise, MSTR_OSC is used to generate these master clocks (ZSRC = 01). While the PLL is selected, MSTR_OSC must remain at 8MHz and the PLL must not be reconfigured. The PLL (ZSRC=01) must be deselected before changing the MSTR_OSC frequency (away from 8MHz) or altering the PLL controls PLLPD and PLLCOD.

2. MSTR_OSC must be 8MHz before turning on the PLL (PLLPD = 0). The 8MHz can come from the ROSC in normal mode (PRECS = 0, ROPD = 0, ROSB = 0) or from an 8MHz external clock applied to the GPIOB6 pad (8MHz input to GPIOB6 and PRECS = 1).
3. The PLL must be on (PLLPD = 0) before it will lock (LCK1, LCK2).
4. The PLL must be on (PLLPD = 0) and locked (LCK1, LCK2) before the PLL postscaler output can be used to generate the master clocks (ZSRC = 10).
5. You must revert to using MSTR_OSC for master clock generation (ZSRC = 01) before altering the frequency of MSTR_OSC (away from 8MHz) or changing the PLL controls PLLCOD or PLLPD.

The OCCS guarantees glitch-free transition when changing the selection of primary clock source (PRECS) or changing the signal used for master clock generation (ZSRC). The ROSC also guarantees glitch-free transition when being reconfigured (altering ROSB or TRIM).

Master clock generation is done differently depending on the setting of ZSRC. When the PLL is selected to generate the master clocks (ZSRC = 10), the PLL postscaler output is divided by 3 to generate MSTR_2X (2—64MHz) and divided by 2 to generate MSTR_3X (3—96MHz). While MSTR_OSC is selected to generate the master clocks (ZSRC = 01), MSTR_2X is fed directly from MSTR_OSC and MSTR_3X is off. This eliminates the dividers and reduces the MSTR_OSC frequency required for operating the system bus at its maximum supported rate of 32MHz. This is illustrated in **Figure 2-1**.

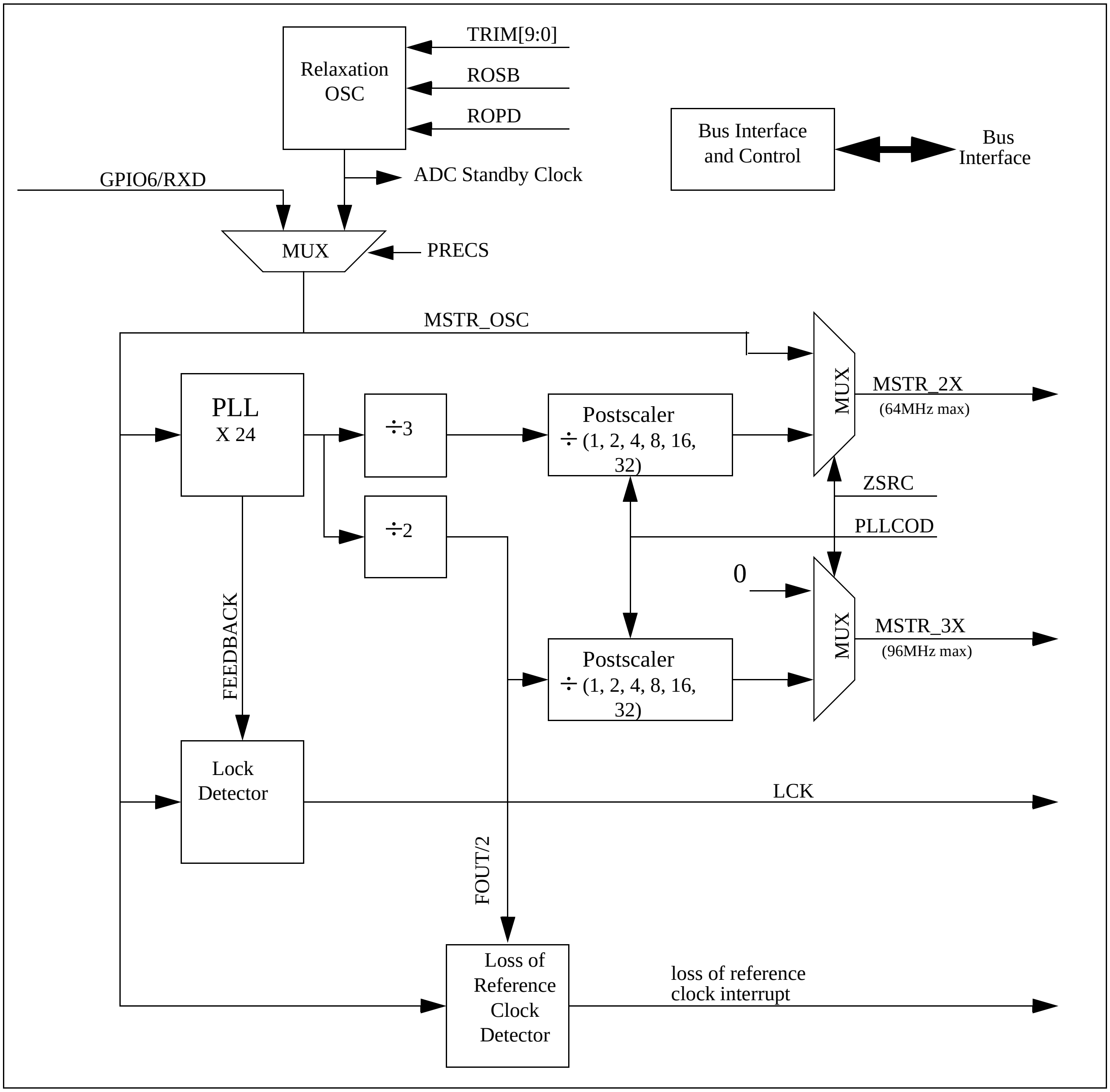

Figure 2-1. OCCS Master Clock Generation

2.3 System Integration Module (SIM)

Core, system, and normal rate peripheral clocks are derived by dividing MSTR_2X by 2. The previously discussed restrictions and functionality insure that the maximum rate is 32MHz and that the clocks are glitch free. High-speed peripheral clocks are derived directly from MSTR_3X . MSTR_3X operates at three times the normal system bus rate and thus at a maximum 96MHz.

The SIM contains controls that determine whether a high-speed or normal-speed clock is delivered to a peripheral supporting high-speed operation (PWM and Timer). Since the MSTR_3X clock only operates when the PLL postscaler is selected in OCCS to generate the master clocks (ZSRC = 10), it's easy to see the next restriction.

6. The high-speed mode enables for the Timer and PWM modules (TCR and PCR in SIM_GPS) must only be asserted if the PLL is selected in OCCS to generate the master clocks (ZSRC = 10).

One of the power management functions of the SIM is the ability to put the large voltage regulator into Standby mode. The large regulator generates the internal V_{DD_CORE} rail which supplies all the digital logic. Standby mode reduces the bias current consumed by the large regulator but can not maintain V_{DD_CORE} if the system bus frequency exceeds 200KHz.

7. The large regulator standby mode should not be asserted (LRSTDBY in SIM_PWR = 1) at system bus frequencies over 200KHz. The system bus frequencies required for large regulator standby mode can be accomplished either by using the ROSC while it is in standby (PRECS = 0, ROSB = 1, ROPD = 0) or by sourcing from an external clock of 400KHz or less (maximum 400KHz into GPIOB6 and PRECS = 1).

The SIM has several functions used to gate the peripheral and system clocks it generates and which therefore affect the functionality of other modules. These fields will be referenced in clocking restrictions related to other modules.

The SIM STOP_DISABLE field controls whether Stop Mode is entered upon execution of a core STOP instruction and, similarly, WAIT_DISABLE controls whether Wait Mode is entered upon execution of a core WAIT instruction. System clocks and core clocks (to the 56800E core) are disabled in Wait Mode. System clocks, core clocks, and, optionally, peripheral clocks are disabled in Stop mode.

Interrupts cause the SIM to return to Run mode from Wait or Stop mode upon the occurrence of any enabled interrupt. The timer channel peripheral clocks can be exempted from being disabled in Stop mode by setting the corresponding TCx_SD bit. The SCI can be exempted from being disabled in Stop mode by setting SCI_SD. This provides the option for these peripherals to operate and generate interrupts capable of recovering the part from Stop to Run Mode.

The ONCE_EBL bit in SIM_CTRL allows the debug clock (PCLK) to the core to operate even when the core's TAP interface is disabled. PCLK is used to clock EONCE registers. Real-time debugging requires the applications code input or output to these registers. Setting ONCE_EBL guarantees these registers are clocked, regardless of the state of the core TAP. This is addressed as a restriction under the core later in this document.

Finally, the SIM_PCE register contains a bit per peripheral to enable clocking to that peripheral. This is useful for power management. These controls are referenced in peripheral-related restrictions later in this document.

2.4 Clock Generation Coming Out of Reset

At reset, the primary clock source (MSTR_OSC) in OCCS is the ROSC (PRECS = 0) in normal mode (ROSB = ROPD = 0) outputting 8MHz. The reset default of ZSRC = 01, so that the master clocks are derived from MSTR_OSC rather than PLL postscaler output and the PLL is off (PLLPD = 1). Since MSTR_OSC is used for master clock generation, MSTR_2X is MSTR_OSC (8MHz), and MSTR_3X is off. Therefore, high-speed peripheral clocking is not yet available and all enabled system, core, and peripheral clocks will operate at 4MHz (MSTR_2X divided by 2). The default state of the SIM is Run mode, so all system and core clocks are enabled out of reset. All peripheral clocks are disabled, however, since the reset default state of the SIM_PCE register is all 0.

The important thing to realize is that the core and memories operate at 4MHz, using clocks generated from the ROSC until the clocking is reconfigured.

3. Peripherals

General restrictions are presented here and any peripheral-specific restrictions are presented in the subsections that follow. Since most peripherals must be appropriately configured based on the frequency of its peripheral clock, the correct operation of peripherals is not guaranteed when changing peripheral clock frequency or when the peripheral clock is disabled by peripheral-specific controls or by power savings modes. While it is not electrically damaging to leave a peripheral enabled under these conditions, it is recommended in order to prevent the use of invalid results.

8. A peripheral must not be accessed unless its peripheral clock is also enabled (the corresponding bit in SIM_PCE is set to 1).
9. Peripherals should be disabled when changing master clock frequency. Master clock frequency will change if you change external clock frequency while sourcing from the external clock (change external clock frequency into GPIOB6 while PRECS = 1); if you change the ROSC output frequency while sourcing from it (change ROSB, ROPD, or TRIM while PRECS = 0); or change the PLL postscaler output frequency while the PLL postscaler output is being used to generate the master clocks (change PLLPD or PLLCOD while ZSRC = 10).
10. Peripherals should be disabled before entering Stop mode (before executing the STOP instruction while STOP_DISABLE is not asserted), unless the SIM provides a peripheral-specific stop-disable control and it is asserted (peripheral is the SCI and SCI_SD = 1 or the peripheral is a timer channel and the corresponding TMR*x*_SD = 1).
11. Communications interface peripherals generally require an accurate, stable peripheral bus frequency and provide clock prescalers to configure the module for a required or desired transfer rate. Peripherals may constrain the accuracy of the system/peripheral clock and some transfer rates may be unsupported at some peripheral clock frequencies. This should be determined from the **56F8000 Peripheral Reference Manual**.
12. When using the ROSC as the primary clock source, the TRIM field in the OCCS_OCTRL register must be initialized at start-up to the factory-provided value, which can be obtained from the FM_OPT1 register of the Flash Module (FM). This is done automatically by the Freescale software development tools and insures that a ROSC frequency error will not exceed 2.8% over temperature. This insures that frequency accuracy is sufficient to permit correct operation of the part’s communication interfaces over the device’s allowed operating range.

3.1 ADC

The ADC generates its conversion clock by dividing down the ADC peripheral clock. The ADC is designed to operate with a conversion clock rate between 100KHz and 5.33MHz. The ADC’s peripheral clock always runs at the system bus rate. The divider must be set to divide the system bus rate (MSTR_2X divided by 2) down to a frequency in this range before the ADC is enabled.

13. The ADC peripheral clock frequency (MSTR_2X divided by 2) after division per the ADC CLKDIV field must produce an ADC conversion clock in the range 100KHz to 5.33MHz (32MHz divided by 6).

When performing scans in any mode except looping modes, the scans are initiated by Start signals, the frequency of which is determined by the user. The duration of a scan is based upon the conversion clock frequency, the setting of the power-up delay (PUDELAY), and the number of samples to be taken by the scan. The details of this are covered in Application Note AN3104 and the **56F8000 Peripheral Reference Manual**.

14. When operating in non-looping Scan modes, the scan duration (as determined by the Scan mode, number of samples per scan, conversion clock frequency, and PUDELAY) must be configured so that a scan completes within the period available per the scan frequency.

3.2 GPIO

The external pads can typically be configured as GPIO or as one or more different peripheral functions. GPIOB6 has one clock-related dependency. While the pad is being used as an external clock source, the GPIO and peripheral functions must not enable the output buffer of the pad, causing contention with the input clock signal. The following restriction is based on keeping the GPIO in control of the pad and configured as an input so the output driver will not contend. Other solutions are possible, but one is sufficient.

15. While GPIOB6 is being used as an external clock source (PRECS = 1), the GPIOB6 pad must remain configured as a GPIO input (this is the reset default) in order to avoid contention with the clock input signal (GPIOB_PEREN[6] = 0, GPIOB_DDIR[6] = 0).

4. 56800E Core and RAM

The core and RAM can operate at any system bus frequency. The only module-specific functions affected by clock configuration are the embedded EONCE debugger and core TAP interface. The core TAP interface is used by the software development/debug environment to download code, access the Program and Data spaces, and access core registers via the EONCE module. The TAP interface clock frequency (TCLK) should not exceed 1/8 the system bus frequency. The internal debug clock (PCLK) generated by the SIM is used to clock debug registers within the core. These registers are code accessible for real-time debugging. PCLK normally operates only when the core TAP is enabled. Setting ONCE_EBL in the SIM insures that PCLK operates regardless of the state of the TAP.

16. TCLK frequency must not exceed 1/8 of the system bus frequency.
17. Set ONCE_EBL in SIM_CTRL = 1 when doing real-time debugging to insure that debug registers in the core being accessed from the applications code are clocked, regardless of the state of the core TAP.

5. Program Flash Memory

The Flash Module (FM) and Program Flash support Flash reads at any frequency. Flash write and erase operations are supported only for system bus frequencies of at least 1MHz.

18. Flash program and erase functions require a minimum system bus frequency of 1MHz. The clock must be sourced from the ROSC in normal mode (ROSB = 0, ROPD = 0) or from an external clock of at least 2MHz in order to perform Flash program or erase.

6. Summary List of Restrictions

1. A valid external clock input signal must be applied to the GPIOB6 pad before and while it is selected as the primary clock source (PRECS = 1). A valid clock input will be 0—64MHz and glitch free.
2. MSTR_OSC must be 8MHz before turning on the PLL (PLLPD = 0). The 8MHz can come from the ROSC in normal mode (PRECS = 0, ROPD = 0, ROSB = 0) or from an 8MHz external clock applied to the GPIOB6 pad (8MHz input to GPIOB6 and PRECS = 1).
3. The PLL must be on (PLLPD = 0) before it will lock (LCK1, LCK2).
4. The PLL must be on (PLLPD = 0) and locked (LCK1, LCK2) before the PLL postscaler output can be used to generate the master clocks (ZSRC = 10).
5. You must revert to using MSTR_OSC for master clock generation (ZSRC = 01) before altering the frequency of MSTR_OSC (away from 8MHz) or changing the PLL controls PLLCOD or PLLPD.
6. The high-speed mode enables for the Timer and PWM modules (TCR and PCR in SIM_GPS) must only be asserted if the PLL is selected in OCCS to generate the master clocks (ZSRC = 10).
7. The large regulator standby mode should not be asserted (LRSTDBY in SIM_PWR = 1) at system bus frequencies over 200KHz. The system bus frequencies required for large regulator standby mode can be accomplished either by using the ROSC while it is in standby (PRECS = 0, ROSB = 1, ROPD = 0) or by sourcing from an external clock of 400KHz or less (maximum 400KHz into GPIOB6 and PRECS = 1).
8. A peripheral must not be accessed unless its peripheral clock is also enabled (the corresponding bit in SIM_PCE is set to 1).
9. Peripherals should be disabled when changing master clock frequency. Master clock frequency will change if you change external clock frequency while sourcing from the external clock (change external clock frequency into GPIOB6 while PRECS = 1); if you change the ROSC output frequency while sourcing from it (change ROSB, ROPD, or TRIM while PRECS = 0); or change the PLL postscaler output frequency while the PLL postscaler output is being used to generate the master clocks (change PLLPD or PLLCOD while ZSRC = 10).
10. Peripherals should be disabled before entering Stop mode (before executing the STOP instruction while STOP_DISABLE is not asserted), unless the SIM provides a peripheral-specific stop-disable control and it is asserted (peripheral is the SCI and SCI_SD = 1 or the peripheral is a timer channel and the corresponding TMR*x*_SD = 1).
11. Communications interface peripherals generally require an accurate, stable peripheral bus frequency and provide clock prescalers to configure the module for a required or desired transfer rate. Peripherals may constrain the accuracy of the system/peripheral clock and some transfer rates may be unsupported at some

peripheral clock frequencies. This should be determined from the **56F8000 Peripheral Reference Manual**.

12. When using the ROSC as the primary clock source, the TRIM field in the OCCS_OCTRL register must be initialized at start-up to the factory-provided value which can be obtained from the FM_OPT1 register of the Flash Module (FM). This is done automatically by the Freescale software development tools and insures that a ROSC frequency error will not exceed 2.8% over temperature. This insures that frequency accuracy is sufficient to permit correct operation of the part's communication interfaces over the device's allowed operating range.
13. The ADC peripheral clock frequency (MSTR_2X divided by 2) after division per the ADC CLKDIV field must produce an ADC conversion clock in the range 100KHz to 5.33MHz (32MHz divided by 6).
14. When operating in non-looping Scan modes, the scan duration (as determined by the Scan mode, number of samples per scan, conversion clock frequency, and PUDELAY) must be configured so that a scan completes within the period available per the scan frequency.
15. While GPIOB6 is being used as an external clock source (PRECS = 1), the GPIOB6 pad must remain configured as a GPIO input (this is the reset default) in order to avoid contention with the clock input signal (GPIOB_PEREN[6]=0, GPIOB_DDIR[6] = 0).
16. TCLK frequency must not exceed 1/8 of the system bus frequency.
17. Set ONCE_EBL in SIM_CTRL = 1 when doing real-time debugging to insure that debug registers in the core being accessed from the applications code are clocked, regardless of the state of the core TAP.
18. Flash program and erase functions require a minimum system bus frequency of 1MHz. The clock must be sourced from the ROSC in normal mode (ROSB = 0, ROPD = 0) or from an external clock of at least 2MHz in order to perform Flash program or erase.

7. References

The following references can be found on the Freescale web site at:
http://www.freescale.com

1. *56F8000 Peripheral Reference Manual*, MC56F8000RM, Freescale Semiconductor, Inc.
2. *56F801x Technical Data* document for the specific device being implemented, MC56F801x, Freescale Semiconductor, Inc.
3. *DSP56800E Reference Manual*, DSP56800ERM, Freescale Semiconductor, Inc.

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