Freescale Semiconductor
Application Note

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MC13783 Recommended Audio Output SPI Sequences

by: Power Management and Audio Applications Team

1 Introduction

This document describes the recommended audio output SPI sequences for the MC13783 to ensure proper start up of the digital audio converters. The recommended audio output SPI sequences minimize undesirable speaker noises—such as, pops, garbled audio.

2 CODEC Startup From Full Audio Shutdown

Table 1 provides the CODEC startup sequences from full audio shutdown. The CODEC is the only audio source of interest. This use case activates the audio subsystem to use the voice CODEC for Tx and Rx audio. Bit settings designated as "X" are "don't care" or depend on the specific intended application, for example, which output amplifier path to activate, and so on.

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NOTE

It is assumed that the VAUDIO regulator is enabled and in full power mode before any of the SPI sequences are attempted.

The “don't care” bits (X) signify that the actual value programmed is not important to the success of the SPI sequence. However, the step in which the bit is programmed is still important. The actual value of these bits will be determined by each specific application.

Table 1. CODEC Startup From Full Audio Shutdown

Sequence	Register	Bit #	Bit Name	Bit Value	Notes
1	36	1	BIASEN	1	Enable Audio Bias.
	36	2	BIASSPEED	0	Slow Ramp.
2[1]	SW	WAIT	WAIT	250 ms	Wait for AUDIO BIAS to reach full value.
3	39	2	CDCTXRXSLOT0	X	—
	39	3	CDCTXRXSLOT1	X	—
	39	4	CDCTXSECSLOT0	X	—
	39	5	CDCTXSECSLOT1	X	—
	39	6	CDCRXSECSLOT0	X	—
	39	7	CDCRXSECSLOT1	X	—
	39	8	CDCRXSECGAIN0	X	—
	39	9	CDCRXSECGAIN1	X	—
	39	10	CDCSUMGAIN	X	—
	39	11	CDCFSDLY	X	FSYNC delay relative to BCLK.
4	40	0	CDCSSISEL	X	—
	40	1	CDCCLKSEL	X	—
	40	2	CDCSM	X	—
	40	3	CDCBCLINV	X	—
	40	4	CDCFSINV	X	—
	40	5	CDCFS0	X	—
	40	6	CDCFS1	X	—
	40	7	CDCCLK0	X	—
	40	8	CDCCLK1	X	—
	40	9	CDCCLK2	X	—
	40	10	CDCFS8K16K	X	—
	40	11	CDCEN	1	—
	40	12	CDCCLKEN	X	—
	40	13	CDCTS	0	—
	40	14	CDCDITH	X	—
	40	15	CDCRESET	1	CDCRESET must be set.
	40	16	CDCBYP	X	—
	40	17	CDCALM	X	—
	40	18	CDCDLM	X	—
	40	20	AUDOHPF	X	—
5	40	Same as previous step.			Rewrite REG 40 with previous step settings.

Table 1. CODEC Startup From Full Audio Shutdown (continued)

Sequence	Register	Bit #	Bit Name	Bit Value	Notes
6	SW	WAIT	WAIT	15 ms	Wait for data converter to settle.
7	37	0	PGARXEN	1	—
	37	1	PGARX0	X	—
	37	2	PGARX1	X	—
	37	3	PGARX2	X	—
	37	4	PGARX3	X	—
	37	5	PGASTEN	0	—
	37	10	ARXINEN	0	—
	37	16	MONO0	X	—
	37	17	MONO1	X	—
	37	18	BAL0	X	—
	37	19	BAL1	X	—
	37	20	BAL2	X	—
	37	21	BALLR	X	—
8	36	3	ASPEN	X	Choose an output path.
	36	4	ASPSEL	X	
	36	5	ALSPEN	X	
	36	7	ALSPSEL	X	
	36	9	AHSREN	X	
	36	10	AHSLEN	X	
	36	11	AHSSEL	X	
	36	15	ARXOUTREN	X	
	36	16	ARXOUTLEN	X	
	36	17	ARXOUTSEL	X	
	36	18	CDCOUTEN	X	
	36	21	ADDCDC	X	
	36	22	ADDSTDC	0	
	36	23	ADDRXIN	0	
	49	14	CONMODE0	X	
	49	15	CONMODE1	X	
	49	16	CONMODE2	X	

[1] If the slow bias WAIT times cannot be tolerated, the FAST BIAS setting can be used. However, the best possible pop-noise performance will not be achieved if the fast bias is used. Table 2 provides the bit settings and WAIT time changes when using the fast bias. All other bit settings remain the same.

Table 2. CODEC FAST BIAS Setting

Sequence	Register	Bit #	Bit Name	Bit Value	Notes
1	36	1	BIASEN	1	Enable Audio Bias.
	36	2	BIASSPEED	1	Fast Ramp.
2	SW	WAIT	WAIT	25 ms	Wait for AUDIO BIAS to reach full value.

3 SDAC Startup From Full Audio Shutdown

Table 3 provides the SDAC startup sequences from full audio shutdown. The SDAC is the only audio source of interest. This use case activates the 16-bit stereo DAC for Rx path audio playback. Bit settings designated as "X" are "don't care" or depend on the specific intended application, for example, which output amplifier path to activate, and so on.

Table 3. SDAC Startup From Full Audio Shutdown

Sequence	Register	Bit #	Bit Name	Bit Value	Notes
1	36	1	BIASEN	1	Enable Audio Bias.
	36	2	BIASSPEED	0	Slow Ramp.
2[1]	SW	WAIT	WAIT	250 ms	Wait for AUDIO BIAS to reach full value.
3	39	12	STDCSLOTS0	X	—
	39	13	STDCSLOTS1	X	—
	39	14	STDCRXSLOT0	X	—
	39	15	STDCRXSLOT1	X	—
	39	16	STDCRXSECSLOT0	X	—
	39	17	STDCRXSECSLOT1	X	—
	39	18	STDCRXSECGAIN0	X	—
	39	19	STDCRXSECGAIN1	X	—
	39	20	STDCSUMGAIN	X	—
4	40	13	CDCTS	X	—
5	41	0	STDCSSISEL	X	—
	41	1	STDCCLKSEL	X	—
	41	2	STDCSM	X	—
	41	3	STDCBCLINV	X	—
	41	4	STDCFSINV	X	—
	41	5	STDCFS0	X	—
	41	6	STDCFS1	X	—
	41	7	STDCCLK0	X	—
	41	8	STDCCLK1	X	—
	41	9	STDCCLK2	X	—
	41	10	STDCFSDLYB	X	FSYNC delay relative to BCLK.
	41	11	STDCEN	1	—
	41	12	STDCCLKEN	X	—
	41	15	STDCRESET	1	STDCRESET must be set.
	41	16	SPDIF	0	—
	41	17	SR0	X	—
	41	18	SR1	X	—
	41	19	SR2	X	—
	41	20	SR3	X	—
6	41	Same as previous step.			Rewrite REG 41 with previous step settings.
7	SW	WAIT	WAIT	10 ms	Wait for data converter to settle.

Table 3. SDAC Startup From Full Audio Shutdown (continued)

Sequence	Register	Bit #	Bit Name	Bit Value	Notes
8	37	0	PGARXEN	0	—
	37	5	PGASTEN	1	—
	37	6	PGAST0	X	—
	37	7	PGAST1	X	—
	37	8	PGAST2	X	—
	37	9	PGAST3	X	—
	37	10	ARXINEN	0	—
	37	16	MONO0	X	—
	37	17	MONO1	X	—
	37	18	BAL0	X	—
	37	19	BAL1	X	—
	37	20	BAL2	X	—
	37	21	BALLR	X	—
9	36	3	ASPEN	X	Choose an output path.
	36	4	ASPSEL	X	
	36	5	ALSPEN	X	
	36	7	ALSPSEL	X	
	36	9	AHSREN	X	
	36	10	AHSLEN	X	
	36	11	AHSSEL	X	
	36	15	ARXOUTREN	X	
	36	16	ARXOUTLEN	X	
	36	17	ARXOUTSEL	X	
	36	21	ADDCDC	0	
	36	22	ADDSTDC	1	
	36	23	ADDRXIN	0	
	49	14	CONMODE0	X	
	49	15	CONMODE1	X	
	49	16	CONMODE2	X	

[1] If the slow bias WAIT times cannot be tolerated, the FAST BIAS setting can be used. However, the best possible pop-noise performance will not be achieved if the fast bias is used. The bit setting and WAIT time changes for using the fast bias are provided in Table 4. All other bit settings remain the same.

Table 4. SDAC FAST BIAS Setting

Sequence	Register	Bit #	Bit Name	Bit Value	Notes
1	36	1	BIASEN	1	Enable Audio Bias.
	36	2	BIASSPEED	1	Fast Ramp.
2	SW	WAIT	WAIT	25 ms	Wait for AUDIO BIAS to reach full value.

4 CODEC Full Audio Shutdown From On State

Table 5 provides the sequence for the CODEC full audio shutdown from on state. This sequence is recommended for deactivation of the voice CODEC subsystem.

Table 5. CODEC Full Audio Shutdown From On State

Sequence	Register	Bit #	Bit Name	Bit Value	Notes
1	36	3	ASPEN	0	Disable output path previously enabled.
	36	5	ALSPEN	0	
	36	9	AHSREN	0	
	36	10	AHSLEN	0	
	36	15	ARXOUTREN	0	
	36	16	ARXOUTLEN	0	
	36	18	CDCOUTEN	0	
	36	21	ADDCDC	0	
	49	14	CONMODE0	0	
	49	15	CONMODE1	0	
	49	16	CONMODE2	0	
2	37	0	PGARXEN	0	—
3	40	11	CDCEN	0	—
	40	12	CDCCLKEN	0	—
	40	13	CDCTS	1	—
4	36	1	BIASEN	0	—

5 SDAC Full Audio Shutdown From On State

Table 6 provides the sequence for the SDAC full audio shutdown from on state. This sequence is recommended for deactivation of the 16-bit stereo DAC subsystem.

Table 6. SDAC Full Audio Shutdown From On State

Sequence	Register	Bit #	Bit Name	Bit Value	Notes
1	36	3	ASPEN	0	Disable output path previously enabled.
	36	5	ALSPEN	0	
	36	9	AHSREN	0	
	36	10	AHSLEN	0	
	36	15	ARXOUTREN	0	
	36	16	ARXOUTLEN	0	
	36	22	ADDSTDC	0	
	49	14	CONMODE0	0	
	49	15	CONMODE1	0	
	49	16	CONMODE2	0	
2	37	5	PGASTEN	0	—
3	41	11	STDCEN	0	—
	41	12	STDCCLKEN	0	—
4	36	1	BIASEN	0	—

6 CODEC On and SDAC Off Transition to CODEC Off and SDAC On

Table 7 provides the sequence to transition the CODEC on and SDAC off to CODEC off and SDAC on. This sequence is recommended to switch the audio subsystem from 13-bit voice mode to16-bit stereo mode. Bit settings designated as "X" are "don't care" or depend on the specific intended application.

Table 7. CODEC On and SDAC Off Transition to CODEC Off and SDAC On

Sequence	Register	Bit #	Bit Name	Bit Value	Notes
1	36	3	ASPEN	0	Disable output path previously enabled.
	36	5	ALSPEN	0	
	36	9	AHSREN	0	
	36	10	AHSLEN	0	
	36	15	ARXOUTREN	0	
	36	16	ARXOUTLEN	0	
	36	18	CDCOUTEN	0	—
	36	21	ADDCDC	0	—
	49	14	CONMODE0	0	—
	49	15	CONMODE1	0	—
	49	16	CONMODE2	0	—
2	37	0	PGARXEN	0	—
3	40	11	CDCEN	0	—
	40	12	CDCCLKEN	0	—
	40	13	CDCTS	X	—
4	39	12	STDCSLOTS0	X	—
	39	13	STDCSLOTS1	X	—
	39	14	STDCRXSLOT0	X	—
	39	15	STDCRXSLOT1	X	—
	39	16	STDCRXSECSLOT0	X	—
	39	17	STDCRXSECSLOT1	X	—
	39	18	STDCRXSECGAIN0	X	—
	39	19	STDCRXSECGAIN1	X	—
	39	20	STDCSUMGAIN	X	—

Table 7. CODEC On and SDAC Off Transition to CODEC Off and SDAC On (continued)

Sequence	Register	Bit #	Bit Name	Bit Value	Notes
5	41	0	STDCSSISEL	X	—
	41	1	STDCCLKSEL	X	—
	41	2	STDCSM	X	—
	41	3	STDCBCLINV	X	—
	41	4	STDCFSINV	X	—
	41	5	STDCFS0	X	—
	41	6	STDCFS1	X	—
	41	7	STDCCLK0	X	—
	41	8	STDCCLK1	X	—
	41	9	STDCCLK2	X	—
	41	10	STDCFSDLYB	X	FSYNC delay relative to BCLK.
	41	11	STDCEN	1	—
	41	12	STDCCLKEN	X	—
	41	15	STDCRESET	1	STDCRESET must be set.
	41	16	SPDIF	0	—
	41	17	SR0	X	—
	41	18	SR1	X	—
	41	19	SR2	X	—
	41	20	SR3	X	—
6	41	Same as previous step.			Rewrite REG 41 with previous step settings.
7	SW	WAIT	WAIT	10 ms	Wait for data converter to settle.
8	37	5	PGASTEN	1	—
	37	6	PGAST0	X	—
	37	7	PGAST1	X	—
	37	8	PGAST2	X	—
	37	9	PGAST3	X	—
	37	10	ARXINEN	0	—
	37	16	MONO0	X	—
	37	17	MONO1	X	—
	37	18	BAL0	X	—
	37	19	BAL1	X	—
	37	20	BAL2	X	—
	37	21	BALLR	X	—

Table 7. CODEC On and SDAC Off Transition to CODEC Off and SDAC On (continued)

Sequence	Register	Bit #	Bit Name	Bit Value	Notes
9	36	3	ASPEN	X	Choose an output path.
	36	4	ASPSEL	X	
	36	5	ALSPEN	X	
	36	7	ALSPSEL	X	
	36	9	AHSREN	X	
	36	10	AHSLEN	X	
	36	11	AHSSEL	X	
	36	15	ARXOUTREN	X	
	36	16	ARXOUTLEN	X	
	36	17	ARXOUTSEL	X	
	36	21	ADDCDC	0	
	36	22	ADDSTDC	1	
	36	23	ADDRXIN	0	
	49	14	CONMODE0	X	
	49	15	CONMODE1	X	
	49	16	CONMODE2	X	

7 SDAC On and CODEC Off Transition to SDAC Off and CODEC On

Table 8 provides the sequence to transition the SDAC on and CODEC off to SDAC off and CODEC on. This sequence is recommended to switch the audio subsystem from the 16-bit stereo mode to 13-bit voice mode. Bit settings designated as "X" are "don't care" or depend on the specific intended application.

Table 8. SDAC On and CODEC Off Transition to SDAC Off and CODEC On

Sequence	Register	Bit #	Bit Name	Bit Value	Notes
1	36	3	ASPEN	0	Disable output path previously enabled.
	36	5	ALSPEN	0	
	36	9	AHSREN	0	
	36	10	AHSLEN	0	
	36	15	ARXOUTREN	0	
	36	16	ARXOUTLEN	0	
	36	22	ADDSTDC	0	
	49	14	CONMODE0	0	
	49	15	CONMODE1	0	
	49	16	CONMODE2	0	
2	37	5	PGASTEN	0	—
3	41	11	STDCEN	0	—
	41	12	STDCCLKEN	0	—

Table 8. SDAC On and CODEC Off Transition to SDAC Off and CODEC On (continued)

Sequence	Register	Bit #	Bit Name	Bit Value	Notes
4	39	2	CDCTXRXSLOT0	X	—
	39	3	CDCTXRXSLOT1	X	—
	39	4	CDCTXSECSLOT0	X	—
	39	5	CDCTXSECSLOT1	X	—
	39	6	CDCRXSECSLOT0	X	—
	39	7	CDCRXSECSLOT1	X	—
	39	8	CDCRXSECGAIN0	X	—
	39	9	CDCRXSECGAIN1	X	—
	39	10	CDCSUMGAIN	X	—
	39	11	CDCFSDLY	X	FSYNC delay relative to BCLK.
5	40	0	CDCSSISEL	X	—
	40	1	CDCCLKSEL	X	—
	40	2	CDCSM	X	—
	40	3	CDCBCLINV	X	—
	40	4	CDCFSINV	X	—
	40	5	CDCFS0	X	—
	40	6	CDCFS1	X	—
	40	7	CDCCLK0	X	—
	40	8	CDCCLK1	X	—
	40	9	CDCCLK2	X	—
	40	10	CDCFS8K16K	X	—
	40	11	CDCEN	1	—
	40	12	CDCCLKEN	X	—
	40	13	CDCTS	0	—
	40	14	CDCDITH	X	—
	40	15	CDCRESET	1	CDCRESET must be set.
	40	16	CDCBYP	X	—
	40	17	CDCALM	X	—
	40	18	CDCDLM	X	—
	40	20	AUDOHPF	X	—
6	40	Same as previous step.			Rewrite REG 40 with previous step settings.
7	SW	WAIT	WAIT	15 ms	Wait for data converter to settle.

Table 8. SDAC On and CODEC Off Transition to SDAC Off and CODEC On (continued)

Sequence	Register	Bit #	Bit Name	Bit Value	Notes
8	37	0	PGARXEN	1	—
	37	1	PGARX0	X	—
	37	2	PGARX1	X	—
	37	3	PGARX2	X	—
	37	4	PGARX3	X	—
	37	10	ARXINEN	0	—
	37	16	MONO0	X	—
	37	17	MONO1	X	—
	37	18	BAL0	X	—
	37	19	BAL1	X	—
	37	20	BAL2	X	—
	37	21	BALLR	X	—
9	36	3	ASPEN	X	Choose an output path.
	36	4	ASPSEL	X	
	36	5	ALSPEN	X	
	36	7	ALSPSEL	X	
	36	9	AHSREN	X	
	36	10	AHSLEN	X	
	36	11	AHSSEL	X	
	36	15	ARXOUTREN	X	
	36	16	ARXOUTLEN	X	
	36	17	ARXOUTSEL	X	
	36	18	CDCOUTEN	X	
	36	21	ADDCDC	X	
	36	22	ADDSTDC	0	
	36	23	ADDRXIN	0	
	49	14	CONMODE0	X	
	49	15	CONMODE1	X	
	49	16	CONMODE2	X	

8 Revision History

Table 9 summarizes revisions to this document since the release of the previous version (Rev. 1).

Table 9. Revision History

Location	Revision
Throughout document	Prepared for public release. No technical content changes.

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