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Application Note

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Using the S12XE Family as a Development Platform for the S12XS Family

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1 Introduction

This document will help designers maintain compatibility when using a member of the S12XE family as an emulation tool while developing an application targeted at a member of the S12XS family. Allowing for minor constraints, as detailed in each section, code can be written for an XE family device which then runs unmodified on XS family devices. This document is intended for use with the documents listed on the product summary page for S12X products (see http://www.freescale.com/automotive).

Documents:

- Data sheet MC9S12XEP100
- Data sheet MC9S12XS Family
- Product preview MC9S12XE Family
- Product preview MC9S12XS Family

Due to the timeline of devices launching from the 9S12XE family and the 9S12XS family, this document

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is mainly written with the assumption that a 9S12XE100 or 9S12XE512 will be used for the development part to transfer to a 9S12XS family member.

2 Overview of Families

Key considerations:

- Peripheral count
  - The XS family has a reduced peripheral set from the XE family
  - XS256 and XS128 devices have one MSCAN, one SPI, no IIC, no XGATE, one ATD, no ECT, no external bus, and only a standard TIM.
- Memory maps
  - The XS family devices has no emulated EEPROM (EEE), less RAM, and less data flash than an equivalent XE family device. Mapping of these modules is upwards compatible.
- Flash memory
  - The XS family offers flash ranges from 256K to 64K; the XE family offers flash ranges from 1.024M to 128K.

Table 1 shows a summary of feature-sets for XE family devices. All XE family devices are listed in the XE family product brief.

Table 1. Family Features

Device	Package	XGATE	CAN	SPI	SCI	IIC	ECT	TIM	PIT	A/D	PWM	I/O
9S12XE Family												
9S12XEP100	208 MAPBGA	Yes	5	3	8	2	8ch	8ch	8ch	2/32	8ch	152
	144 LQFP		5	3	8	2	8ch	8ch[1]	8ch	2/24	8ch	119
	112 LQFP		5	3	4	2	8ch	8ch0	4ch	1/16	8ch	91
9S12EXP768	208 MAPBGA		5	3	8	2	8ch	0	8ch	2/32	8ch	152
	144 LQFP		5	3	8	2	8ch	8ch[1]	8ch	2/24	8ch	119
	112 LQFP		5	3	4	2	8ch	8ch[1]	4ch	1/16	8ch	91
9S12XEQ512	144 LQFP		4	3	6	2	8ch	0	4ch	2/24	8ch	119
	112 LQFP		4	3	4	2	8ch	0	4ch	1/16	8ch	91
	80 QFP		4	3	2	2	8ch	0	4ch	1/8	8ch	59
9S12XEQ384	144 LQFP		4	3	4	1	8ch	0	4ch	2/24	8ch	119
	112 LQFP		4	3	4	1	8ch	0	4ch	1/16	8ch	91
	80 QFP		4	3	2	1	8ch	0	4ch	1/8	8ch	59
9S12XET256	144 LQFP		3	3	2	1	8ch	0	4ch	2/24	8ch	119
	112 LQFP		3	3	2	1	8ch	0	4ch	1/16	8ch	91
	80 QFP		3	3	2	1	8ch	0	4ch	1/8	8ch	59
9S12XEG128	112 LQFP	Yes [2]	2	2	2	1	8ch	0	2ch	1/16	8ch	91
	80 QFP		2	2	2	1	8ch	0	2ch	1/8	8ch	59

Table 1. Family Features (continued)

Device	Package	XGATE	CAN	SPI	SCI	IIC	ECT	TIM	PIT	A/D	PWM	I/O
9S12XS Family												
9S12XS256	112 LQFP	No	1	1	2	0	0	8ch	4ch	1/16	8ch	91
	80 QFP		1	1	2	0	0	8ch	4ch	1/8	7ch	59
	64 LQFP		1	1	2	0	0	8ch	4ch	1/8	6ch	44
9S12XS128	112 LQFP		1	1	2	0	0	8ch	4ch	1/16	8ch	91
	80 QFP		1	1	2	0	0	8ch	4ch	1/8	7ch	59
	64 LQFP		1	1	2	0	0	8ch	4ch	1/8	6ch	44
9S12XS64	112 LQFP		1	1	2	0	0	8ch	4ch	1/16	8ch	91
	80 QFP		1	1	2	0	0	8ch	4ch	1/8	7ch	59
	64 LQFP		1	1	2	0	0	8ch	4ch	1/8	6ch	44

1 Internal only, not bonded out

2 Can execute code only from RAM

2.1 Part IDs

Each device has a unique identifier value encoded in the Part ID register. This value may be decoded by an application and appropriate routines selected for the device. See Section 4, “Part IDs,” for details.

3 XE and XS Module Summary

3.1 Device Memory Maps

Local and global memory maps are compatible for the XE and XS families. Out of reset, the families have equivalent maps and default values. For devices with smaller memory sizes, those areas are unused in the map and cause a reset if accessed. To maintain compatibility, ensure code development on an XE device accesses only the memory locations implemented on the XS device. See Figure 1 for local and global map comparisons for the 9S12XE100 and 9S12XS256 devices.

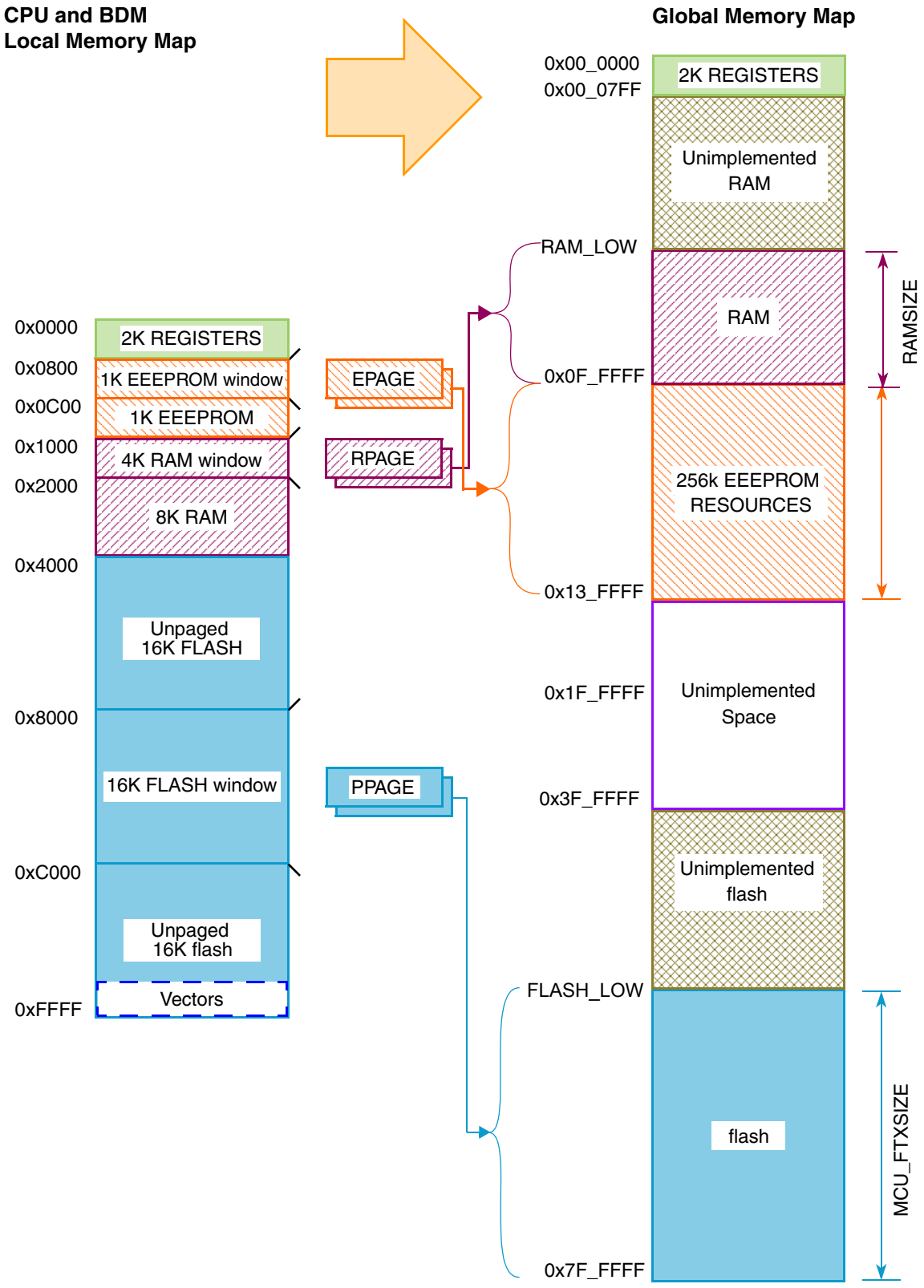

Figure 1. MC9S12XE Global Memory Map

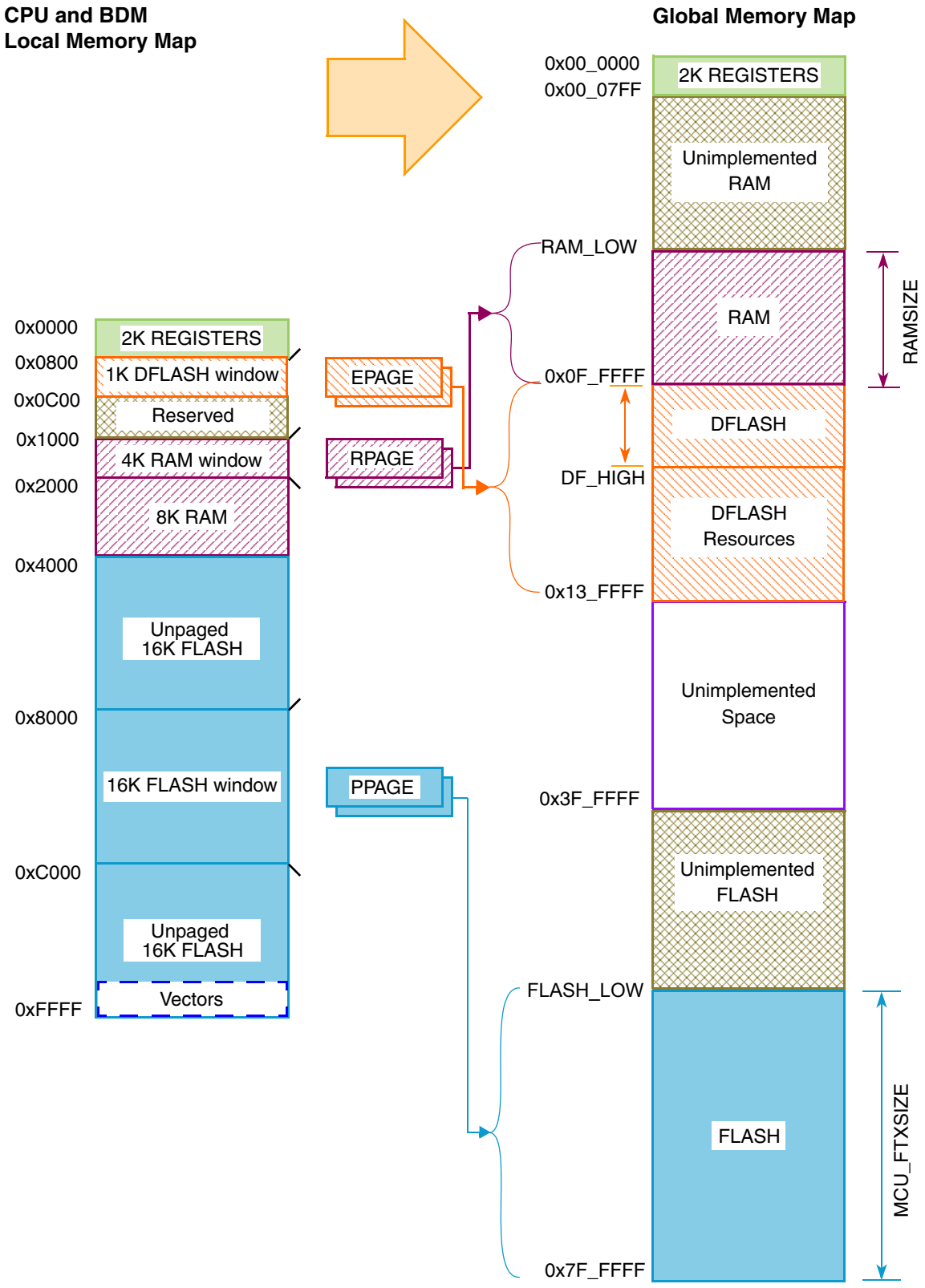

Figure 2. MC9S12XS Global Memory Map

3.1.1 Flash Memory Maps

The XE family offers higher flash sizes than the XS family. Compatibility can be maintained by not accessing areas of flash unimplemented on the XS family. The 9S12XE100 contains five physical flash blocks. The S12XS family has one physical flash block. Table 2 summarizes the size and block number for each family member's physical flash block.

Table 2. Physical Flash Block

Device	0x70_0000	0x72_0000	0x74_0000	0x76_0000	0x78_0000	0x7A_0000	0x7C_0000	0x7E_0000
9S12XEx100	B3		B2		B1S	B1N	B0	
9S12XEx768								
9S12XEx512								
9S12XEx384								
9S12XEx256								B0(128K)
9S12XEx128								
9S12XS256							B0	
9S12XS128								B0(128K)
9S12XS64								B0(64K)

To maintain compatibility when developing on a 9S12XE100 device for a 9S12XS256:

- Use only the flash memory in B0, global address range 0x7C_0000 to 0x7F_FFFF.

For a 9S12XS128:

- Use only the flash in range 0x7E_0000 to 0x7F_FFFF

For a 9S12XS64:

- Use only the flash in range 0x7F_0000 to 0x7F_FFFF.

NOTE

Because the XS family does not have expanded bus available, the MMC Control Register (MMCCTL1) should be left with default values ROMHM=RAMHM=0. ROMHM=0 (reset value) and 16-Kbyte unpaged flash is visible in the local map address range 0x4000 to 0x7FFF. This enables a linear space in the local map with the visible PPAGEs: 0xFF (0xC000 – 0xFFFF), 0xFE (0x8000 – 0xBFFF), and 0xFD (0x4000 – 0x7FFF) for the XE and XS devices. Do not access PPAGEs less than 0xF0 when developing for a 9S12XS256, less than 0xF8 when developing for a 9S12XS128, or less than 0xFC when developing for a 9S12XS64.

3.1.2 D-Flash

The XS family offers D-flash (data flash) in place of emulated EEPROM (EEE) on the XE family. Because the EEE on the XE family is a combination of EEE-buffer RAM and data flash, compatibility can be maintained when developing code to move between the two families.

The D-flash on the XE device can be configured so the code can be dropped into an XS device. However, there are some key differences to be noted, but compensating for these differences can ensure a seamless transfer. The main differences are due to the removal of EEE functionality on XS device. These key differences are within the memory map, register locations, protection scheme, and commands.

3.1.2.1 Memory Map

Memory map changes as implemented space dedicated to EEE functionality on the XE device becomes reserved space on the XS devices.

Flash configuration fields between the two families differ for the protection of the EEE and D-flash. The global address 0x7F_FF0D is the D-flash protection byte on the XS devices and the EEE Protection byte on the XE devices. See Section 3.1.2.2, “FTM Register Differences,” for more details.

On the XE family, the memory between global addresses 0x10_0000 to 0x13_FFFF is defined as the EEE resource memory map. On the XS family, this space is defined as the D-flash and memory controller resource memory map. Table 3 shows the portions of memory within the global address space of 0x10_0000 to 0x13_FFFF that become reserved with the removal of EEE functionality on the XS devices. To maintain compatibility between the two families, the EEE resources for buffer RAM and Tag RAM should not be written or accessed.

Table 3. D-Flash Memory Map

Global Address	XE device description	XS device description
0x10_0000 – 0x10_7FFF	D-Flash Memory (User and EEE)	D-Flash Memory (User)
0x10_8000 – 0x11_FFFF	Reserved	Reserved
0x12_0000 – 0x12_007F	EEE Nonvolatile Information Register (EEEIFRON1 = 1)	D-Flash Nonvolatile Information Register (DFIFRON[1] = 1)
0x12_0080 – 0x12_0FFF	Reserved	Reserved
0x12_1000 – 0x12_1EFF	Reserved	Reserved
0x12_1FC0 – 0x12_1FFF	EEE Tag RAM (TMGRAMON1 = 1)	Reserved
0x12_2000 – 0x12_3BFF	Reserved	Reserved
0x12_3C00 – 0x12_3CFF	Memory Controller Scratch RAM (TMGRAMON1 = 1)	Reserved
0x12_3D00 – 0x12_3FFF	—	Memory Controller Scratch RAM (MGRAMON1 = 1)
0x12_4000 – 0x12_DFFF	Reserved	Reserved
0x12_E000 – 0x12_FFFF	Reserved	Reserved
0x13_0000 – 0x13_EFFF	Reserved	Reserved
0x13_F800 – 0x13_FFFF	Buffer RAM (User and EEE)	Reserved

[1] The MMCCTL1 register bit and location of register is the same for XE and XS families at 0x13.

The D-flash can be accessed on the local memory map through the EPAGE for the XE and XS families. For both families, the EPAGE register has the same default value out of reset of 0xFE. On the XE family, the 1-Kbyte EPAGE window (0x0800 – 0x0BFF) can access any 1-Kbyte range within the 256-Kbyte global range (0x10_0000 – 0x13_FFFF). On the XS family, the EPAGE can access any 1-Kbyte range within the 256-Kbyte global range (0x10_0000 – 0x13_FFFF). However, because there is no EEE functionality, the range from 0x13_0000 – 0x13_FFFF is reserved space. To maintain compatibility between the two families, only equivalent EPAGEs should be accessed. Table 4 shows the D-flash memory space and corresponding EPAGEs for the 9S12XE100 device versus the XS family. The 1-Kbyte fixed EEE page on the local map corresponds to EPAGE 0xFF on the XE devices, which is reserved on the XS devices. Therefore, on the XS devices, the 1-Kbyte fixed paged on the local memory map is reserved space and should not be accessed.

Table 4. D-Flash and EPAGEs

Device	Global Data Flash Range	D-Flash EPAGEs	Size
9S12XEx100	0x10_0000 – 0x10_7FFF	0x00 – 0x1F	32k
9S12XS256	0x10_0000 – 0x10_1FFF	0x00 – 0x07	8k
9S12XS128	0x10_0000 – 0x10_1FFF	0x00 – 0x07	8k
9S12XS64	0x10_0000 – 0x10_0FFF	0x00 – 0x03	4k

3.1.2.2 FTM Register Differences

There are also differences in the FTM registers between the XE and XS families with the removal of the EEE functionality from the XS family.

On the XE family, the ETAG (EEE Tag Counter Register) used by the memory controller to count number of updates to the D-flash is a reserved register on the XS family. The register is located at 0x010C – 0x010D. It is never writeable for either family and is unnecessary to read when writing code for a XS device.

The protection on XE devices is different from the XS devices, due to the removal of EEE functionality from the XS family. It is possible to maintain code compatibility when developing on the XE family for transfer to a XS device, with careful set up of this register. The protection register is located at 0x00_0109 for both families. The register is the EPROT on the XE family and is the DFPROT on the XS family. On the XE family, bit 7 enables or disables protection on the entire buffer RAM EEE from writes. Bit 7 enables or disables protection on the D-flash memory within the defined address range selected by bits 4:0 from writes or erase. Bit 4 on the XE family enables or disables protection on the address range specified by bits 3:0. On the XS family, bit 4 is part of the address range selection for setting protection. Writing to the EPROT register on the XE devices without the EEE enabled has no effect. When developing code to transfer from a XE device to a XS device, it is possible to write the desired DFPROT value to the EPROT register. If using this suggested method, the XE device is not protected against writes or erase in the D-flash memory. When the code is placed in to a XS device, protection is valid.

3.1.2.3 FTM Command Differences

The commands that pertain specifically to the EEE on the XE family become invalid on the XS family. To maintain compatibility, do not use the commands that are for EEE functionality. Table 5 shows a side-by-side comparison of commands not valid for the XS family.

Table 5. D-Flash Commands on XE-Family vs. XS-Family

FCMD	Command	XE-Family	XS-Family
0x01	Erase Verify All Blocks	X	X
0x02	Erase Verify Block	X	X
0x08	Erase All Blocks	X	X
0x09	Erase Flash Block	n/a	X
0x0B	Unsecure Flash	X	X
0x0D	Set User Margin Level	X	X
0x0E	Set Field Margin Level	X	X
0x0F	Full Partition D-Flash	X	invalid
0x10	Erase Verify D-Flash Section	X	X
0x11	Program D-Flash	X	X
0x12	Erase D-Flash Sector	X	X
0x13	Enable EEPROM Emulation	X	invalid
0x14	Disable EEPROM Emulation	X	invalid
0x15	EEPROM Emulation Query	X	invalid
0x20	Partition D-Flash	X	invalid

3.1.3 RAM Map

The RAM memory maps are compatible between the XE and XS families, with smaller implemented sizes for the XS family. Compatibility can be maintained by not accessing areas of unimplemented RAM on the XS family.

The RAM memory sizes are mapped from the higher-order address to the lower-order address. The RPAGE register has equivalent default values for XE devices and XS devices out of reset, 0xFD. For simplicity, the RPAGE register should be left with this value. Table 6 shows a comparison of the XE and XS devices' RAM locations for local and global maps.

Table 6. RAM Addresses[1]

Device	Global Address Range	Local Address Range	4K RPAGE	Size
9S12XEx100	0x0F_0000 – 0x0F_FFFF	0x1000 – 0x1FFF	0xF0 – 0xFD	64K
		0x2000 – 0x3FFF	FE & 0xFF (fixed window)	
9S12XS256	0x0F_D000 – 0x0F_FFFF	0x1000 – 0x1FFF	0xFD	12K
		0x2000 – 0x3FFF	FE & 0xFF (fixed window)	
9S12XS128	0x0F_E000 – 0x0F_FFFF	unimplemented	unimplemented	8k
		0x2000 – 0x3FFF	FE & 0xFF (fixed window)	
9S12XS64[2]	0x0F_F000 – 0x0F_FFFF	Unimplemented	Unimplemented	4k
		0x3000 – 0x3FFF	0xFF (fixed window)	

1 Table 6 assumes RAMHM=ROMHM=0 for the XE family. Not applicable for XS family.

2 The 9S12XS64 uses the 9S12XS128 die. RAH address ranges 2000 – 2FFF are untested and should not be used for reliability purposes.

3.2 Memory Protection Unit (MPU)

The XS family does not have a MPU. To maintain compatibility, do not use the MPU module on the XE device. The U bit is not present in the condition-code register (CCR) on the XS devices.

3.3 Signal Description

Packages and pin-outs are equivalent for 112 LQFP, 80 QFP, and 64 LQFP are upwards compatible. For a module on the XE family unimplemented on XS family devices, its I/O functions are unavailable on associated ports. All other appropriate I/O pin functions are compatible.

The module routing is not equivalent for the XE and XS families. However, the pinouts after reset are equivalent. On the XS Family, CAN0 routing options are removed and extra options are added for SCI1, TIM, and PWM. To maintain compatibility between the two families, modules routing for pinouts should be left to default reset conditions.

3.4 System Clock

The system-clock distribution is compatible.

3.5 Modes of Operation

Chip configuration is backwards compatible between XE and XS families. The XS family does not have an external bus. Therefore, to maintain compatibility, do not use expanded or emulation modes. All other modes are equivalent for power mode, freeze mode, and system state.

3.6 Security

Security for XE and XS family is compatible with the options/security byte located at global address 0x7F_FF0F for both device families.

3.7 Resets and Interrupts/Vector Tables

Resets and interrupts are functionally compatible for the CPU. To maintain compatibility, do not route interrupts to the XGATE or have the XGATE interrupt the CPU. The vector locations are reserved where an interrupt is associated with a module not used on the XS family. For compatibility, these locations must remain unimplemented and unprogrammed or configured to point to a TRAP routine.

3.8 CPU12X

The CPU12X is compatible for low-power modes, background-debug mode, memory mapping control, and interrupt handling.

The XE devices have a maximum bus frequency of 50 MHz; the XS devices are specified at a maximum of 40 MHz. To maintain compatibility, do not exceed a bus frequency of 40 MHz.

The XS family does not have the MPU (memory protection unit), but the XE family does. CPU12X-1 is used for the XS family, and CPU12X-2 is used for the XE family. The U-bit is used in the CPU12X-2 condition code register that controls the system for user and supervisor states and removed in CPU12X-1.

The CPU and BDM on the XE family can access resources on different target busses in the same cycle, because all internal and external resources are connected to specific target busses. The XS family has one target bus for all the available resources. Therefore, to maintain compatibility between the families, do not use the CPU and BDM for simultaneous accesses.

3.9 Oscillator

The XE and XS families are compatible.

3.10 Clock and Reset Generator (CRG)

CRG modules are compatible.

3.11 Timer (TIM)

The XE and XS families have a standard timer module (TIM) but route to different I/O ports. The TIM module on the XE devices routes to port R; the XS devices routes to port T. Using the enhanced-capture-timer module (ECT) and only standard timer functions maintain code compatibility when developing an XE device to convert to an XS device. Compatibility is maintained because both modules route to port T and the ECT is a super set of the TIM functions.

Common functions of the TIM and ECT:

- A 16-bit counter
- A timer-overflow interrupt
- Up to eight input/output compare functions
- A 16-bit pulse accumulator

The ECT super set of functions that should not be used when implementing a TIM:

- 16-bit buffer registers on input-capture channels 0 to 3.
- User selectable delay counters on channels 0 to 3 for increased noise immunity.
- A 2nd 16-bit pulse accumulator (event-counter mode) on channel 0.
- Four, 8-bit, buffered pulse accumulators (event-counter mode) on channels 0 to 3
- A 16-bit modulus-down counter with 4-bit prescaler.

NOTE

On the ECT, the pulse accumulator is A or B; on the TIM, it is only referred to as the pulse accumulator.

3.12 Enhanced Capture Timer (ECT)

The XS family does not have an ECT module. To maintain code compatibility, use only the TIM functions of the ECT module.

3.13 Analog to Digital Converter (ATD)

The XE family has two, 16-channel ATD converters; the XS family has one, 16-channel ATD. To maintain code compatibility, use only ATD0 on the XE device when developing for an XS device.

3.14 Inter IC Interface (IIC)

The XS family does not have IIC. To maintain compatibility, do not use the IIC module on the XE device.

3.15 Serial Communications Interface (SCI)

SCI modules are compatible. The XS family has only two SCIs. Additional multiplexing is available on the XS devices for SCI1. To maintain compatibility, use only SCI0 and SCI1; module routing should be left to default reset condition of port S [2:3].

3.16 Serial Peripheral Interface (SPI)

The SPI module is compatible. The XS family has only one SPI. To maintain code compatibility, use only SPI0 on the XE device.

3.17 Pulse Width Modulator (PWM)

PWM modules are compatible.

3.18 MSCAN

The MSCAN modules are compatible. The XS family has only one CAN module. To maintain code compatibility, use only MSCAN0 and leave default routing on XE family to PM0 and PM1. On the XS family, CAN0 only routes to PM0 and PM1.

3.19 Port-Integration Module (PIM)

Because the XE and XS families have a different set of peripherals, differences in the PIM must be considered. The PIM module on all XE and XS family devices contains the same port control and status registers and is compatible when used as general purpose I/O (GPIO).

Unavailable ports on the XS devices are port F, L, and R. Therefore, to maintain compatibility, do not use these ports for general purpose I/O or module routing.

- Because each device has a different number of peripherals requiring I/O multiplexing, some larger devices' functions are unavailable on a smaller device where an equivalent module is unused. Module routing reset conditions are equivalent for the XE and XS devices.
- SPI0 has equivalent multiplexing options. See Table 7 for details. The XS has additional module-routing options for the TIM, PWM, SCI0 and SCI1 that are unavailable on XE devices. To maintain these modules' code compatibility, leave them to route to the port's reset condition.

Table 7. SPI0 Module Routing

Module	Related Pins			
SPI0	MISO	MOSI	SCK	SS
	PS4	PS5	PS6	PS7
	PM2	PM4	PM5	PM3

Where a module on an XE family device is not implemented on XS devices, its functionality is unavailable on the appropriate I/O pins. For example, port A and B are available for addressing in expanded modes and GPIO on the XE family, but are only available for use as GPIO on the XS devices.

3.20 Voltage Regulator (VREG)

VREG is compatible.

3.21 XGATE

XS family does not have a XGATE module. To maintain code compatibility, do not use XGATE module on the XE device.

3.22 Enhanced Interrupt Module (XINT)

Interrupt modules are compatible for CPU. To maintain compatibility, do not route interrupts to the XGATE.

4 Part IDs

The part ID is located in two, 8-bit registers PARTIDH and PARTIDL (addresses 0x001A and 0x001B) for XE and XS families. The read-only value is a unique part ID for each device revision. Table 8 shows the assigned part ID number and mask-set number for each device.

The coding is as follows:

- Bit 15–12: Major family identifier
- Bit 11–8: Minor family identifier
- Bit 7–4: Major mask-set-revision number including FAB transfers
- Bit 3–0: Minor — non full — mask-set revision

Table 8. Part IDs

Device	Mask Set Number	Part ID
MC9S12XEP1OO	2MR8H	0xCC92
MC9S12XS256	0M05M	0xC0C0
MC9S12XS128	0M04M	0xC1C0
MC9S12XS64	0M04M	0xC1C0
	TBD	0xC2C0

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