Freescale Semiconductor
Application Note

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MC9RS08KA Application Hints

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1 Introduction

MC9RS08KA microcontrollers and many other MCUs have features and characteristics that need to be understood for their best performance and to avoid common application issues and pitfalls. The techniques described here are useful for most of the microcontroller devices available in the market and are good application development practices. These techniques and hints are aimed at avoiding EMI, noise, and marginal designs that may disturb circuit operation and cause system malfunctions.

A robust application circuit design is achieved by detailed definition of product operation environment, good knowledge of MCU characteristics, careful device selection and PCB layout, good filtering, decoupling and termination techniques. This is all complemented by good software development techniques. Those items are detailed in the following sections.

2 Shared Pins

Shared pins, required to achieve low pin-count, require a careful selection of pin allocation on the application circuit. Proper termination and filtering at critical pins, such as $\overline{\text{RESET}}$, is also required to avoid operation issues or an inadvertent mode change.

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2.1 Pin Considerations

External V_{PP} voltage (typically 12 V) is required on the PTA2/KBIP2/TCLK/$\overline{\text{RESET}}$/V_{PP} pin when performing flash programming or erasing. The V_{PP} connection is always connected to the internal flash module regardless of the pin function. To avoid over stressing the flash, external V_{PP} voltage must be removed and a voltage higher than V_{DD} must be avoided when flash programming or erasing is not taking place.

The BKGD/MS (background / mode select) function is shared with an output-only pin PTA3 and the analog comparator output. In reset, the pin functions as a mode select pin. Immediately after reset rises, the pin functions as the background pin and can be used for background debug communication. While functioning as a BKGD/MS pin, this pin has an internal pullup device enabled. To use as an output-only port, the background debug mode pin enable bit in system option register must be cleared.

If nothing is connected to this pin, the MCU enters normal operating mode at the rising edge of reset. If a debug system is connected to the 6-pin standard background debug header, it can hold BKGD/MS low during the power-on-reset, which forces the MCU to active background mode.

The BKGD pin is used primarily for background debug controller (BDC) communications using a custom protocol that uses 16 clock cycles of the target MCU's BDC clock per bit time. The target MCU's BDC clock equals the bus clock rate; therefore, no significant capacitance should be connected to the BKGD/MS pin that could interfere with background serial communications.

Although the BKGD pin is a pseudo open-drain pin, the background debug communication protocol provides brief, actively driven, high-speed pulses to ensure fast rise times. Small capacitances from cables and the absolute value of the internal pullup device play almost no role in determining rise and fall times on the BKGD pin.

2.2 Pin Connection Considerations

Pins with shared functions should ideally be used on short connection lines that are far away from noisy circuitry. Careful port-to-function allocation is recommended. See Figure 1. To avoid extra current drain from floating input pins, the reset initialization routine in the application program should enable on-chip pullup/pulldown devices or change the direction of unused pins to outputs.

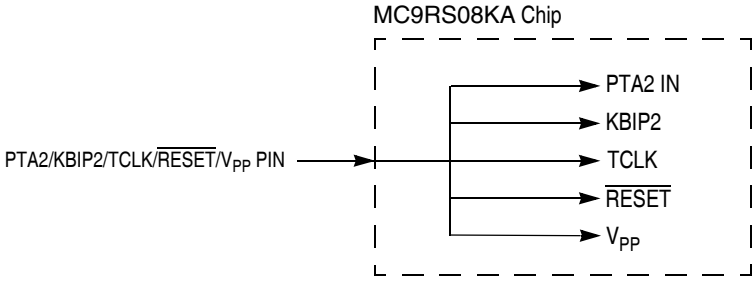


Figure 1. MC9RS08KA Shared Function Example

3 Power On Reset

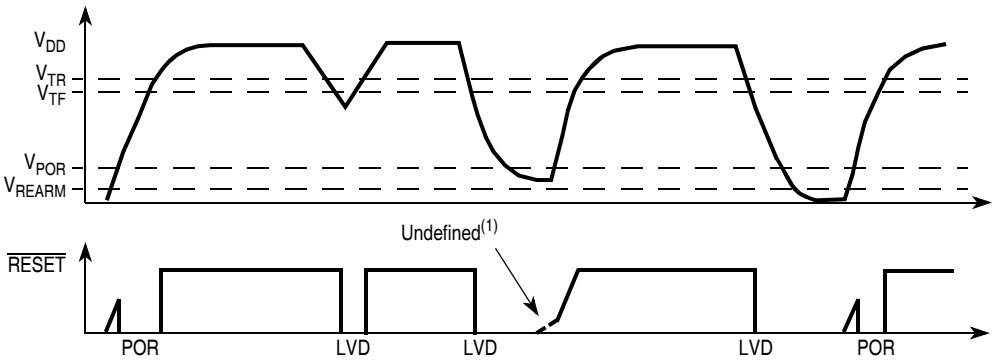
The internal Power On Reset (POR) module generates a reset when V_{DD} rises to typically 1.4 V. The POR rearm voltage is below this value before the module is ready to generate a POR again as V_{DD} falls and rises. If the application circuit does not discharge V_{DD} typically 0.9 V in a power-down sequence, POR may not be generated on the next power up. In this case, internal logic states are not initialized to guaranteed levels and may cause a malfunction. To guarantee circuit initialization, the POR pulse depends on the V_{DD} voltage level plus a number of clock cycles.

For a comprehensive explanation of POR and resets in general consult application note *Resetting MC9RS08KA During Power Transitions* (Freescale document order number AN3394).

4 Low Voltage Detect

The low-voltage detect (LVD) module sets a flag bit, triggers an interrupt, or generates a reset if properly programmed at the system power management status and control 1 (SPMSC1) register when V_{DD} falls below trip falling level. The reset signal is deactivated when V_{DD} rises above the trip rising level (falling threshold level + hysteresis). LVD module enable, LVD stop mode enable, and LVD reset generation are selected by default upon reset.

Figure 2 illustrates reset generation for both POR and LVD situations. V_{DD} is not plotted on a linear scale. The difference between POR and LVD voltages are exaggerated for illustrative purpose. V_{POR} is power on reset voltage, V_{REARM} is POR rearm voltage, V_{TF} is LVD trip falling voltage, and V_{TR} is LVD trip rising voltage.



1. Undefined state when POR is not rearmed

Figure 2. Supply Voltage Variation and Reset Generation

Due to characteristics mentioned at the initialization sequence, application software has to take care of:

- Shared pin functionality selection
- LVD configuration

Different microcontroller families available in the market present other characteristics and limitations that should be considered when designing application circuits.

For more detailed information on these topics and electrical specifications, refer to the *MC9RS08KA2 Data Sheet*.

5 Application Hints

Good design practices must be used when developing application circuits, some of which are briefly described here. A detailed description of these techniques and hints may be found in other noise reduction, EMC, and PCB design bibliography.

5.1 Supply Circuit

- Analyze current consumption, power-up and power-down sequences
- Determine noise filtering and add appropriate transient suppressor and decoupling capacitors
- Many voltage regulators require a ceramic capacitor near input pins as well as a low equivalent series resistance (ESR) capacitors plus decoupling capacitors on output pins
- Electrolytic or tantalum capacitors, with adequate capacitance to provide charge during supply voltage drops, and ceramic capacitors should be placed close to regulator output pins
- In specifically noisy environments, such as an automotive battery network, zener diodes or varistors and series resistors may be required to filter extreme, high-energy, high-voltage transients
- Supply derived from AC mains should be of the preferred resistive type (a low-pass filter) instead of the capacitive type, which is a high-pass filter and allows line transients to reach the V_{DD} network.

5.2 Noise Filtering and Decoupling

- Small capacitors with high resonant frequency, or even RC filters, may be added to critical signal pins (such as $\overline{\text{RESET}}$ and Comparator inputs)
- Good decoupling for internal and external noise, generally combining 0.1 µF and 0.01 µF ceramic or multilayer capacitors, are used as close as possible to V_{DD} and V_{SS} pins of the MCUs
- Pins, leads, and track inductance may degrade decoupling efficiency

For additional information, refer to Figure 3, Table 1, and the application note titled *Designing for Board Level Electromagnetic Compatibility* (Freescale document order number AN2321).

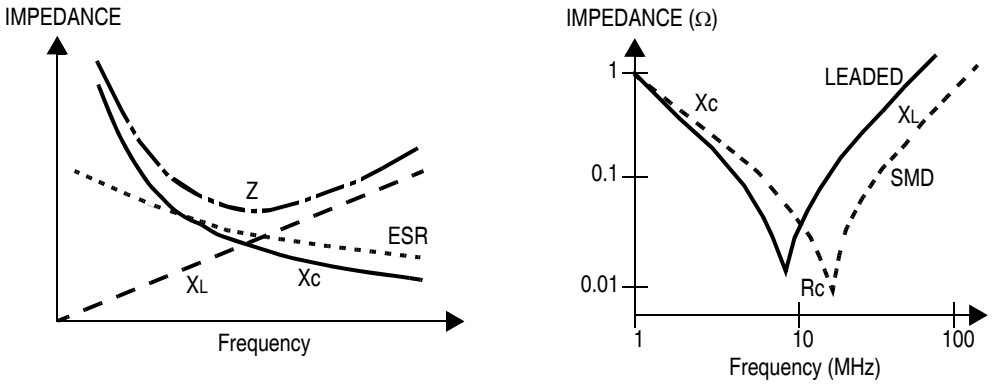


Figure 3. Typical Capacitor Parameters with Frequency

Table 1. Typical Electronic Device Characteristics

	Capacitance	Inductance	ESR	Self-Resonant Frequency
Leaded devices	4 pF per pin	1 nH/mm	—	—
Leadless devices	0.3 pF per pin	0.5 nH	—	—
Ceramic Z5U through-hole capacitor	For example, 0.1 μF	3.5 nH	—	8 MHz
Multilayer NPO through-hole capacitor	For example, 1 nF	3 nH	—	80 MHz
Ceramic Z5U SMD capacitor	For example, 0.1 μF	1 nH	—	16 MHz
Multilayer NPO SMD capacitor	For example, 1nF	0.5 nH	—	160 MHz
Aluminum electrolytic capacitor	For example, 10 μF	—	20 Ω	—
Aluminum electrolytic capacitor	For example, 1000 μF	—	0.5 Ω	—
Tantalum capacitor	For example, 10 μF	—	3 Ω	—
Tantalum capacitor	For example, 100 μF	—	0.8 Ω	—

5.3 Line Termination and Pullup/Pulldown Resistors

- Line termination and pullup/pulldown resistors may be required to guarantee voltage levels at high impedance or unused pins (do not tie directly to V_{DD}/V_{SS})
- Floating input pins may store intermediate voltage levels that would cause current drain on internal logic gates
- Floating pins are also prone to pick up noise and suffer electrostatic discharge stress (ESD)

For MCUs, the $\overline{\text{RESET}}$ pins should have decoupling capacitors to V_{DD} close to the MCU pins. If possible, pullup resistors and short connections should be far from high-noise circuitry.

5.4 POR and LVD Modules

- Internal POR circuits and LVD modules are efficient ways to protect MCUs from V_{DD} voltage drops (brown-out) and power-up/power-down events.
- To check for proper operation with the power supply (within operating ranges), threshold levels and response times can be obtained from the MCU electrical specifications.
- POR requires a number of clock cycles to release internal reset signals.

5.5 Protection Devices

Protection devices should be added to cancel spikes and to clamp voltages, such as:

- Free-wheel diodes on relay coils and inductors
- Clamp diodes to V_{DD} or V_{SS} on critical pins subject to high energy noise,
- Reverse diodes on power switches to avoid arcs
- Zener diodes to limit voltage excursion at some critical circuit points

5.6 Printed Circuit Board

Printed circuit boards should be designed following good common practices, such as:

- Maximizing ground plan or ground mesh (small ground loops to avoid high frequency induced currents)
- Single-point ground connection for low-frequency signals
- Multi-point ground connection for high-frequency signals
- Signal layers inside V_{DD} and V_{SS} planes on multilayer PCBs
- Separate analog and digital power lines
- Large V_{DD} and V_{SS} tracks
- Narrow signal tracks to minimize inductance
- Short tracks on critical signals such as clocks, oscillators, and $\overline{\text{RESET}}$
- Ground shielding parallel to critical lines and around critical circuit areas (oscillators, analog circuitry, power circuitry, relays, etc.)
- Shielding around whole PCB

For more detailed information, refer to the application note titled *Designing for Electromagnetic Compatibility (EMC) with HCMOS Microcontrollers* (Freescale document order number AN1050).

5.7 Noise Reduction Checklist

To control the use of the most important techniques and to be sure that the design was thoroughly reviewed, use a noise reduction checklist. For more detailed information, refer to the application titled *System Design and Layout Techniques for Noise Reduction in MCU-Based Systems* (AN1259).

5.8 Software Coding Practices

Incorporate software coding practices, such as:

- Sanity checking routines or token pass routines on main flow
- Port or flag polling to control execution flow
- Filling empty memory with NOPs and JUMPs to allow recovery from wrong addressing

All of these may help to avoid code runaway or being lost on a bad loop, making the application more robust.

5.9 Typical MC9RS08KA Application Circuit

The circuit shown in Figure 4 is an application example of a microcontroller system in a high-voltage environment such as an appliance controller at the AC line.

The MC9RS08KA MCU is used to:

- Read a switch and one analog input
- Control a light-emitting diode (LED) and a relay through a bipolar driver

Such a circuit presents good noise immunity and is the basis for reliable microcontroller system operation.

Some of the points recommended in this application note have been implemented in the circuit shown in Figure 4. They are:

- Series resistor and zener diode at +DC for high voltage protection
- Ceramic decoupling capacitors close to regulator in and out pins
- Low ESR tantalum capacitor at regulator output
- Decoupling capacitor (multi-layer suggested) close to MCU V_{DD}/V_{SS} pins
- Pullup resistor (internal or external) and noise filtering capacitor (multi-layer suggested) at $\overline{\text{RESET}}$ pin, which deserves special attention at PCB layout (far from noise sources)
- PTA2/$\overline{\text{RESET}}$ pin used for on-board jumper reading, not for external signal
- CN1 is the system connector, which may have long and noisy lines
- Optional background header may be used for in-circuit programming of MCU flash
- RC low-pass filter at analog sensor input (ACMP-) for noise filtering
- Noise filtering capacitor at KBIP0 pin, with internal pullup resistor enabled
- Relay with protection diodes and noise filtering capacitor at load line.

NOTE

To filter incoming noise and high-voltage pulses, ideally 1 nF decoupling capacitors should be added at the system connector pins in noisy high-voltage applications.

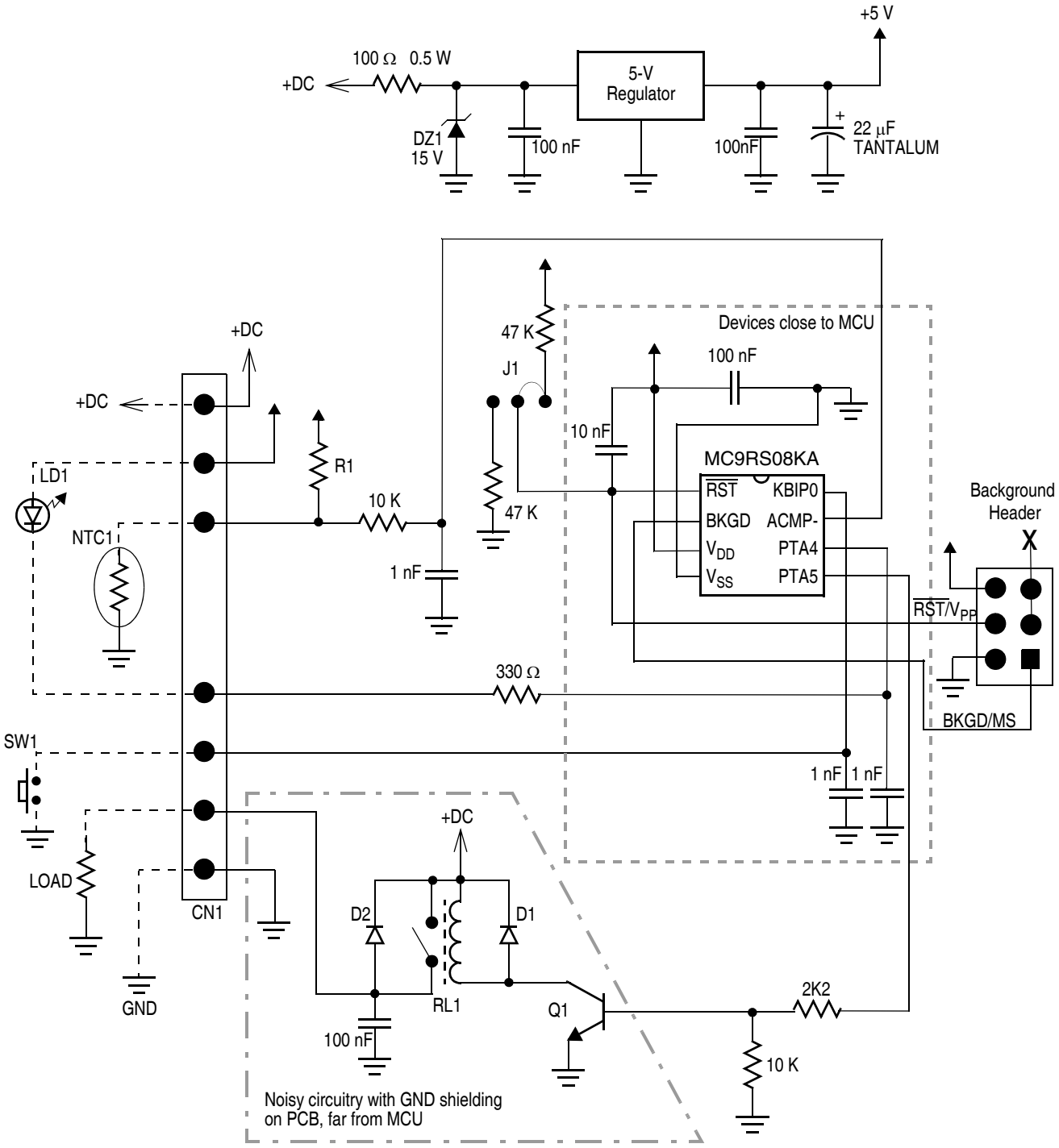


Figure 4. Typical Application Circuit Using the MC9RS08KA MCU

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