Freescale Semiconductor
Application Note

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Design Checklist for PowerQUICC™ II Pro MPC8315E Processor

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This application note describes the generally recommended connections for new designs based on the Freescale MPC8315E and MPC8315 processors. The design checklist may also apply to future bus or footprint-compatible processors. It can also serve as a useful guide to debugging a newly-designed system, by highlighting those areas of a design that merit special attention during initial system startup.

Contents

1 MPC8315/MPC8315E Background

This section outlines recommendations to simplify the first phase of design. Before designing a system with a PowerQUICC™ II Pro device, the designer should be familiar with the available documentation, software, models, and tools.

1.1 References

Some references listed here may be available only under a nondisclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

- Collateral
  - — *MPC8315E PowerQUICC™ II Pro Integrated Host Processor Family Reference Manual* (MPC8315ERM)
  - — *MPC8315E PowerQUICC™ II Pro Integrated Host Processor Family Chip Errata* (MPC8315ECE)
  - — *MPC8315E PowerQUICC™ II Pro Integrated Host Processor Hardware Specifications* (MPC8315EEC)
- Tools
  - — UPM programming tool
- Models
  - — IBIS
  - — BSDL, Rev. 1.0, Rev. 1.1 and Rev. 1.2 silicon

1.2 Device Errata

The device errata document (MPC8315ECE) describes the latest fixes and work arounds for the PowerQUICC II Pro family of devices. Carefully study these documents before starting a design with the respective PowerQUICC II Pro device.

1.3 UPM Programming Tool

The UPM programming tool GUI is a user-friendly interface for programming all three PowerQUICC II Pro UPM machines. The GUI consists of a wave editor, table editor, and report generator. The user can directly edit the waveform or RAM array. Then the report generator prints out the UPM RAM array for use in a C program. The UPM programming tool can be found on the MPC8315E product page at the web site listed on the back cover of this document.

1.4 Product Revisions

Table 1. PowerQUICC II Pro (MPC8315) Product Revisions

Device	Package	SVR (Rev. 1.0)	SVR (Rev. 1.1)	SVR (Rev. 1.2)
MPC8315E	TEPBGA-II	80B4_0010	80B4_0011	80B4_0012
MPC8315	TEPBGA-II	80B5_0010	80B5_0011	80B5_0012
MPC8314E	TEPBGA-II	80B6_0010	80B6_0011	80B6_0012
MPC8314	TEPBGA-II	80B7_0010	80B7_0011	80B7_0012

Note: PVR = 8085_0020 for all devices and revisions in this table.

2 Power

This section provides design considerations for the PowerQUICC II Pro power supplies, as well as power sequencing. For information on PowerQUICC II Pro AC and DC electrical specifications and thermal characteristics, refer to MPC8315EEC. For power sequencing recommendations, see Section 2.2, "Power Consumption."

2.1 Power Supply

The PowerQUICC II Pro has a core voltage, V_{DD}, that operates at a lower voltage than the I/O voltages GV_{DD}, LV_{DD}, and NV_{DD}. The V_{DD} should be supplied through a variable switching supply or regulator to allow for compatibility with core voltage changes on future silicon revisions. The core voltage, 1.0 V (±5%), is supplied across V_{DD} and GND.

The MPC8315EEC lists the recommended range for each power supply listed in Table 2. These voltages are typically supplied by simple linear regulators, which increases the complexity of the system because multiple voltage supplies and PCB power planes are required for the design. No external signals on the MPC8315E are 5-V-tolerant. Note that absolute maximum ratings are stress ratings only. The functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or permanently damage the device.

2.2 Power Consumption

The MPC8315E hardware specification document provides the power dissipation of V_{DD} for various configurations of the coherent system bus (CSB) and the e300 core frequencies. The hardware specification also estimates power dissipation for all the I/O power rails. I/O power highly depends on the application and is an estimate. A full analysis of your board implementation is required to define your I/O power supply needs. The typical V_{DD} power plus I/O power should be used for the thermal solution design. The junction temperature must not exceed the maximum specified value. The maximum V_{DD} power is the worst case power consumption and should be used for the core power supply design.

2.3 Power Sequencing

One consequence of multiple power supplies is that when power is initially applied, the voltage rails ramp up at different rates. These rates depend on the power supply, the type of load on each power supply, and the manner in which different voltages are derived. However, advances in the PowerQUICC II Pro ESD design allow flexibility in the order in which power rails ramp up, as long as the supplies do not exceed absolute maximum ratings (as defined in the device-specific hardware specifications).

NOTE

From a system standpoint, if the I/O power supplies ramp up before the V_{DD} core supply stabilizes there may be a period of time when the I/O pins are driven to a logic one or logic zero state. After the power is stable, as long as $\overline{\text{PORESET}}$ is asserted, most IP pins are three-stated. To minimize the time that I/O pins are actively driven, apply core voltage before I/O voltage and assert $\overline{\text{PORESET}}$ before the power supplies fully ramp up.

Table 2 shows the current maximum ratings for the power supplies. Supplies must not exceed these absolute maximum ratings. However, during normal operation, use of the recommended operating conditions tables in the hardware specifications is recommended. Any information in the relevant hardware specifications supersedes information in Table 2.

Figure 1 shows a power sequencing example.

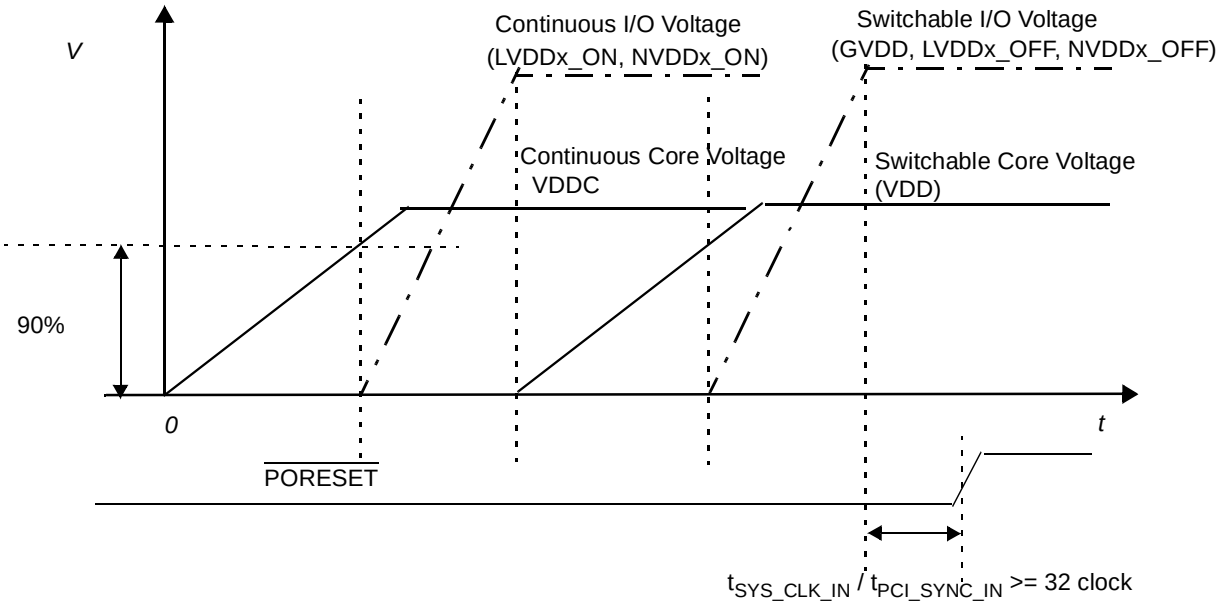


Figure 1. Power Sequencing Example with Low power D3 Warm Mode

2.4 Power sequencing during Power Management

During power down modes, where switchable 1 V supply (VDD, AVDD1, SDAVDD, USB_PWR_PLL1, XCOREVDD, XPADVDD, SATA_VDD, VDD1IO, and VDD1ANA) and the switchable I/Os (GVDD, MVREF, USB_PWR_PLL3, USB_VDDA, USB_VDDA_BIAS, LVDD1_OFF, NVDD*_OFF, VDD33PLL, and VDD33ANA) are switched off, the sequencing has to be maintained.

While entering D3 warm state, switchable I/Os has to be switched off first, and it is followed by switchable 1 V supply. While exiting from D3 warm state, switchable 1 V supply has to come up, and it is followed by the switchable I/O supply.

2.5 Power Planes

Each V_{DD} pin should be provided with a low-impedance path to the board power supply. Similarly, each ground pin should be provided with a low-impedance path to ground. The power supply pins drive distinct groups of logic on-chip. The capacitor leads and associated printed-circuit traces connecting to chip V_{DD} and ground should be kept to less than half an inch per capacitor lead.

2.6 Decoupling

Due to large address and data buses and high operating frequencies, the PowerQUICC II Pro can generate transient power surges and high-frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PowerQUICC II Pro system, and it requires a clean, tightly regulated source of power. Therefore, the system designer should place at least one decoupling capacitor at each V_{DD}, GV_{DD}, LV_{DD}, $LV_{DD1\_OFF,}$ LV_{DD2_ON} and NV_{DD} pin. These decoupling capacitors should receive their power from separate V_{DD}, GV_{DD}, LV_{DD}, $LV_{DD1\_OFF,}$ $LV_{DD2\_ON,}$ NV_{DD}, and GND power planes in the PCB, using short traces to minimize inductance. Capacitors can be placed directly under the device using a standard escape pattern. Other capacitors can surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic surface mount technology (SMT) capacitors should be used to minimize lead inductance.

In addition, several bulk storage capacitors should be distributed around the PCB, feeding the V_{DD}, GV_{DD}, LV_{DD}, $LV_{DD1\_OFF,}$ LV_{DD2_ON} and NV_{DD} planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low equivalent series resistance (ESR) rating to ensure quick response time. They should also connect to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors: 100–300 µF.

Use simulation to minimize noise on the power supplies before proceeding into the PCB design and manufacturing stage of development.

2.7 Core PLL Power Supply Filtering

Each PowerQUICC II Pro PLL is provided power through independent power supply pins (AVDD1, AVDD2, respectively). The AV_{DD} level should always be equivalent to V_{DD}, and preferably these voltages are derived directly from V_{DD} through a low frequency filter scheme.

There are a number of ways to reliably provide power to the PLLs, but the recommended solution is to provide independent filter circuits as illustrated in Figure 2, one to each of the AVDD pins, thus reducing noise injection from one PLL to the other. This circuit filters noise in the PLL resonant frequency range from 500 kHz to 10 MHz. It should be built with surface mount capacitors with a minimum effective series inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended instead of a single large value capacitor.

Place each circuit as closely as possible to the specific AVDD pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the package, without the inductance of vias.

Figure 2 shows the PLL power supply filter circuit for CORE PLL(AV_{DD1}) and SYSTEM PLL(AV_{DD2}).

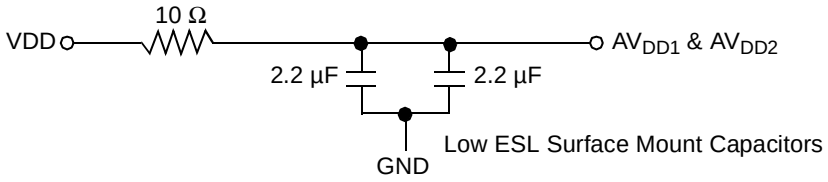


Figure 2. PLL Power Supply Filter Circuit

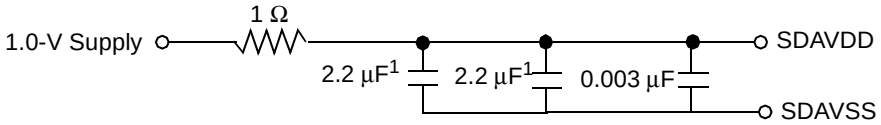
2.8 SerDes PLL Power Supply Filtering

The power supplied to the SerDes PLL must be filtered to ensure a stable internal clock. It must also use a proper decoupling scheme to ensure a clean and tightly regulated source of power.

The SDAVDD signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit like the one shown in Figure 3.

For maximum effectiveness the following SerDes PLL power supply filtering recommendations should be followed:

- Place the filter circuit as closely as possible to the $SDAV_{DD}$ ball to ensure it filters out as much noise as possible.
- Ensure that the ground connection is near the $SDAV_{DD}$ ball.
- Place the 0.003 µF capacitor closest to the $SDAV_{DD}$ ball, followed by the 2.2 µF capacitor, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from $SDAV_{DD}$ to the ground plane.
- Use ceramic chip capacitors with the highest possible self-resonant frequency.
- Keep all traces short, wide, and direct.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 3. SerDes PLL Power Supply Filter Circuit

2.9 SerDes Power Supply Decoupling Recommendations

The SerDes block requires a clean, tightly regulated source of power (XCOREVDD and XPADVDD) to ensure low jitter on transmit and reliable recovery of data in the receiver. An appropriate decoupling scheme is outlined below.

- Only surface mount technology (SMT) capacitors should be used to minimize inductance.
- Connections from all capacitors to power and ground should be done with multiple vias to further reduce inductance.
- The board should have at least 10 × 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device. Where the board has blind vias, these capacitors should be placed directly below the chip supply and ground connections. Where the board does not have blind vias,

these capacitors should be placed in a ring around the device as close to the supply and ground connections as possible.

- There should be a 1-µF ceramic chip capacitor from each SerDes supply (XCOREVDD and XPADVDD) to the board ground plane on each side of the device. This should be done for all SerDes supplies.
- Between the device and any SerDes voltage regulator there should be a 10-µF, low equivalent series resistance (ESR) SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

2.10 SATA Power Supply Filtering

The analog 1.0-V and analog 3.3-V supplies (VDD1ANA, VDD33PLL and VDD33ANA respectively) are used in the SATA PLL and Bias Blocks. These share a common analog ground (VSS1ANA).

It is strongly recommended that the digital power for SATA be kept separate from any other digital logic supply. Add filters on digital and analog supplies for SATA block as shown below.

Figure 4 shows the PLL power supply filter circuit for SATA PLL (VDD33PLL).

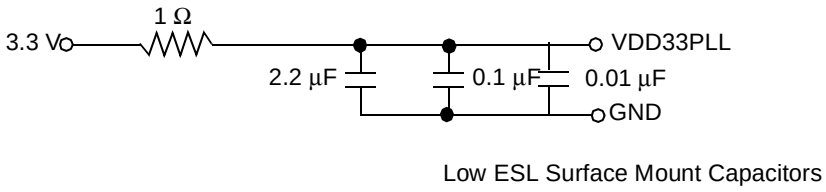


Figure 4. SATA PLL Power Supply Filter Circuit

Figure 5 shows the Analog power supply filter circuit for SATA (VDD33ANA).

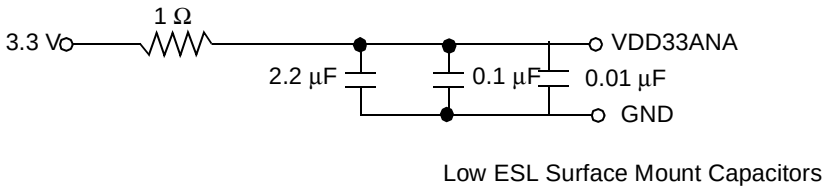


Figure 5. SATA Analog Power Supply Filter Circuit

Figure 6 shows the 1-V power supply filter circuit for SATA_VDD, VDD1IO and VDD1ANA.

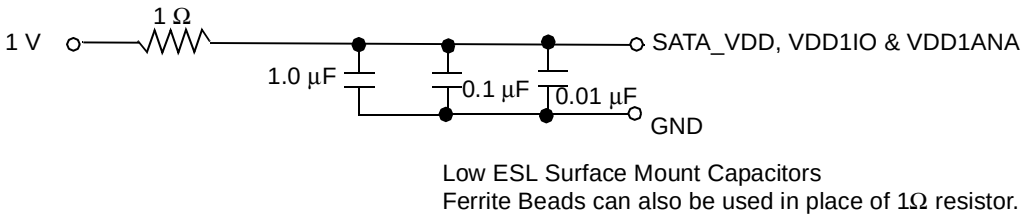


Figure 6. SATA Power Supply Filter Circuit

3 Pin Listing and Connections

Table 2 summarizes the power signal pins.

Table 2. Power Signal Pin Listing

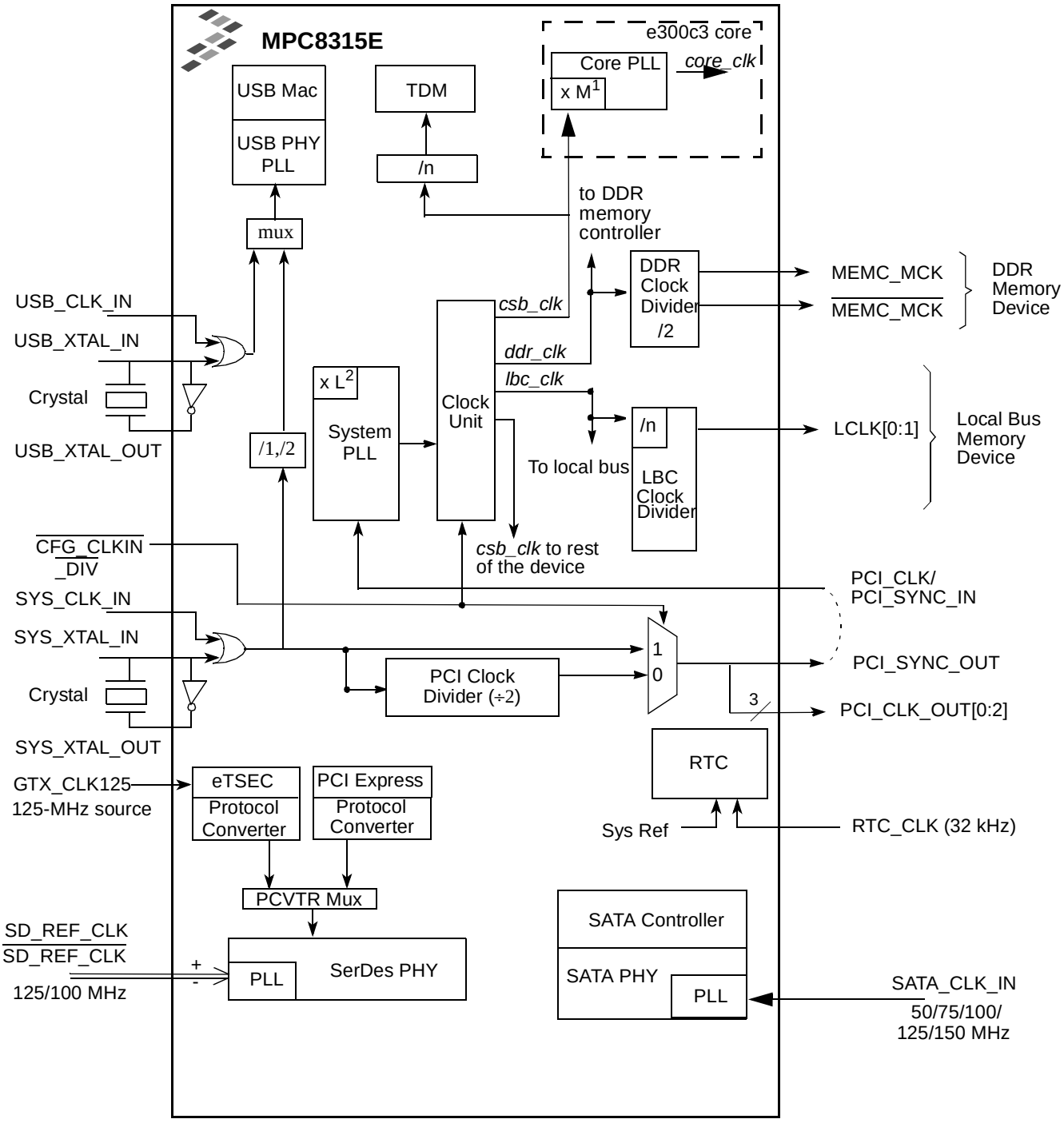
Signal	Pin Type	MPC8315E	MPC8315	Connection	Notes
AV_{DD1}	—	X	X	1.0 V ± 50 mV	Analog power for e300 core PLL (switchable)
AV_{DD2}	—	X	X	1.0 V ± 50 mV	Analog power for system PLL (always on)
SDAVDD	—	X	X	1.0 V ± 50 mV	SerDes analog power for PLL (switchable)
USB_PLL_PWR1	—	X	X	1.0 V ± 50 mV	Analog power for USB PLL (switchable)
USB_PLL_PWR3	—	X	X	3.3 V ± 165mV	Analog power for USB PLL (switchable)
USB_VDDA	—	X	X	3.3 V ± 300 mV	USB transceiver power (switchable)
USB_VDDA_BIAS	—	X	X	3.3 V ± 300 mV	USB BIAS circuit power (switchable)
GV_{DD}	—	X	X	2.5 V ± 200mV 1.8 V ± 100 mV	DDR and DDR2 I/O voltage (switchable)
MVREF	—	X	X	0.49xGV_{DD} to 0.51 xGV_{DD}	DDR reference voltage (switchable)
LVDD1_OFF	—	X	X	2.5 V ± 125 mV or 3.3 V ± 300 mV	eTSEC1/USBDR I/O supply (switchable)
LVDD2_ON	—	X	X	2.5 V ± 125 mV or 3.3 V ± 300 mV	eTSEC2 (always on)
VDDC	—	X	X	1.0 V ± 50 mV	Core supply voltage (always on)
VDD	—	X	X	1.0 V ± 50 mV	Core supply voltage (switchable)
NVDD1_ON	—	X	X	3.3 V ± 300 mV	Standard I/O voltage (always on)
NVDD1_OFF	—	X	X	3.3 V ± 300 mV	Standard I/O voltage (switchable)
NVDD2_ON	—	X	X	3.3 V ± 300 mV	Standard I/O voltage (always on)
NVDD2_OFF	—	X	X	3.3 V ± 300 mV	Standard I/O voltage (switchable)
NVDD3_OFF	—	X	X	3.3 V ± 300 mV	Standard I/O voltage (switchable)
NVDD4_OFF	—	X	X	3.3 V ± 300 mV	Standard I/O voltage (switchable)
XCOREVDD	—	X	X	1.0 V ± 50 mV	SerDes internal digital power (switchable)
XPADVDD	—	X	X	1.0 V ± 50 mV	SerDes I/O digital power (switchable)
SATA_VDD	—	X	X	1.0 V ± 50 mV	SATA digital power (switchable)
VDD1IO	—	X	X	1.0 V ± 50 mV	SATA analog I/O power (switchable)
VDD1ANA	—	X	X	1.0 V ± 50 mV	SATA core analog power (switchable)
VDD33PLL	—	X	X	3.3 V ± 165 mV	SATA PLL power (switchable)
VDD33ANA	—	X	X	3.3 V ± 165 mV	SATA analog power (switchable)

NOTE

- LV_{DD1_OFF} and LV_{DD2_ON} can be powered from different I/O voltage supplies.
- For MII and RMII operations LV_{DD1_OFF} and LV_{DD2_ON} should be tied to 3.3 V.
- For RGMII and RTBI operations LV_{DD1_OFF} and LV_{DD2_ON} can be at 2.5 V or 3.3V.
- FOR DDR1, GV_{DD} should be tied to 2.5 V.
- FOR DDR2, GV_{DD} should be tied to 1.8 V.
- Core power V_{DD} can be switched off during power-down mode.
- All the power pins need to be tied to their corresponding voltages irrespective of the fact that a module is used or not in the system. For example, even if USB interface is not used in the system, the USB power pins (USB_PLL_PWR1, USB_PLL_PWR3, USB_VDDA, and USB_VDDA_BIAS) need to be tied to their corresponding voltages.
- All the I/Os should be interfaced with peripherals operating at same voltage levels.

4 Clocking

Figure 7 shows the internal distribution of clocks within the MPC8315E.



1 Multiplication factor M = 1, 1.5, 2, 2.5, and 3. Value is decided by RCWLR[COREPLL].

2 Multiplication factor L = 2, 3, 4 and 5. Value is decided by RCWLR[SPMF].

Figure 7. Clock Subsystem Block Diagram

The primary clock source for the MPC8315E is one of two inputs, CLKIN or PCI_CLK, depending on whether the device is configured as a PCI host or PCI agent. Table 3 lists the clock signal pins.

Table 3. Clock Signal Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
PCI_CLK_OUT[0:2]	O	As needed	Open	• **Device as PCI host:** Functions as PCI output clock banks. OCCR register determines whether clocks are set as CLKIN or CLKIN÷2. • **Device as PCI agent:** These signals are not used.
PCI_SYNC_IN/ PCI_CLK	I	Connect to PCI_SYNC_OUT or 25–66 MHz clock signals	**Not applicable.** This pin should always be connected	• **Device as PCI host:** Functions as PCI_SYNC_IN. Connect externally to PCI_SYNC_OUT. • **Device as PCI agent:** Functions as PCI_CLK. A valid 25–66.67 MHz clock signal (at NV_{DD} level) must be applied to this signal.
PCI_SYNC_OUT	O	Connect to PCI_SYNC_IN	Open	• **Device as PCI host:** Connect externally to PCI_SYNC_IN signal for de-skewing of external PCI clock routing. Loop trace should match with PCI_CLK_OUTx signal traces. • **Device as PCI agent:** This signal is not used.
SYS_CLK_IN / SYS_XTAL_IN and SYS_XTAL_OUT	I I O	Connect to 25–66.67 MHz clock signal (Recommended: 33/66MHz)	1 k–4.7 kΩ to GND.	Clock input when configured in PCI host mode. A valid 25–66.67 MHz clock signal (at NV_{DD} level) must be applied to this input when used. When an oscillator is used to feed SYS_CLK_IN, tie the SYS_XTAL_IN pin to GND and leave SYS_XTAL_OUT unconnected. When Crystal is connected across SYS_XTAL_IN and SYS_XTAL_OUT, tie SYS_CLK_IN to GND.
USB_CLK_IN / USB_XTAL_IN and USB_XTAL_OUT	I I O	Connect to 24 or 48 MHz clock signal	1 k–4.7 kΩ to GND.	A valid 24/48 MHz clock signal (at NV_{DD} level) must be applied to this input when used. When an oscillator is connected to USB_CLK_IN, tie the USB_XTAL_IN pin to GND and leave USB_XTAL_OUT unconnected. When Crystal is connected across USB_XTAL_IN and USB_XTAL_OUT, tie USB_CLK_IN to GND.
GTX_CLK125	I	Connect to 125 MHz clock signal	1 k–4.7 kΩ to GND.	A valid 125 MHz clock signal must be applied to this signal. This must be externally generated with an oscillator or is sometimes provided by the PHY.
SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ (SGMII/PCI Express PHY CLOCK)	I	Connect to a 125 MHZ single-ended or differential clock for SGMII or connect to a 100 MHz differential clock for PCI Express	Tie both the pins to GND	A Valid 125/100 MHz clock signal must be applied to this input when used. The reference is 1 V and not 3.3 V. When a single-ended clock is used, feed the clock to the SD_REF_CLK pin and leave $\overline{\text{SD\_REF\_CLK}}$ unconnected.

Table 3. Clock Signal Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
SATA_CLKIN	I	Connect to a 75 MHz clock signal 75/100/125/150 MHz. Recommended: 75 MHz	1 k–4.7 kΩ to GND.	A valid 75 MHz clock signal must be applied to this input when it is used.
USBDR_CLK	I	For ULPI, connect 60 MHz clock from the ULPI Phy.	1 k–4.7 kΩ to GND	A valid 60 MHz clock signal must be applied to this input when it is used.
RTC_CLK	I	Tie to 32.768 kHz crystal	1 k–4.7 kΩ to GND	Real-time clock/periodic interval timer input from external 32.768 kHz crystal

4.1 System Clock in PCI Host Mode

When the MPC8315E is configured as a PCI host device (RCWH[PCIHOST] = 1), CLKIN is its primary input clock. CLKIN feeds the PCI clock divider (÷2) and the PCI_SYNC_OUT and PCI_CLK_OUT multiplexers. PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal PCI controller clock to synchronize with the external PCI agent clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system.

PCI_CLK_OUT[0:2] output buffers are enabled by RCWH[PCICKDRV]. The individual PCI_CLK_OUT[0:2] can be disabled by clearing the OCCR[PCICOEn] bit. For example, if only one PCI clock is needed, then set RCWH[PCICKDRV] and configure OCCR[0:2] = 3’b100.

$\overline{\text{CFG\_CLKIN\_DIV}}$ selects whether CLKIN or CLKIN÷2 is driven out on the PCI_SYNC_OUT and PCI_CLK_OUT[0:2] signals. If $\overline{\text{CFG\_CLKIN\_DIV}}$ = 0, then the PCI interface runs at half the CLKIN speed.

4.2 System Clock in PCI Agent Mode

When the MPC8315E is configured as a PCI agent device, PCI_CLK is the primary input clock. In agent mode, the CLKIN signal can be tied to GND. PCI_CLK_OUT*n* and PCI_SYNC_OUT are not used. When the device is configured as a PCI agent mode, the $\overline{\text{CFG\_CLKIN\_DIV}}$ configurations input can be used to double the internal clock frequencies, if sampled as ‘0’ during power-on reset assertion. This feature is useful if a fixed internal frequency is desired regardless of whether the PCI clock is running at 33 or 66 MHz. PCI specification requires the PCI clock frequency information to be provided by the M66EN signal.

NOTE

M66EN is an input pin in the PCI interface that determines the frequency of PCI bus operation.

4.3 System Clock if PCI is Disabled

If the PCI interface is not used, PCI_CLK is the primary input clock. CLKIN and CFG_CLKIN_DIV can be tied to GND in case the CLK is fed directly from PCI_CLK. However CLK can still be fed through the CLKIN pin and PCI_SYNC_OUT and PCI_CLK need to be shorted. CFG_CLKIN_DIV will have no effect on the output of CLK unit.

4.4 USB Clocking

When the on-chip USB PHY is used, the reference input can be provided externally through a separate clock source, either a crystal or an external oscillator. The PHY supplies the clock to the USB DR controller in UTMI mode. The PHY clock domain and the CSB clock domain are synchronized in the USB controller. An option is provided to supply the USB reference clock from the SYS_CLK_IN or SYS_XTAL_IN inputs. Therefore, a single crystal or clock input can supply both system and USB references. The USB reference clock can be provided with a divide by 1 or 2 from these inputs. When using the single clock or crystal option, the frequency for the SYS_CLK_IN or SYS_XTAL_IN must be chosen such that the USB reference is 24 or 48 MHz for the divide by 1 or 2 option. That is, the SYS_CLK_IN must be 24 or 48 MHz.

If this option is used in PCI agent mode, the PCI clock supplied to device must still be chosen at the appropriate frequencies. The PCI source clock would be tied to both SYS_CLK_IN and PCI_CLK inputs. The clock source must meet the input clock specifications for both SYS_CLK_IN and USB_CLK_IN.

4.5 PCI Express or Ethernet Clocking

The MPC8315 processor contains an integrated Serdes PHY that can be programmed to act as either a PCI Express lane or SGMII interface. This PHY has its own PLL and requires a 125 MHz or 100 MHz differential clock reference input. SGMII requires 125 MHz, and PCI Express requires a 100 MHz clock. The reference is 1 V and not 3.3 V. The PHY generates its own transmit and receive sampling clock. The receive clock is recreated from the receive data. The PHY supplies the transmit/receive clock between the PHY and the MAC (PCI Express controller/eTSEC controller). Synchronization between the MAC and the CSB clock domain occurs in the MAC. For proper synchronization, the CSB must be running at a higher frequency than the transmit/receive clock. When running in RGMII or RTBI modes (not using the SerDes) the reference clock is supplied by the GTX_CLK125 input on the eTSEC interface. This clock input is 125 MHz. Set the bit 27 in SICRH register when the GTX_CLK125 input is 2.5 V.

NOTE

This signal lies in the 3.3 V I/O bank of MPC8315 and if GTX_CLK125 input is 2.5 V, bit 27 in SICRH register needs to be set.

4.6 SATA Clocking

SATA PHYs are integrated in the MPC8315 processor. They require a 75 MHz/100 MHz/125 MHz/150 MHz clock reference input.

5 Power-On Reset and Reset Configurations

A detailed power-on reset flow is as follows:

1. Power to the device is applied.
2. The system asserts $\overline{\text{PORESET}}$ (and optionally $\overline{\text{HRESET}}$) and $\overline{\text{TRST}}$ initializing all registers to their default states.
3. The system applies a stable CLKIN (PCI host mode) or PCI_CLK (PCI agent mode) signal and stable reset configuration inputs (CFG_RESET_SOURCE, CFG_CLKIN_DIV).
4. The system negates $\overline{\text{PORESET}}$ after at least 32 stable CLKIN or PCI_CLK clock cycles.
5. The device samples the reset configuration input signals to determine the clock division and the reset configuration words source.
6. The device starts loading the reset configuration words. When the reset configuration word low is loaded, the system PLL begins to lock. When the system PLL is locked, the *csb_clk* is supplied to the e300 PLL.
7. The e300 PLL begins to lock.
8. The device drives $\overline{\text{HRESET}}$ asserted until the e300 PLL is locked and until the reset configuration words are loaded.
9. If enabled, the boot sequencer loads configuration data from the serial EEPROM as described in the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual.*

5.1 Reset Configuration Signals

Various device functions of the PowerQUICC II Pro are initialized by sampling certain signals during the assertion of the $\overline{\text{PORESET}}$ signal after a stable clock is supplied. These inputs are either pulled high or low. Although these pins are generally output pins during normal operation, they are treated as inputs while $\overline{\text{PORESET}}$ is asserted. See Table 4 for termination recommendations for the reset configuration pins.

Table 4. Reset Configuration Pin Listing

Signal	Pin Type	Termination
$\overline{\text{PORESET}}$	I	Driven actively by the external reset logic
$\overline{\text{HRESET}}$	I/O	Pullup with 1 kΩ to NV_{DD}
eTSEC2_TXD3/ CFG_RESET_SOURCE0	I/O	Pull up with 4.7 kΩ to LV_{DD2_ON} or pulldown with 1 kΩ to GND as desired, see Table 5 OR Driven as needed during $\overline{\text{HRESET}}$ assertion and tri-state after HRESET negation The length of the stubs introduced by connecting the resistors or any other active device should be kept minimum. Failing to do so may distort the TSEC2 transmit data signals.
eTSEC2_TXD2/ CFG_RESET_SOURCE1	I/O	
eTSEC2_TXD1/ CFG_RESET_SOURCE2	I/O	
eTSEC2_TXD0/ CFG_RESET_SOURCE3	I/O	
$\overline{\text{CFG\_CLKIN\_DIV}}$	I	Pull up with 4.7 kΩ to NV_{DD} or pull down with 1 kΩ to GND as desired
TSEC_MDC/LB_POR_CFG_ BOOT_ECC	I/O	Pull up with 1.5K kΩ to NV_{DD1_ON}; no pull down resistor required when logic 0 needs to be driven as the internal pull down is implemented in SOC OR Driven as needed during $\overline{\text{HRESET}}$ assertion and tri-state after HRESET negation.

For the TSEC_MDC/LB_POR_CFG_BOOT_ECC signal, Figure 8 shows the circuit to disable ECC checking during boot-up.

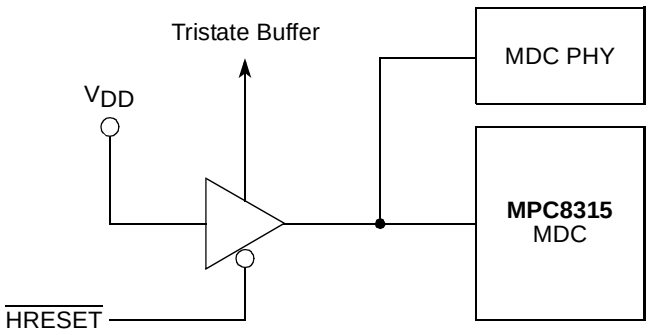


Figure 8. Recommended Circuit for Disabling ECC Checking during Boot-Up

The CFG_RESET_SOURCE[0:3] input signals are sampled during the assertion of $\overline{\text{PORESET}}$ to select the interface to load the reset configurations words:

- I^2C interface
- A device (that is, CPLD, EEPROM, or Flash) on the local bus
- From an internally-defined word value. See Table 5.

Table 5. Reset Configuration Word Source

Reset Configuration Signal Name	Value (Binary)	Meaning
CFG_RESET_SOURCE[0:3]	0000	NOR FLASH
	0001	NAND Flash 8 bit small page
	0010	Reserved
	0011	Reserved
	0100	I^2C EEPROM
	0101	NAND Flash 8 bit large page
	0110	Reserved
	0111	Reserved
	1000	Hard coded option 0
	1001	Hard coded option 1
	1010	Hard coded option 2
	1011	Hard coded option 3
	1100	Hard coded option 4
	1101	Reserved
	1110	Reserved
	1111	Reserved

The CFG_CLKIN_DIV input signal is also sampled during the assertion of $\overline{\text{PORESET}}$ to determine the relationship between CLKIN and PCI_SYNC_OUT. See Table 6.

Table 6. CLKIN Divisor Configuration

Reset Configuration Signal Name	Value (Binary)	Meaning
$\overline{\text{CFG\_CLKIN\_DIV}}$	1	In PCI host mode: • CLKIN:PCI_SYNC_OUT = 1:1 • *csb_clk* = (PCI_SYNC_IN *× SPMF) • All PCI_CLK_OUT clocks are limited to the CLKIN frequency. In PCI agent mode: • *csb_clk* = (PCI_CLK ×* SPMF)
	0	In PCI host mode: • CLKIN:PCI_SYNC_OUT = 2:1 • *csb_clk* = (PCI_SYNC_IN* × 2* × SPMF) In PCI agent mode: • *csb_clk* = (PCI_CLK * × 2 * ×SPMF)

5.2 Reset Configuration Words

The reset configuration words control the clock ratios and other basic device functions such as PCI host or agent mode, boot location, eTSEC modes, and endian mode. The reset configuration words are loaded from the local bus or from the I^2C interface during the power-on or hard reset flows. If the reset configuration word is from the flash memory, it should reside at the beginning of the flash memory. That is, it should start from address 0. A total of two 32-bit-words are read. The first byte is read from address

0x0, the second byte from address 0x8, the third byte from address 0x10, and so on until all 8 bytes are read. Bytes b0–b3 form a word, and this is the reset configuration word low register (RCWLR). Bytes b4–b7 form the reset configuration word high register (RCWHR). Refer to MPC8315 Reference Manual for more details:

- RCWLR
  0x0000: b0xxxxxx xxxxxxxx
  0x0008: b1xxxxxx xxxxxxxx
  0x0010: b2xxxxxx xxxxxxxx
  0x0018: b3xxxxxx xxxxxxxx
- RCWHR
  0x0020: b4xxxxxx xxxxxxxx
  0x0028: b5xxxxxx xxxxxxxx
  0x0030: b6xxxxxx xxxxxxxx
  0x0038: b7xxxxxx xxxxxxxx

If the reset configuration word is from an I^2C device, the I^2C setup must comply with the following requirements:

- EEPROM of extended address type must be used.
- EEPROM must respond to the calling address 0x101_0000.
- Use the special data format as described in the reference manual.

5.3 Useful System POR Debug Registers

The hardware reset configuration settings can be read in the reset configuration word low register (RCWLR), the reset configuration word high register (RCWHR), the reset status register (RSR), and the system PLL mode register (SPMR). See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual*. Note that all of these registers are read-only, except RSR.

5.4 Boot Sequencer

The boot sequencer provides the means to load the hardware reset configuration word and to configure any memory-mapped register before the boot-up code runs. Reset configuration load mode is selected based on the settings of the CFG_RESET_SOURCE pins during the power-on reset sequence. The I^2C interface loads the reset configuration words from an EEPROM at a specific calling address while the rest of the device is in the reset state. When the reset configuration words are latched inside the device, I^2C is reset until $\overline{\text{HRESET}}$ is negated. Then the device is initialized using boot sequencer mode.

Boot sequencer mode is selected at power-on reset by the BOOTSEQ field in the reset configuration word high register (RCWH). If the boot sequencer mode is selected, the I^2C module communicates with one or more EEPROM through the I^2C interface to initialize one or more configuration register of the PowerQUICC II Pro. For example, this code can be used to configure the port interface registers if the device is booting from the PCI. Refer to the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for the complete data format for programming the I^2C EEPROM.

The boot sequencer contains a basic level of error detection. If the I^2C boot sequencer fails while loading the reset configuration words are loaded, the RSR[BSF] bit is set. If a preamble or CRC fail is detected in boot sequencer mode, there is no internal or external indication that the boot sequencer operation failed Use one of the GPIO pins for that purpose.

5.5 $\overline{\text{HRESET}}$

The $\overline{\text{HRESET}}$ signal is not a pure input signal. It is an open-drain signals that the MPC8315E processor can drive low. The connection on the left side of Figure 9 causes signal contention and must not be used.

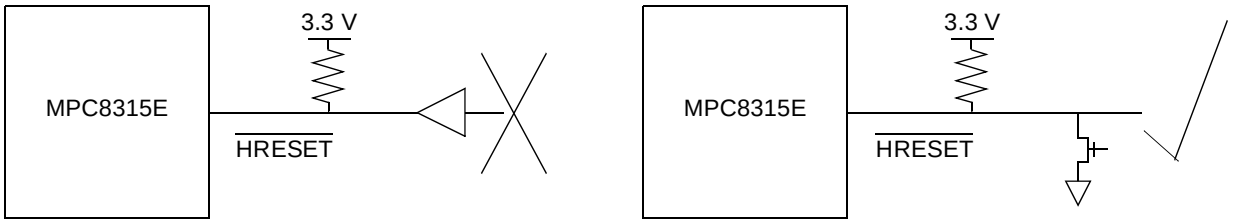


Figure 9. $\overline{\text{HRESET}}$ Connection

6 JTAG and Debug

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 11. Care must be taken to ensure that these pins are maintained at a valid negated state under normal operating conditions as most have asynchronous behavior and spurious assertion give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1™ specification, but it is provided on all processors that implement Power Architecture™. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{PORESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ independently to control the processor fully. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 11 allows the COP port to assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ independently, while ensuring that the target can drive $\overline{\text{PORESET}}$ as well.

The COP interface has a standard header, shown in Figure 10, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter- clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 10 is common to all known emulators.

If the JTAG interface and COP header are not used, Freescale recommends all of the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{PORESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{PORESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 11. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.

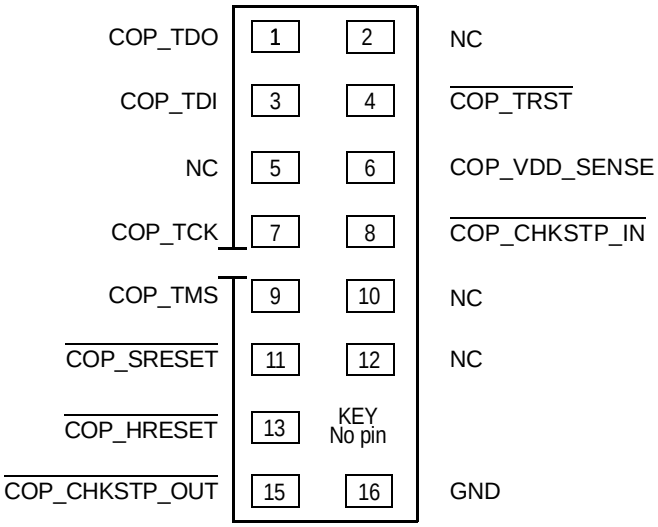
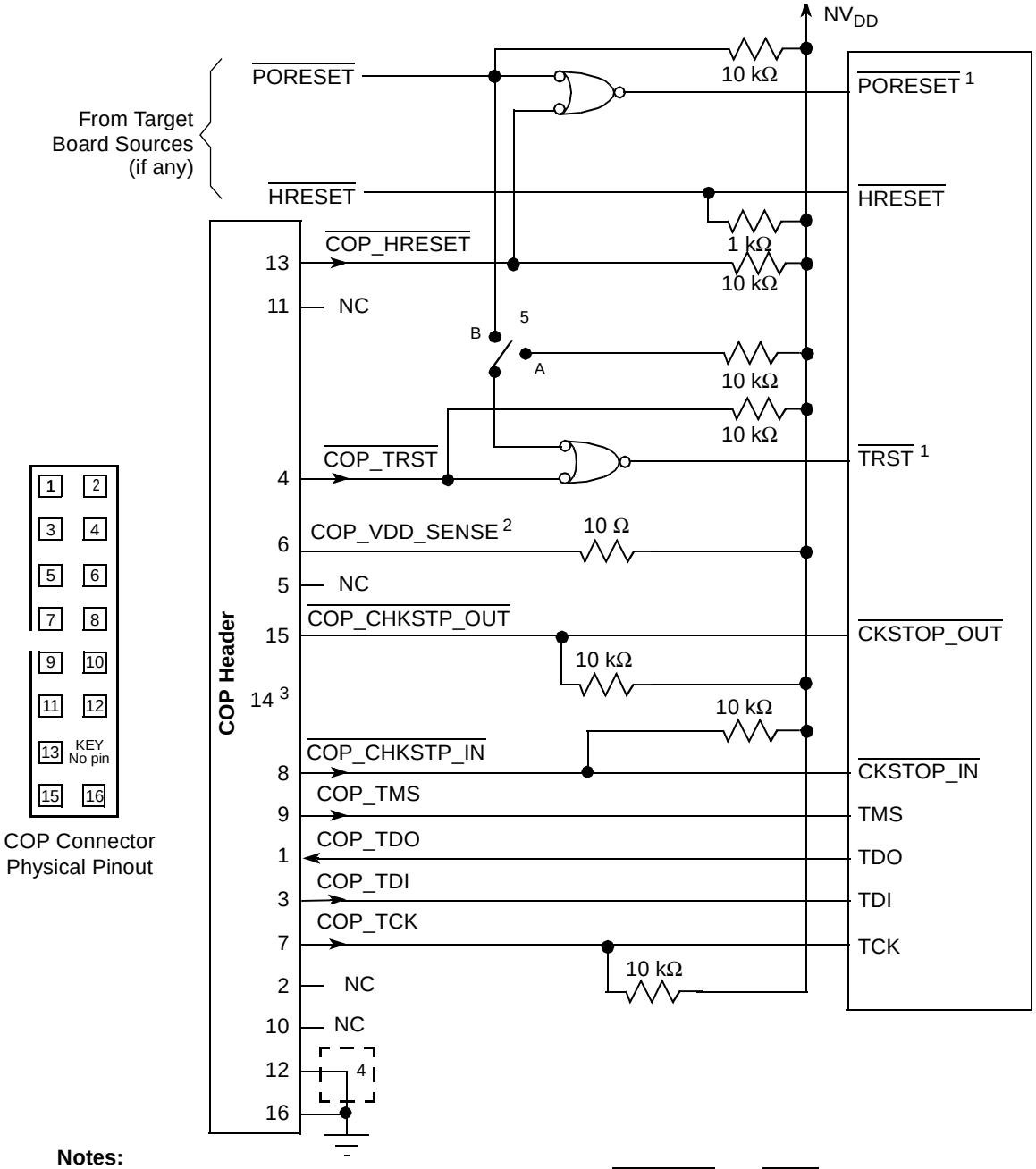


Figure 10. COP Connector Physical Pinout



Notes:

1. The COP port and target board should be able to assert $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ independently to the processor to control the processor fully as shown here.
2. Populate this with a 10 Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the /TRST line. If BSDL testing is not being performed, this switch should be closed to position B.

Figure 11. JTAG Interface Connection

Table 7 details the termination recommendations for the JTAG, TEST, PMC, and thermal management pins.

Table 7. JTAG and TEST Pin Listing

Signal	Pin Type	Termination		Notes
		If Used	If Not Used	
TCK	I	As needed + 10 kΩ to NV_{DD}	10 kΩ to NV_{DD}	Commonly used for boundary scan testing. If this pin is truly not used, it can be tied directly to GND.
TDI	I	As needed	Open	This JTAG pin has a weak internal pull-up P-FET that is always enabled.
TDO	O	As needed	Open	Actively driven during RESET
TMS	I	As needed	Open	This JTAG pin has a weak internal pull-up P-FET that is always enabled.
$\overline{\text{TRST}}$	I	Tie to the output of a Negative OR gate	Tie to $\overline{\text{PORESET}}$ through a 0 kΩ	This JTAG pin has a weak internal pull-up P-FET that is always enabled. If an In-Circuit Emulator is used in the design, $\overline{\text{TRST}}$ should be tied to the output of a Negative OR gate logic. The inputs to the Negative OR gate logic should be any external $\overline{\text{TRST}}$ source and the $\overline{\text{PORESET}}$ signal
Test				
TEST_MODE	I	Tie directly to GND		—
DEBUG				
$\overline{\text{QUIESCE}}$	O	As needed	Open	—
Thermal Management				
THERM0	I	As needed	Tie to GND using 4.7K or above	Thermal sensitive resistor

7 Functional Blocks

This section presents the recommendations and guidelines for designing with various functional blocks on the PowerQUICC II Pro.

7.1 PCI Bus Interface

The reset configuration word high controls the hardware configuration of the PCI blocks as follows:

- RCWH[PCIHOST]— Host/agent mode for PCI
- RCWH[PCIARB]—PCI internal/external arbiter mode select.

As Table 8 shows, signals of the PCI interface are multiplexed with the CompactPCI Hot Swap pins. Either PCI or Hot Swap functionality is selected by the RCWH[PCIARB] bit setting. When an external arbiter is selected (RCWH[PCIARB] = 0), the CompactPCI Hot Swap pins function. When an internal arbiter is selected (RCWH[PCIARB] = 1), the $\overline{\text{GNT}}x/\overline{\text{REQ}}x$ pins function. Refer to the *MPC8315E PowerQUICC*

II Pro Integrated Host Processor Family Reference Manual for details on the reset configuration word high settings.

Table 8. PCI Bus Interface Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{PCI\_INTA}}$	O	2 k–10 kΩ to NV_{DD}	Open	Open drain signal. In agent mode, $\overline{\text{INTA}}$ typically connects to a central interrupt controller.
$\overline{\text{PCI\_RESET\_OUT}}$	O	As needed	Open	This signal is used only in host mode. It should be left unconnected in agent mode.
PCI_AD[31:0]	I/O	As needed	2 k–10 kΩ to NV_{DD} or Open	If the PCI port is not used, no termination is needed if the bus is parked. Software needs to park the bus as follows: 1. RCWHR[PCIHOST] = 1 2. RCWHR[PCIARB] = 1 3a. PCIACR[PM]=1, or 3b. PCI_GCR[BBR] = 1
PCI_C/$\overline{\text{BE}}$[3:0]	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD} or Open	If the PCI port is not used, no termination is needed if the bus is parked. Software needs to park the bus as follows: 1. RCWHR[PCIHOST] = 1 2. RCWHR[PCIARB] = 1 3a. PCI Arbiter Control Configuration Register PM bit = 1, or 3b. PCI_GCR[BBR] = 1
PCI_PAR	I/O	As needed	2 k–10 kΩ to NV_{DD}	If the PCI port is not used, this signal must be pulled up.
$\overline{\text{PCI\_FRAME}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	PCI specification requires a weak pullup.
$\overline{\text{PCI\_TRDY}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	PCI specification requires a weak pullup.
$\overline{\text{PCI\_IRDY}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	PCI specification requires a weak pullup.
$\overline{\text{PCI\_STOP}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	PCI specification requires a weak pullup.
$\overline{\text{PCI\_DEVSEL}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	PCI specification requires a weak pullup.
PCI_IDSEL	I	**PCI host:** Tie to GND **PCI agent:** One of PCI_AD[31:0]	Tie to GND using 4.7K	IDSEL should be connected to GND for host systems and to one address line for agent systems. If the PCI port is not used, it should be grounded. • PCI host is selected by RCWH[PCIHOST] = 1. • PCI agent is selected by RCWH[PCIHOST] = 0.

Table 8. PCI Bus Interface Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{PCI\_SERR}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	PCI specification requires a weak pullup.
$\overline{\text{PCI\_PERR}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	PCI specification requires a weak pullup.
$\overline{\text{PCI\_REQ0}}$	I/O	**External arbiter:** As needed **Internal arbiter:** As needed + 2 k–10 kΩ to NV_{DD}	**External arbiter:** Open **Internal arbiter:** 2 k–10 kΩ to NV_{DD}	If an external arbiter is used, $\overline{\text{REQ0}}$ becomes an *output* signal and does not need to be terminated. • External arbiter selected by RCWH[PCIARB] = 0. • Internal arbiter selected by RCWH[PCIARB] = 1.
$\overline{\text{PCI\_REQ}}$[1]/ CPCI_HS_ES	I	**External arbiter:** As needed **Internal arbiter:** As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	This pin is multiplexed with a CompactPCI Hot Swap function. CompactPCI functionality selected when external arbiter is used. • External arbiter selected by RCWH[PCIARB] = 0. • Internal arbiter selected by RCWH[PCIARB] = 1.
$\overline{\text{PCI\_REQ}}$[0:2]	I	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	
$\overline{\text{PCI\_GNT}}$[0]	I/O	**External arbiter:** As needed + 2 k–10 kΩ to NV_{DD} **Internal arbiter:** As needed	**External arbiter:** 2 k–10 kΩ to NV_{DD} **Internal arbiter:** Open	If an external arbiter is used, $\overline{\text{GNT0}}$ becomes an *input* signal and should be pulled up with 2 k–10 kΩ to NV_{DD}. • External arbiter selected by RCWH[PCIARB] = 0. • Internal arbiter selected by RCWH[PCIARB] = 1.
$\overline{\text{PCI\_GNT}}$[1]/ CPCI_HS_LED	O	As needed	Open	This pin is multiplexed with a CompactPCI Hot Swap function. CompactPCI functionality selected when external arbiter is used. • External arbiter selected by RCWH[PCIARB] = 0. • Internal arbiter selected by RCWH[PCIARB] = 1.

Table 8. PCI Bus Interface Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{PCI\_GNT}}$[2]/ CPCI_HS_ENUM	O	**External arbiter:** As needed + 2 k–10 kΩ to NV_{DD} **Internal arbiter:** As needed	**External arbiter:** Open **Internal arbiter:** Open	This pin is multiplexed with a CompactPCI Hot Swap function. CompactPCI functionality selected when external arbiter is used. • If **CompactPCI** Hot Swap function is used, a weak pullup is required (2 k–10 kΩ to NV_{DD}). • External arbiter selected by RCWH[PCIARB] = 0. • Internal arbiter selected by RCWH[PCIARB] = 1.
$\overline{\text{PCI\_PME}}$	IO	**As needed** 2 k–10 kΩ to NV_{DD}	Open	This pin has a weak internal pull up. No role if PCI is not used.
M66EN	I	As needed	5 kΩ to NV_{DD} or 1 kΩ to GND	Open-drain signal. No role if PCI is not used.

7.2 DDR SDRAM

Refer to the following application notes for details on layout consideration and DDR programming guidelines:

- AN2582: *Hardware and Layout Design Considerations for DDR Memory Interfaces,* for signal integrity and layout considerations.
- AN2583: *Programming the PowerQUICC™ III DDR SDRAM Controller,* for DDR programming guidelines.

The DDR controller on the PowerQUICC II Pro can be configured with a 32- or 16-bit data bus interface. The DDR_SDRAM_CFG[DBW] bit controls the bus width selection. The burst length is set to 8 beats for 32-bit mode by properly configuring the DDR_SDRAM_CFG[8_BE] bit. Refer to the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for details on these register settings.

NOTE

For PowerQUICC II Pro devices, only the source synchronous clock mode is supported for the DDR controller. Software must ensure that the DDR_SDRAM_CLK_CNTL[SS_EN] bit is set to 1 before the DDR interface is enabled.

Table 9 summarizes the DDR SDRAM pins.

Table 9. DDR SDRAM Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
MDQ[0:31]	I/O	As needed	Open	When in use, proper signal integrity analysis must be performed using the respective device IBIS model. Parallel termination is optional for DDR signals and should be simulated to verify necessity. • Parallel termination is optional for DDR signals and should be simulated to verify necessity. • Differential termination is included on DIMMs. It is only required for discrete memory applications.
MDM[0:3]	O	As needed	Open	—
MDQS[0:3]	I/O	As needed	Open	In 16 bit mode, unused MDQS[2:3] should be grounded through 150ohm resistor
MBA[0:2]	O	As needed	Open	—
MA[0:14]	O	As needed	Open	—
$\overline{\text{MWE}}$	O	As needed	Open	—
$\overline{\text{MRAS}}$	O	As needed	Open	—
$\overline{\text{MCAS}}$	O	As needed	Open	—
$\overline{\text{MCS}}$[0:1]	O	As needed	Open	—
MCKE	O	As needed	Open	This output is actively driven during reset rather than being three-stated during reset.
MCK	O	As needed	Open	—
$\overline{\text{MCK}}$	O	As needed	Open	—
ODT[0:1]	O	As needed	Open	—

7.3 Enhanced Local Bus Controller

The eLBC provides one GPCM, one FCM, and three UPMs for the local bus, with no restriction on how many of the four banks (chip selects) can be programmed to operate with any given machine. When a memory transaction is dispatched to the eLBC, the memory address is compared with the address information if each bank. The corresponding machine assigned to that bank (GPCM, FCM or UPM) then takes ownership of the external signals that control the access and maintains control until the transaction ends. Thus, with the eLBC in GPCM or FCM, or UPM mode, only one of the four chip selects is active at any time for the duration of the transaction.

The local bus clock is not configured while it is executing from the local bus, but rather by executing code from the DDR. The PowerQUICC II Pro local bus features a multiplexed address and data bus, LAD[0:15]. An external latch is required to de-multiplex these signals to the connecting device.

7.3.1 Local Bus Address

Figure 12 shows the correct way to make the address for the local bus.

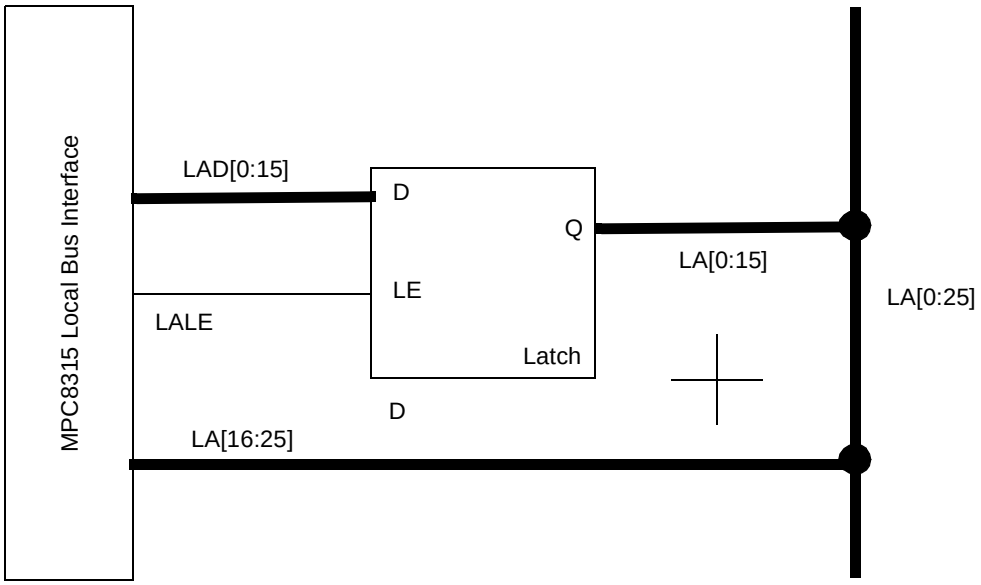


Figure 12. Local bus address

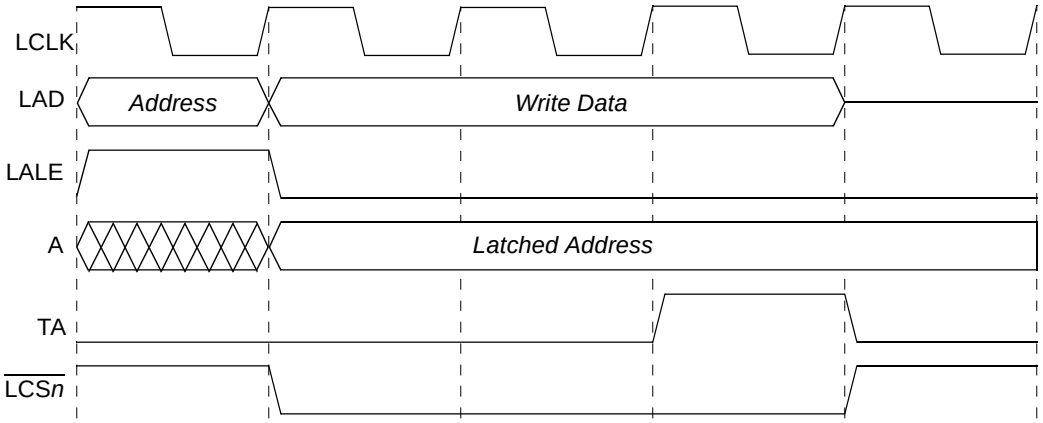


Figure 13. LALE timing

For every assertion of $\overline{\text{LCS}}n$, LALE is asserted first. While LALE is asserted, all other control signals are negated. The duration of LALE can be programmed to 1–4 cycles in LCRR[EADC]. The default is 4 cycles. The timing of LALE negation is important to ensure the correct latch. If the change of LAD and negation of LALE are too close and the margin for the latch is not sufficient, RCWHR[LALE] can be set. LALE is negated ½ a local bus clock earlier, which should ensure enough margin.

Table 10 lists guidelines for connecting to 8-bit, and 16-bit devices. LAD[0] is the most significant address and data bit, and LAD[15] is the least significant address and data bit. Notice that for a 16-bit port connection, the address LA[25] is normally not required because byte lane control is achieved through signals as outlined in Table 10.

Table 10. Local Bus Byte Lane Control

Device Data Width	Address	Data	Byte Lane Control		
			GPCM	FCM	UPM
8-bit	LA[0:25]	LAD[0:7]	$\overline{\text{LWE}}$[0]	LFWE	$\overline{\text{LBS}}$[0]
16-bit	LA[0:24]	LAD[0:15]	$\overline{\text{LWE}}$[0:1]	—	$\overline{\text{LBS}}$[0:1]

7.3.2 NAND Flash Interface

The FCM provides a glueless interface to parallel-bus NAND flash EEPROM devices. The figure given below shows a simple connection between an 8-bit port size NAND flash EEPROM and the eLBC in FCM mode. Commands, address bytes and data are all transferred on LAD[0:7].

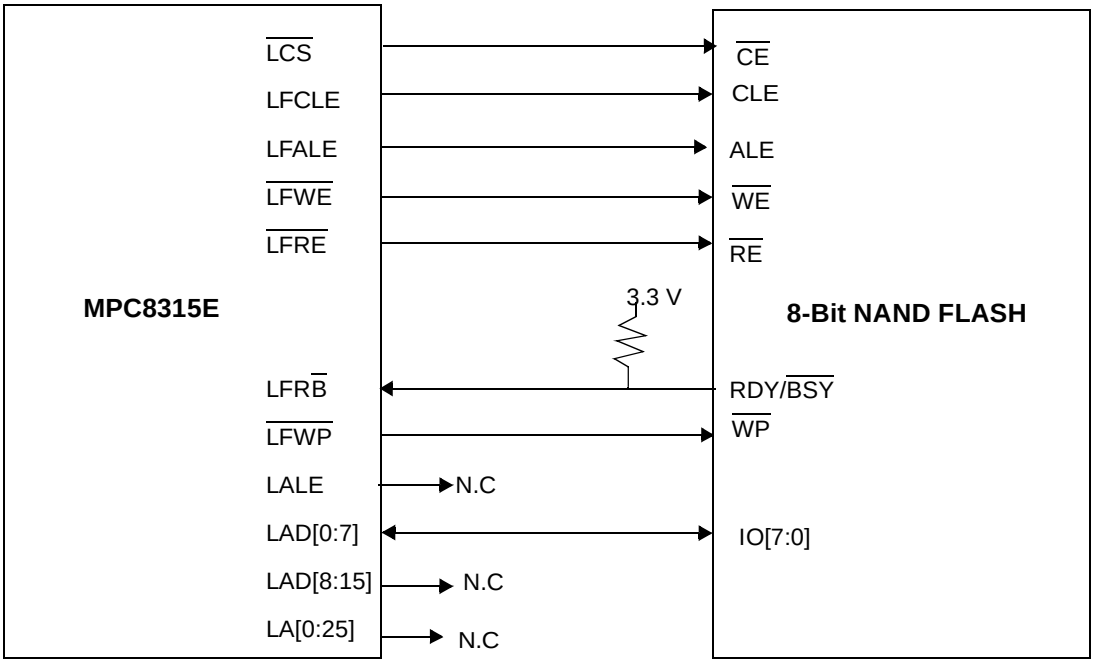


Figure 14. NAND Flash Connection Diagram

Table 11 summarizes the local bus pins.

Table 11. Local Bus Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
LAD[0:15]	I/O	As needed	Open	—
LA[16:25]	O	As needed	Open	—
$\overline{\text{LCS}}$[0:3]	O	As needed	Open	—
$\overline{\text{LWE}}$/$\overline{\text{LFWE}}$/ $\overline{\text{LBS}}$	O	As needed	Open	—
LBCTL	O	As needed	Open	—
LALE	O	As needed	Open	—
LGPL0/LFCLE	O	As needed	Open	—
LGPL1/**LFALE**	O	As needed	Open	—
LGPL2/$\overline{\text{LFRE}}$/$\overline{\text{LOE}}$	O	As needed	Open	—
LGPL3/$\overline{\text{LFWP}}$	O	As needed	Open	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ LFR$\overline{\text{B}}$	I/O	As needed	Open	Output when configured as LGPL4. This pin has a weak internal pull up.
LGPL5	O	As needed	Open	—
LCLK[0:1]	O	As needed	Open	—

Note: All local bus signals are HiZ during $\overline{\text{PORESET}}$ assertion. During RCW loading, the state is as shown in Reference manual: "Output Signal States During Reset"

7.4 General-Purpose I/O Timers

Four general-purpose timers are multiplexed with the GPIO[0:11] pins. Each timer interface consists of the $\overline{\text{TGATE}}$*n*, TIN*n*, and $\overline{\text{TOUT}}$*n* pins. Each timer pin is programmed using the system I/O configuration High (SICRH) register.

GPIO[0:11] are multiplexed with general-purpose timer interface pins. DMA control signals are also multiplexed with some of the GPIO signals. Each GPIO pin is programmed using the system I/O configuration low (SICRL) and system I/O configuration register high (SICRH) registers.

Table 12 summarizes the general-purpose I/O pins.

Table 12. General-Purpose I/O Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
GPIO_0/ DMA_DREQ/GTM1_TOUT1	I/O	As needed	Open	Pin functionality determined by SICRH[0–1]
GPIO_1/DMA_DACK1/–GTM1_TIN2/GTM2_TIN1	I/O	As needed	Open	Pin functionality determined by SICRH[2–3]
GPIO_2/DMA_DONE1/GTM1_TGATE2/GTM2_TGATE1	I/O	As needed	Open	Pin functionality determined by SICRH[4–5]
GPIO_3/GTM1_TIN3/GTM2_TIN4	I/O	As needed	Open	Pin functionality determined by SICRH[6–7]
GPIO_4]/GTM1_TGATE3/GTM2_TGATE4	I/O	As needed	Open	Pin functionality determined by SICRH[8–9]
GPIO_5]/GTM1_TOUT3/GTM2_TOUT1	I/O	As needed	Open	Pin functionality determined by SICRH[10–11]
GPIO_6/GTM1_TIN4/GTM2_TIN3	I/O	As needed	Open	Pin functionality determined by SICRH[12–13]
GPIO_7/GTM1_TGATE4/GTM2_TGATE3	I/O	As needed	Open	Pin functionality determined by SICRH[14–15]
GPIO_8/USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2	I/O	As needed	Open	Pin functionality determined by SICRH[16–17]
GPIO_9/USBDR_PWRFAULT/GTM1_TGATE1/GTM2_TGATE2	I/O	As needed	Open	Pin functionality determined by SICRH[18–19]
GPIO_10/USBDR_PCTL0/GTM1_TOUT2/GTM2_TOUT1	I/O	As needed	Open	Pin functionality determined by SICRH[20–21]
GPIO_11/USBDR_PCTL1/GTM1_TOUT4/GTM2_TOUT3	I/O	As needed	Open	Pin functionality determined by SICRH[22–23]

Note: It is recommended that GPIO pins be programmed to outputs when not used.

7.5 Universal Serial Bus (USB)

Figure 15 shows the USB interface block diagram.

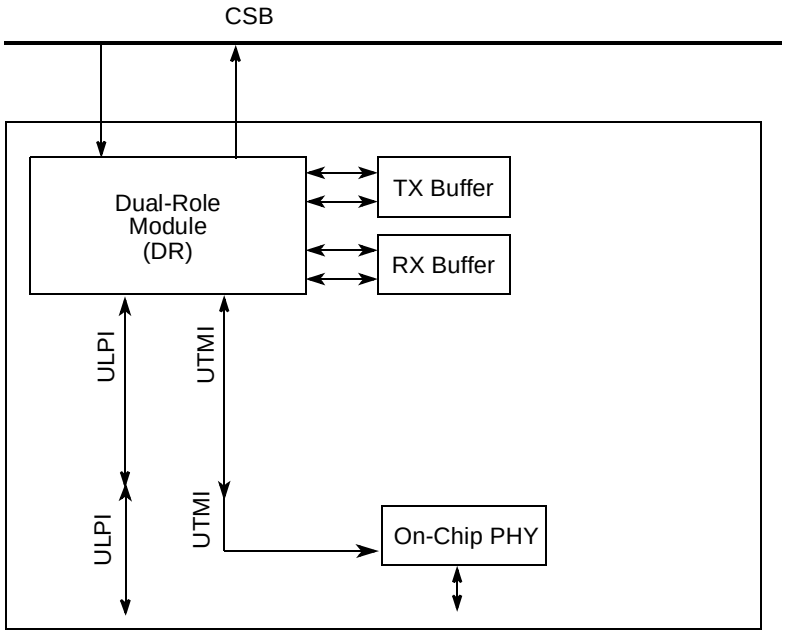


Figure 15. USB Interface Block Diagram

The USB DR module is a USB 2.0- compliant serial interface engine for implementing a USB interface. The DR controller can act as a device or host controller. Interfaces to negotiate the host or device role on the bus in compliance with the on-the-go (OTG) supplement to the USB specification are also provided. The DR module supports the required signaling for USB transceiver macrocell interface (UTMI) and UTMI low pin count interface (ULPI) transceivers (PHYs). The PHY interfacing to the UTMI is an internal PHY and the PHY interfacing to the ULPI is an external PHY.

The USB DR module has three basic operating modes: host, device, and OTG. The module can be configured to use one of two different PHY interfaces: ULPI or UTMI. OTG is supported only through ULPI and is not supported through the UTMI interface

7.5.1 UTMI Interface

The integrated USB PHY has four dedicated external signals, which are only used when the MPC8315E is a host: USBDR_DRIVE_VBUS, USBDR_PWRFAULT, USBDR_PCTL0, and USBDR_PCTL1.

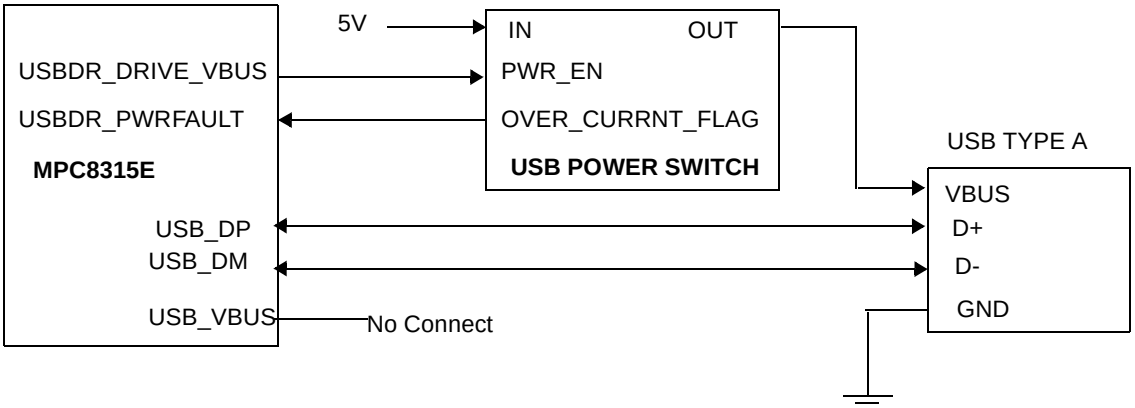


Figure 16. USBDR as HOST in UTMI Mode

The connection diagram shows how the USBDR_DRIVE_VBUS and USBDR_PWRFAULT should be used when the MPC8315E is acting as USB Host in UTMI mode. The USBDR_PCTL0 and USBDR_PCTL1 are status pins used to drive LEDs. The 15 kΩ resistor terminations are built in and not required externally. The VBUS is an output during Host and should be left unconnected. This table summarizes the USBDR as Host in UTMI mode.

Table 13. USBDR Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
USB_DP	I/O	As needed	Open	—
USB_DM	I/O	As needed	Open	—
USB_TPA	I/O	As needed	Open	—
USB_VBUS	I/O	Open	Open	—
USB_VDDA, USB_VDDA_BIAS, USB_PLL_PWR1, USB_PLL_PWR3	I/O	Tie to respective proper power lines	Tie to respective proper power lines	—
USB_VSSA, USB_VSSA_BIAS, USB_PLL_GND	I/O	GND	GND	—
USB_RBIAS	I/O	10 kΩ to GND	10 kΩ to GND	—

This figure shows how the UTMI signals should be used in device mode.

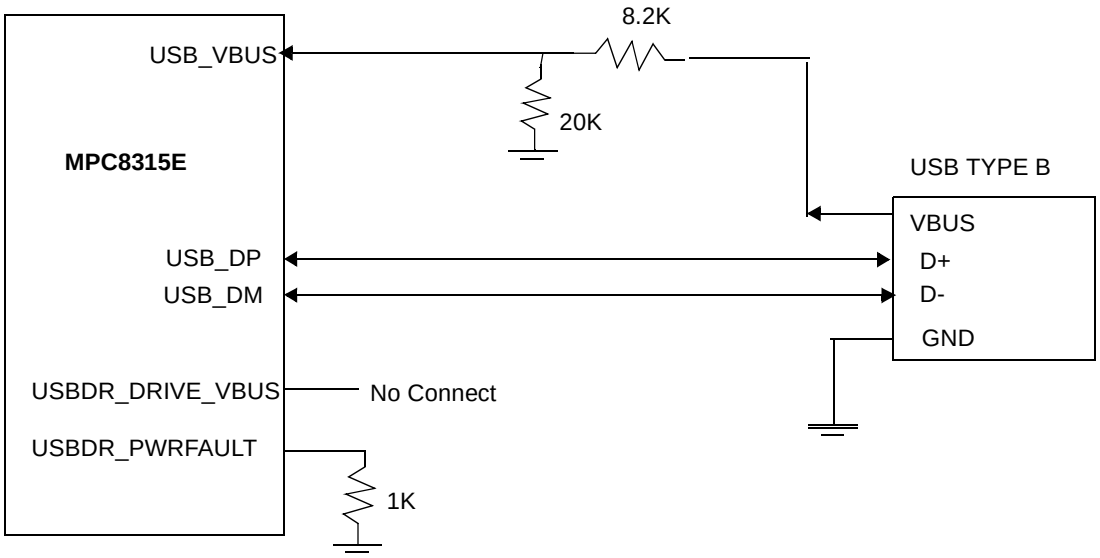


Figure 17. USBDR as DEVICE in UTMI Mode

The 1.5 K pullup resistors that determine the speed are not externally required and the VBUS of the MPC 8315E should not be directly fed with 5 V input. The recommended voltage divider circuit is shown in Figure 17.

Table 14. ULPI Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
USBDR_TXRX[0:7]	I/O	As needed	Open	Pin functionality determined by SICRL[24–25] and SICRL[26–27] bit settings.
USBDR_CLK	I	As needed	1 kΩ to GND	Pin functionality determined by SICRL[26] bit setting.
USBDR_NXT	I	As needed	1 kΩ to GND	Pin functionality determined by SICRL[26–27] bit setting.
USBDR_DIR	I	As needed	1 kΩ to GND	Pin functionality determined by SICRL[26–27] bit setting.
USBDR_STP	O	As needed	Open	Pin functionality determined by SICRL[28–29] bit setting.
USBDR_PWRFAULT	I	As needed	1 kΩ to GND	Pin functionality determined by SICRH[18–19] bit setting.
USBDR_DRIVE_VBUS	O	As needed	Open	Pin functionality determined by SICRH[16–17] bit setting.
USBDR_PCTL0	O	As needed	Open	Pin functionality determined by SICRH[20–21] bit setting.
USBDR_PCTL1	O	As needed	Open	Pin functionality determined by SICRH[22–23] bit setting.
RBIAS	I	10K to GND	10K to GND	Use 1 percent precision resistor.

7.6 Integrated Programmable Interrupt Controller (IPIC)

The integrated programmable interrupt controller (IPIC) provides interrupt management for receiving hardware-generated interrupts from internal and external sources. It also prioritizes and delivers the interrupts to the CPU for servicing. The $\overline{\text{IRQ}}$ lines are multiplexed with signals CKSTOP_IN and CKSTOP_OUT interface pins. The configuration of each $\overline{\text{IRQ}}$ pin is programmed using the system I/O configuration high register (SICRH). Table 15 summarizes the programmable interrupt controller pins.

Table 15. Programmable Interrupt Controller Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{MCP\_OUT}}$	O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	Open-drain signal
$\overline{\text{IRQ}}$[0]/$\overline{\text{MCP\_IN}}$	I	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	—
$\overline{\text{IRQ}}$[1]	I	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	—
$\overline{\text{IRQ}}$[2]	I	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	—

Table 15. Programmable Interrupt Controller Pin Listing (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{IRQ}}$[3]	I	As needed + 2k–10k Ω to NV_{DD}	2 k–10 kΩ to NV_{DD}	—
$\overline{\text{IRQ}}$[4]	I	As needed + 2k–10k Ω to NV_{DD}	2 k–10 kΩ to NV_{DD}	—
$\overline{\text{IRQ5}}$/$\overline{\text{CORE\_SRESET\_IN}}$	I	As needed + 2k–10k to NVDD	2k–10k to NVDD	Pin functionality determined by SICRL[7–8] bit settings.
$\overline{\text{IRQ6}}$/CKSTOP_OUT	I/O	As needed + 2k–10k to NVDD	2k–10k to NVDD	Pin functionality determined by SICRL[9] bit setting.
$\overline{\text{IRQ7}}$/CKSTOP_IN	I	As needed + 2k–10k to NVDD	2k–10k to NVDD	Pin functionality determined by SICRL[9] bit setting.

7.7 Time-Division Multiplexing (TDM)

Four to six signals are required for TDM full-duplex operation, depending on the selected operating mode (shared or independent). The function of the I/O pins for the TDM is determined by a number of control bits, and the direction of clocks and frame syncs can also be configured. Each signal pin can be configured as an input or output. The frame syncs and the clocks can be shared with the other TDM modules on-chip. Table 16 lists the TDM pins.

Table 16. TDM Controller Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
TDM_RCK/ GPIO_18	I/O	As needed	2k–10k to NVDD	Pin functionality is determined by the SICRL[14–15] bit settings. In shared mode, this pin can be ignored or used as GPIO.
TDM_RFS/ GPIO_19	I/O	As needed	2k–10k to NVDD	Pin functionality is determined by the SICRL[14–15] bit settings. In shared mode, this pin can be ignored or used as GPIO.
TDM_RD/ GPIO_20	I/O	As needed	2k–10k to NVDD	Pin functionality is determined by the SICRL[12–13] bit settings.
TDM_TCK/ GPIO_21	I/O	As needed	2k–10k to NVDD	Pin functionality is determined by the SICRL[12–13] bit settings. In shared mode, this clock is used by both transmitter and receiver.
TDM_TFS/ GPIO_22	I/O	As needed	2k–10k to NVDD	Pin functionality is determined by the SICRL[12–13] bit settings. In shared ode, this pin is used as a sync by both the transmitter and receiver.
TDM_TD/ GPIO_23	I/O	As needed	2k–10k to NVDD	Pin functionality is determined by the SICRL[12–13] bit settings.

7.8 Enhanced Three-Speed Ethernet Controllers (eTSEC)

The enhanced three-speed Ethernet controller (eTSEC) supports 10, 100, and 1000 Mbps Ethernet/ IEEE Std 802.3™ networks. The complete eTSEC is designed for single MAC applications with several standard MAC-PHY interfaces to connect to an external Ethernet transceiver:

- IEEE 802.3, IEEE 802.3u, IEEE 802.3x, IEEE 802.3z, IEEE 802.3ac, and IEEE 802ab-compatible
- 10/100 Mbps IEEE 802.3 MII and RMII
- 10/100 Mbps RGMII
- 1000 Mbps full-duplex RGMII
- 10/100 Mbps SGMII
- 1000 Mbps full-duplex SGMII
- 1000 Mbps RTBI

Two eTSECs can be independently configured to support any one of these interfaces. The reset configuration word high controls the hardware configuration of the two eTSEC MAC-PHY interfaces. RCWH[TSEC1M] and RCWH[TSEC2M] are used to configure eTSEC1 and eTSEC2, respectively, in either MII, RMII, RGMII, RTBI or SGMII mode.

eTSEC1 interface pins are multiplexed with USBDR ULPI interface pins and GPIO pins; some eTSEC2 interface pins are multiplexed with GPIO pins and the Reset configuration source signals. Each eTSEC pin is programmed using the system I/O configuration register low (SICRL) register.

Table 17 shows the pin usage and software configuration for each particular MAC-PHY mode. eTSEC interface pins not used in a particular MAC-PHY mode, can be used as GPIO by setting the appropriate bits in the SICRH register.

Table 17. eTSEC MAC-PHY Modes

	MII	RMII	RGMII	RTBI
EC_GTX_CLK125	—	—	125 MHz clock	125 MHz clock
eTSEC*n*_COL	COL	—	—	—
eTSEC*n*_CRS	CRS	—	—	—
eTSEC*n*_GTX_CLK	—	—	GTX_CLK	GTX_CLK
eTSEC*n*_RX_CLK	RX_CLK	—	RX_CLK	RX_CLK
eTSEC*n*_RX_DV	RX_DV	RX_DV	RX_CTL	RCG[4]/RCG[9]
eTSEC*n*_RX_ER	RX_ER	RX_ER	—	—
eTSEC*n*_RXD[3:0]	RxD[3:0]	RxD[1:0]	RxD[3:0]	RCG[3:0]/RCG[8:5]
eTSEC*n*_TX_CLK	TX_CLK	REF_CLOCK	—	—
eTSEC*n*_TXD[3:0]	TxD[3:0]	TxD[1:0]	TxD[3:0]	TCG[3:0]/TCG[8:5]
eTSEC*n*_TX_EN	TX_EN	TX_EN	TX_CTL	TCG[4]/TCG[9]

Table 17. eTSEC MAC-PHY Modes (continued)

	MII	RMII	RGMII	RTBI
eTSEC*n*_TX_ER	TX_ER	TX_ER	—	—
Software configuration	RCWH[TSEC*n*M] = 000 MACCFG2[22–23] = 10	RCWH[TSEC*n*M] = 001 MACCFG2[22–23] = 10	RCWH[TSEC*n*M] = 011 MACCFG2[22–23] = 10	RCWH[TSEC*n*M] = 101 MACCFG2[22–23] = 10

The eTSEC has one management interface that controls all external PHYs. The management interface of eTSEC1 controls the PHY from eTSEC1 as well as all external PHYs. As mentioned earliest the eTSEC pins are multiplexed with GPIOs, USBDR pins and IEEE Std 1588™ pins and hence the pin functionality should be selected by properly setting the appropriate bits in SICRL and SICRH registers respectively. Table 18 summarizes the eTSEC pins.

Table 18. Enhanced Three-Speed Ethernet Controller Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
TSEC_MDC	O	As needed	Open	—
TSEC_MDIO	I/O	As needed + 2 k–10 kΩ to NV_{DD1_ON}	2 k–10 kΩ to NV_{DD1_ON}	Bidirectional signal
TSEC_GTX_CLK125	I	125 MHz clock	1 kΩ to GND	A 125 MHz reference clock should be supplied if either eTSEC is being used in RGMII or RTBI modes.
eTSECn_COL	I/O	As needed	1 kΩ to GND	—
eTSECn_CRS	I/O	As needed	1 kΩ to GND	—
eTSECn_GTX_CLK	O	As needed	Open	Actively driven during $\overline{\text{RESET}}$
eTSECn_RX_CLK	I	As needed	1 kΩ to GND	—
eTSECn_RX_DV	I	As needed	1 kΩ to GND	—
eTSECn_RX_ER	I	As needed	1 kΩ to GND	—
eTSECn_RXD[3:0]	I	As needed	1 kΩ to GND	—
eTSECn_TX_CLK	I	As needed	1 kΩ to GND	—
eTSECn_TXD[3:0]	O	As needed	Open	—
eTSECn_TX_EN	O	As needed	Open	—
eTSECn_TX_ER	O	As needed	Open	—

NOTE

- eTsec1: Pin Functionality determined by SICRL[24–29] bit settings.
- eTsec2: Pin functionality determined by SICRH[24–25] bit settings.

7.9 IEEE Std.1588™ Timer

The eTSEC includes a timer clock module to support the IEEE 1588 timer standard for a precision clock synchronization protocol for networked measurement and control systems. The MPC8315 provides a hardware assisted implementation in which timestamps are generated at the physical level.

Table 19 shows the IEEE 1588 timer pin listing and implementation notes.

Table 19. IEEE 1588 Timer Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
TSEC_TMR_CLK/TSEC1_RXD3	I	As needed	1 kΩ to GND	Pin functionality determined by SICRL[26–27]
TSEC_TMR_TRIG1/TSEC1_RXD2	I	As needed	1 kΩ to GND	Pin functionality determined by SICRL[26–27]
TSEC_TMR_TRIG2/TSEC1_RXD1	I	As needed	1 kΩ to GND	Pin functionality determined by SICRL[26–27]
TSEC_TMR_PP[3:1]/TSEC1_TXD[0:2]/ GPIO[30:28]	O	As needed	Open	Pin functionality determined by SICRL[28–29]
TSEC_TMR_GCLK/TSEC1_TXD3/ GPIO_28	O	As needed	Open	Pin functionality determined by SICRL[28–29]
TSEC_TMR_ALARM1/TSEC1_TX_EN/ GPIO_31	O	As needed	Open	Pin functionality determined by SICRL[28–29]
TSEC_TMR_ALARM2/TSEC1_TX_ER	O	As needed	Open	Pin functionality determined by SICRL[28–29]

IEEE 1588 pps signals are muxed with eTSEC1 signals and hence both cannot be used together. For minimizing the offset between slave and master clock, eTSEC MAC should get the 125-MHz clock from the PHY which is doing IEEE 1588 time-stamping.

7.10 SerDes PHY (PCI Express/SGMII Interface)

The SerDes PHY block operates in the following modes (see Figure 18):

- Two lanes running 1x SGMII at 1.25 Gbps
- Two lanes running 1x PCI Express at 2.5 Gbps.

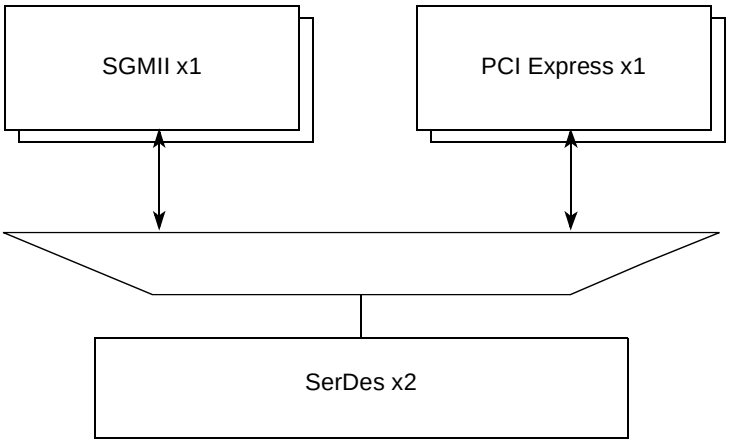


Figure 18. SerDes PHY Operating Modes

The SerDes interface is supported in both MPC8315E and MPC8314 devices, and Table 20 lists the pins and the implementation notes.

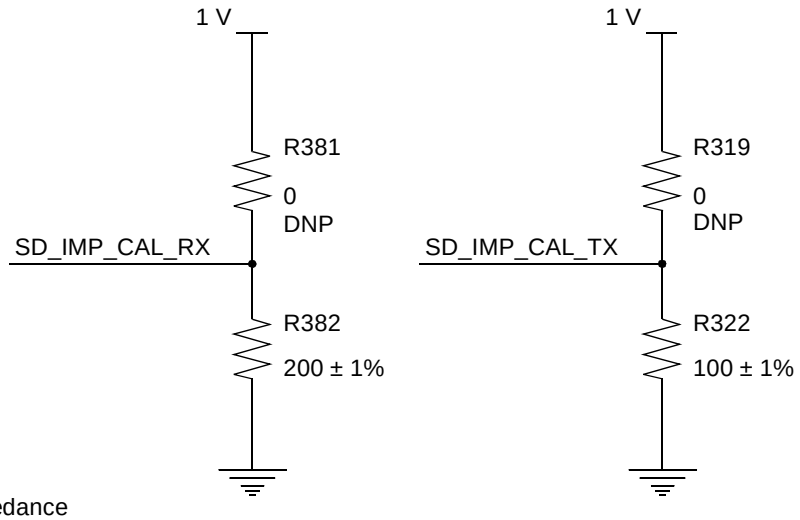
Table 20. SerDes Pin List

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
TXA	O	As needed	Open	Differential signal, serial transmitter, lane A, positive data
$\overline{\text{TXA}}$	O	As needed	Open	Differential signal, serial transmitter, lane A, negative data
RXA	I	As needed	Connect to GND	Differential signal, serial receiver, lane A, positive data
$\overline{\text{RXA}}$	I	As needed	Connect to GND	Differential signal, serial receiver, lane A, negative data
TXB	O	As needed	Open	Differential signal, serial transmitter, lane E, positive data
$\overline{\text{TXB}}$	O	As needed	Open	Differential signal, serial transmitter, lane E, negative data
RXB	I	As needed	Connect to GND	Differential signal, serial receiver, lane E, positive data
$\overline{\text{RXB}}$	I	As needed	Connect to GND	Differential signal, serial receiver, lane E, negative data
SD_REF_CLK	I	As needed	Connect to GND	SGMII: Single-ended 125 MHz clock/differential 125 MHz clock must be connected and the reference is 1 V. PCI Express: 100 MHz differential clock must be connected.
$\overline{\text{SD\_REF\_CLK}}$	I	As needed	Connect to GND	Differential clock input. When Single ended clock is used, leave this pin unconnected. **Note:** PCI express requires Differential clock only
SD_IMP_CAL_TX	I	Connect to GND using 100Ω precision resistor	Connect to 1 V	Transmitter impedance calibration High: Fixed Impedance Low: Impedance can be calibrated

Table 20. SerDes Pin List (continued)

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
SD_IMP_CAL_RX	I	Connect to GND using 200Ω precision resistor	Connect to 1 V	Receiver impedance calibration High: Fixed Impedance Low: Impedance can be calibrated
SD_PLL_TPD	O	Open	Open	Test point
SD_PLL_TPA_ANA	O	Open	Open	—

Figure 19 shows the connection diagram for the impedance calibration pins.



Note:

High: Fixed Impedance
Low: Calibration

Figure 19. Connection Diagram for Impedance Calibration Pins

PCI Express Layout Guidelines

The PCI Express layout guidelines are described as follows:

- Recommended microstrip trace routing guidelines
  - Single ended: 50–60 Ω +/– 15%
  - Differential: 100 Ω +/– 15%
- Recommended stripline trace routing guidelines
  - Single ended: 50–60 Ω +/– 15%
  - Differential: 100 Ω +/– 15%
- Recommended length matching intra-pair: Maximum 5 mil delta, matching maintained segment to segment, and matching at point of discontinuity. However, avoid tight bends.

- Recommended length matching inter-pair: Recommended to keep differences within 3 inches to minimize latency.
- Recommended for all differential signal pairs: Maintain ≥ 20 mil trace edge to plane edge gap.
- Gnd referenced signals is recommended.
- Use Gnd stitching vias by signal layer vias for layer changes.
- Do not route over plane splits or voids. Allow no more than a half trace width routed over via antipad.
- Via usage: Limit via usage to 4 vias per TX trace and 2 vias per RX trace (6 vias total, entire path).
- Bends: Match left/right turn bends whenever possible. No 90-degree bends or tight bend structures.
- The reference clock signal pair should maintain the same reference plane for the entire routed length and should not cross any plane splits (breaks in the reference plane).
- A minimum separation from the reference clock and other traces should be maintained. Assuming a trace width of 'w', no other trace or signal should be allowed within '3w'.
- The reference clock signal pair routing length should be minimized.
- The reference clock signal pair via count should be minimized. As a rule of thumb, via count should not exceed four.
- Reference clock terminating components should be placed as close as possible to their respective devices, ideally within 100 mils of the clock/receiver component pin.
- Match all segment lengths between differential pairs along the entire length of the pair.
- Maintain constant line impedance along the routing path by keeping the same line width and line separation.
- Avoid routing differential pairs adjacent to noisy signal lines or high speed switching devices, such as clock chips.
- Keep clock lines adequately separated from I/O lines.
- Recommended PCI Express reference clock to PCI express reference clock length matching to within 25 mils.
- Unused PCI Express clock outputs (unpopulated down devices or unpopulated add-in card connectors) should be disabled to limit EMI radiations and possible signal reflections.
- Decoupling capacitors: Several PCB-mounted 0.1 to 1.0 µF capacitors should be placed near the PCI Express silicon on the sides of the package to which the PCI Express I/O buffers connect.
- AC coupling capacitors:
  - Do not use capacitor-packs (C-packs) for PCI Express AC coupling capacitor purpose.
  - The same package size and value of capacitor should be used for each signal in a differential pair.
  - Locate capacitors for coupled traces in a differential pair at the same location along the differential traces. Place them as close to each other as possible, as allowed by DFM rules.
  - The breakout into and out of the capacitor mounting pads should be symmetrical for both signal lines in a differential pair.
- Test points and probing structures should not introduce stubs on the differential pairs.

7.11 SATA Controller

The SATA controller has the following features:

- Fully compliant with the *Serial ATA Specification*, revision 2.5.
- Supports both speeds: 1.5 Gbps (first-generation SATA) and 3 Gbps (second-generation SATA).
- Supports advanced technology attachment packet interface (ATAPI) devices.
- Contains a high-speed descriptor-based DMA controller.
- Native command queuing (NCQ) commands.
- Port multiplier operation.
- Hot plug, including asynchronous signal recovery.

Table 21 lists the pins available and the implementation notes.

Table 21. SATA Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
PINTXPLUSA	O	As needed	Open	Differential signal, serial transmitter, port A, positive data.
PINTXMINUSA	O	As needed	Open	Differential signal, serial transmitter, port A, negative data.
PINRXPLUSA	I	As needed	Connect to GND	Differential signal, serial receiver, port A, positive data.
PINRXMINUSA	I	As needed	Connect to GND	Differential signal, serial receiver, port A, negative data.
PINTXPLUSB	O	As needed	Open	Differential signal, serial transmitter, port B, positive data.
PINTXMINUSB	O	As needed	Open	Differential signal, serial transmitter, port B, negative data.
PINRXPLUSB	I	As needed	Connect to GND	Differential signal, serial receiver, port B, positive data.
PINRXMINUSB	I	As needed	Connect to GND	Differential signal, serial receiver, port B, negative data.
SATA_ANAVIZ	O	Open	Open	Connect it to a test point.
SATA_CLK_IN	I	As needed	Connect to GND	Connect 75 MHz clock to this pin. The reference is 3.3 V.
RESREF	I	As needed	Open	Connect a 2.7K 1% precision resistor between this pin and VSSRESREF. VSSRESREF is to be used as a low current ground connection for the External Resistor connection to the Bias Block.

Recommendations for SATA Board Layout

The recommendations for SATA board layout are as follows:

- The general differential routing guidelines for SATA are the same as given for PCI Express (see PCI Express Layout Guidelines”). However following points should be noted:
  - SATA signal should only be routed in the inner layer as a strip line. It should be controlled impedance line with differential impedance of 100 Ω.
  - Only 2 vias should be used; one to enter the stripline from the BGA pad and other to exit near the capacitor.

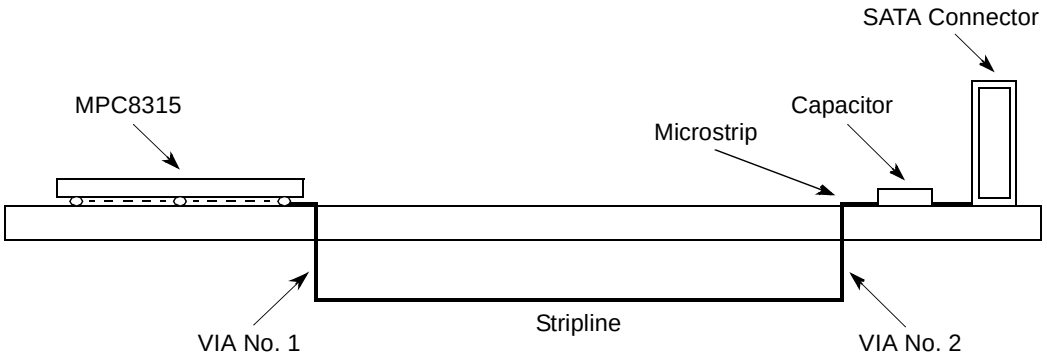


Figure 20. Recommended SATA Board Layout

- The AC coupling capacitors on the Tx and Rx lines for SATA should be of 10 nF. Use 0402 or smaller size and place the AC coupling capacitors close to the SATA connector to avoid layer switching between the cap and the SATA connector.
- The maximum routing length from the MPC8315 BGA pin to SATA connector should be less than 2 inches.
- Length mismatch between the PINTXPLUSn and PINTXMINUSn signals should not exceed 5 mils. Similar condition holds true for the PINRXPLUSn and PINRXMINUSn signals.
- Route the traces as straight as possible with minimum bends and avoid using serpentine for matching lengths. Length matching between the Tx pair and Rx pair is not mandatory.

• All SATA connectors and cables should be SATA compliant. Refer chapter 6 of Serial ATA Revision 2.5.

7.12 DMA

Table 22 lists the DMA signals.

Table 22. DMA Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{DMA\_DREQ0}}$/ GPIO_12	I/O	As needed	2 k–10 kΩ to NV_{DD}	DMA request input. Connect a 4.7K pull-up. Pin functionality is determined by the SICRL[0–1] bit settings.
$\overline{\text{DMA\_DACK0}}$/ GPIO_13	I/O	As needed	2 k–10 kΩ to NV_{DD}	DMA acknowledge output. Connect a 4.7K pull-up. Pin functionality is determined by the SICRL[0–1] bit settings.
DMA_DONE0/ GPIO_14	I/O	As needed	2 k–10 kΩ to NV_{DD}	DMA transfer completion status signal.Pin functionality is determined by the SICRL[0–1] bit settings.

7.13 DUART

Table 23 lists the dual UART pins.

Table 23. Dual UART Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
UART_SOUT[1:2]	O	As needed	Open	Pin functionality determined by SICRL[4–5] bit setting.
UART_SIN[1:2]	I/O	As needed	2 k–10 kΩ to NV_{DD}	Pin functionality determined by SICRL[4–5] bit setting.
$\overline{\text{UART\_CTS}}$[1]	I/O	As needed	2 k–10 kΩ to NV_{DD}	Pin functionality determined by SICRL[4–5] bit setting.
$\overline{\text{UART\_RTS}}$[1]	O	As needed	Open	Pin functionality determined by SICRL[4–5] bit setting.
$\overline{\text{UART\_CTS}}$[2]	I	As needed	2 k–10 kΩ to NV_{DD}	Pin functionality determined SICRL[4–5] bit setting. • If the UART is not used connect a pull-up resistor. • If the UART is used, but the hardware handshaking is not used, connect a pull-down resistor.
$\overline{\text{UART\_RTS}}$[2]	O	As needed	Open	—

7.14 I^2C Interface

Table 24 lists the I^2C pins.

Table 24. I^2C Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
IIC_SCL/ $\overline{\text{CKSTOP\_IN}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Open-drain signal • Pin functionality determined by SICRL[10–11] setting.
IIC_SDA/ $\overline{\text{CKSTOP\_OUT}}$	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Open-drain signal • Pin functionality determined by SICRL[10–11] setting.

7.15 SPI

Table 25 lists the SPI pins.

Table 25. SPI Pin Listing

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
SPIMOSI/ GPIO_15	I/O	**SPI:** As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Software configurable open-drain signal using SPMODE[OD] bit. Pull-up required only if configured as open drain. • Pin functionality determined by SICRL[2–3] bit setting.
SPIMISO/ GPIO_16	I/O	**SPI:** As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Software configurable open-drain signal using SPMODE[OD] bit. Pull-up required only if configured as open drain. • Pin functionality determined by SICRL[2–3] bit setting.
SPICLK	I/O	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Software configurable open-drain signal using SPMODE[OD] bit. Pull-up required only if configured as open-drain.
SPISEL/ GPIO_17	I	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	• Should be used when SPI configured as Slave • Pin functionality determined by SICRL[2–3] bit setting.

7.16 PMC

The core power (VDD) can be switched off as part of power management and the simple connection diagram shows how the external signals of MPC8315E help to implement the feature. However a partial core (VDDC) is always provided with power and should not be switched off. Along with the core, some of the I/Os can also be switched off during low-power mode by using load switches (MOSFETS).

A low power mode (D3Warm) can be achieved using a split supply, which makes the blocks—VDDC, NVDD1_ON, NVDD2_ON, and LVDD2_ON—power-on selectively while the rest of the blocks—VDD, GVDD, NVDD3_OFF, NVDD2_OFF, NVDD4_OFF, NVDD1_OFF, VDD1IO, NVDD3_OFF, SATA_VDD, VDD33_ANA, VDD33_PLL, LVDD1_OFF, XPADVDD, XCOREVDD, USB_VDDA, USB_PLL_PWR1, and USB_PLL_PWR3—are powered-off.

Support from wake-up exist on the Ethernet (ETSEC_2), GPIO (GPIO_0, GPIO_1), interrupt (IRQ_1, IRQ_2), and general purpose timers (GTMs) in D3Warm state.

7.16.1 Switching Off Core VDD

Figure 21 and Figure 22 show ways of switching off Core VDD.

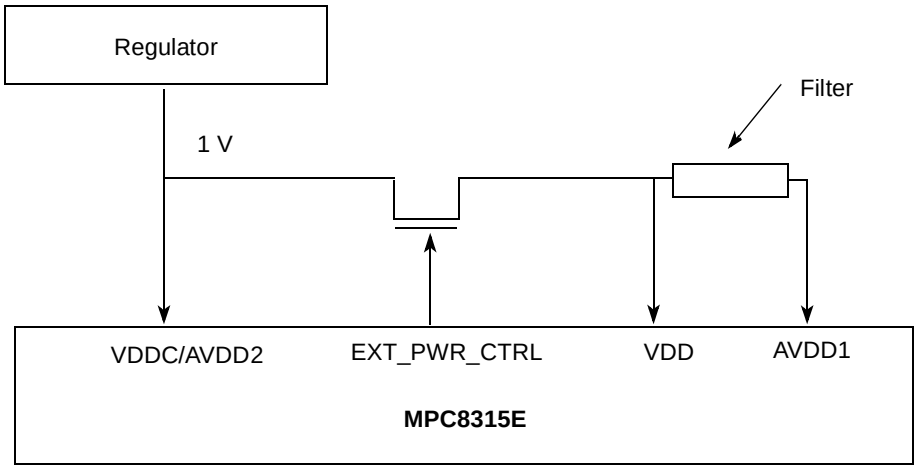


Figure 21. Switching off VDD using FET

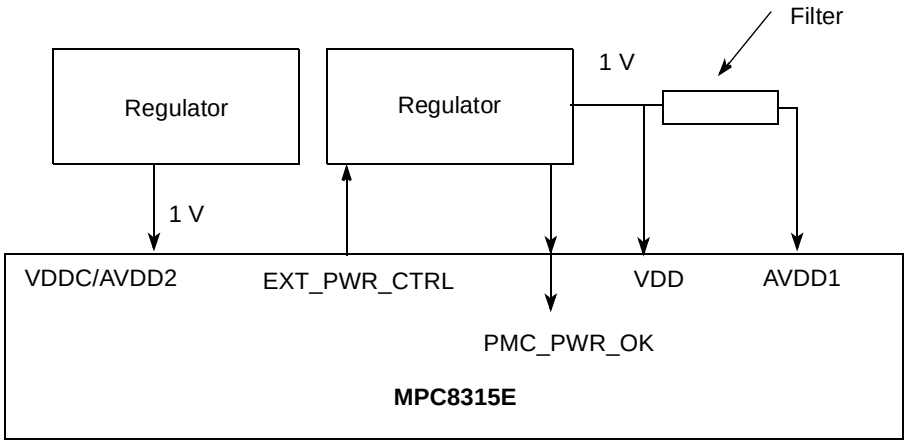


Figure 22. Switching off VDD using a Regulator

Keep the following points in mind:

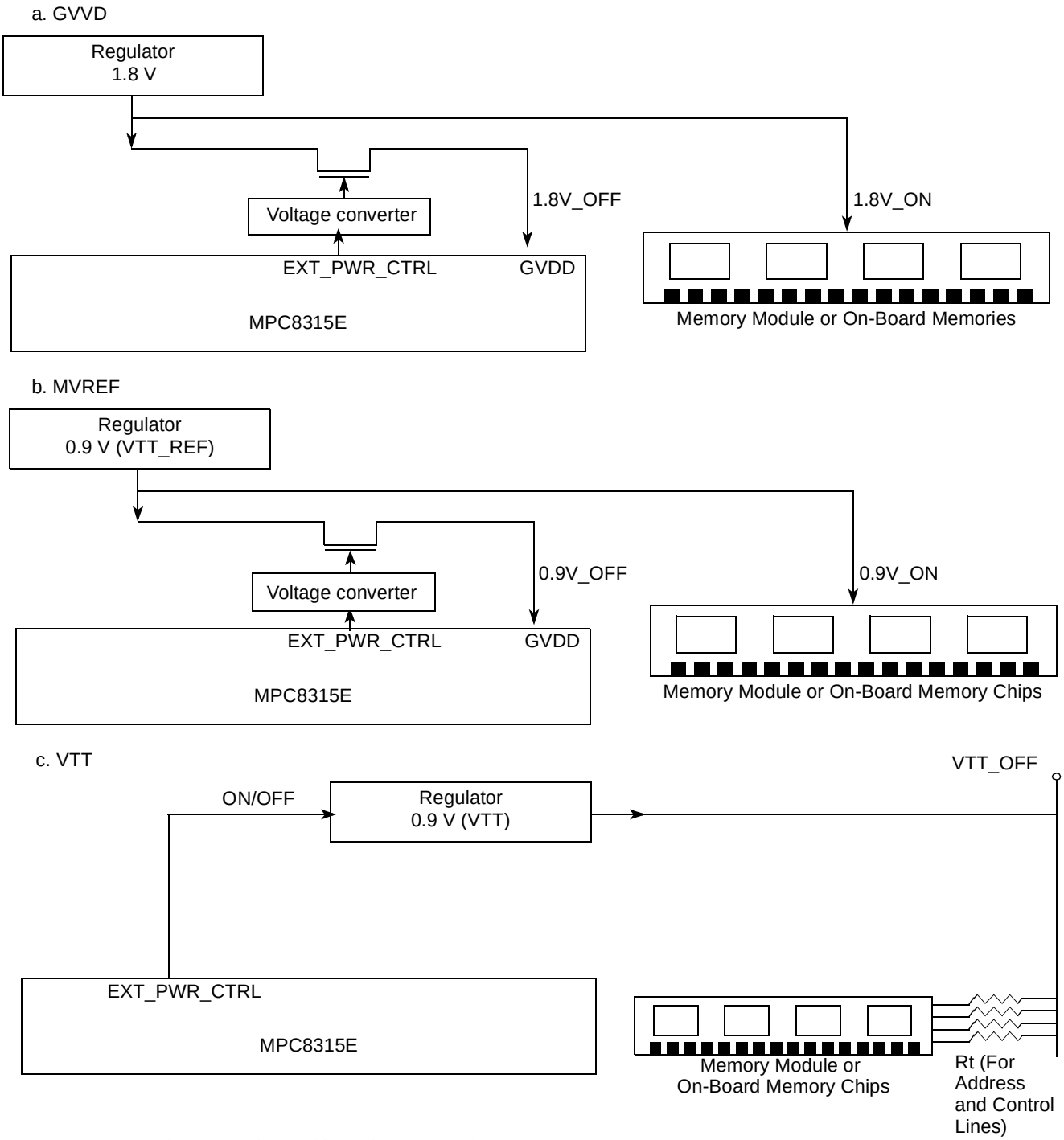
- Only core PLL (AVDD1) can be switched off. Do not switch off the power to system PLL at any time.
- Recommended devices for switchable VDD supply.
  - FET: TPC6004 from Toshiba. (Use low R_{DS} devices)

Table 26. PMC External Signals

Signal	Pin Type	Connection		Notes
		If Used	If Not Used	
$\overline{\text{QUIESCE}}$	O	As needed	Open	Status Pin
EXT_PWR_CTRL	O	As needed + 2 k–10 kΩ to NV_{DD}	Open	—
PMC_PWR_OK	I	As needed + 2 k–10 kΩ to NV_{DD}	2 k–10 kΩ to NV_{DD}	Drive this pin with the power good signal from Reset/voltage monitor circuitry.

7.16.2 Switching Off Memory Controller I/O

Figure 23 shows how to switch off the memory controller I/O.



Note: For VTT, select a regulator with ON/OFF control. EXT_PWR_CTRL can be used to switch off the regulator in power-down mode.

Figure 23. Switching OFF Memory Controller I/O

7.16.3 CKE Termination

CKE needs to remain low after the 8315 DDR I/Os are powered off. Since VTT also needs to be gated off when the 8315 I/Os are off, a pull down should be added to the CKE pin. When VTT is used, use a 100 Ω termination resistor to VTT and 100 Ω resistor to GND on CKE.

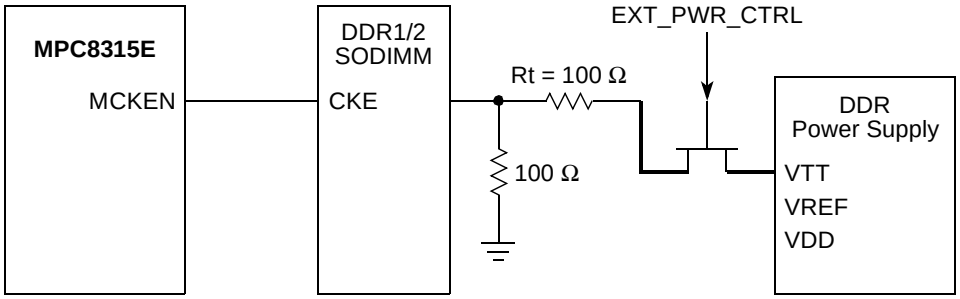


Figure 24. Low Power CKE Termination / VTT Used

When VTT termination is not used, a 1 K pull down should be added to the CKE pin to keep it in low state (when I/Os are switched off).

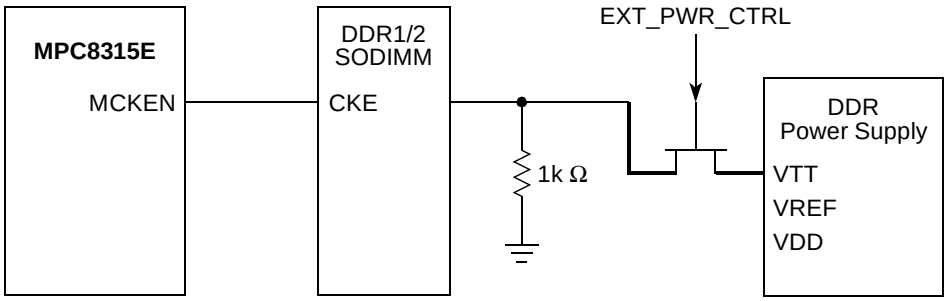


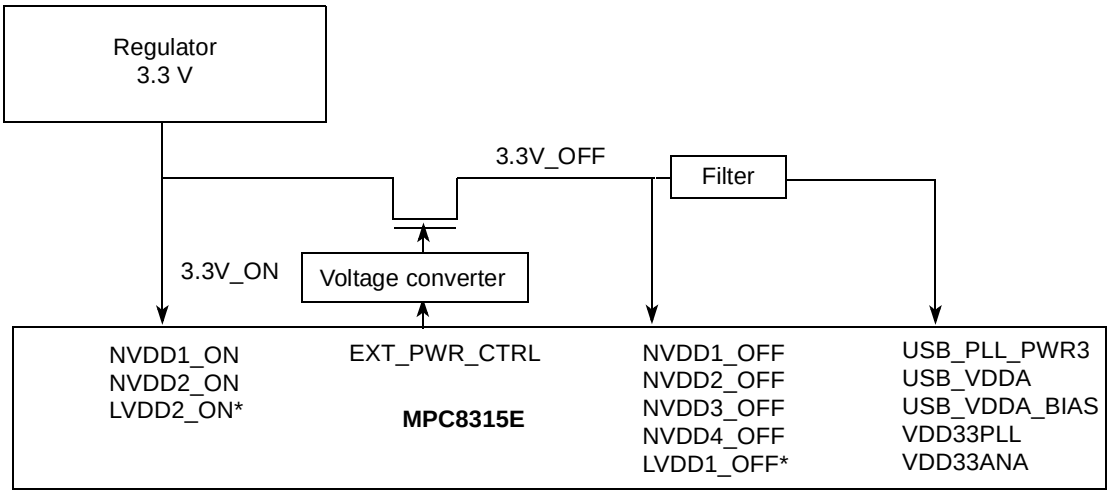
Figure 25. Low Power CKE Termination / VTT Not Used

NOTE

The above recommendation is applicable only to CKE signal and not to other DDR signals.

7.16.4 Switching Off NVDD and LVDD I/O

Figure 26 shows how to switch off NVDD and LVDD I/O.



Note: LVDD2_ON and LVDD2_OFF can also use 2.5 V. A separate switch must be used, as follows.

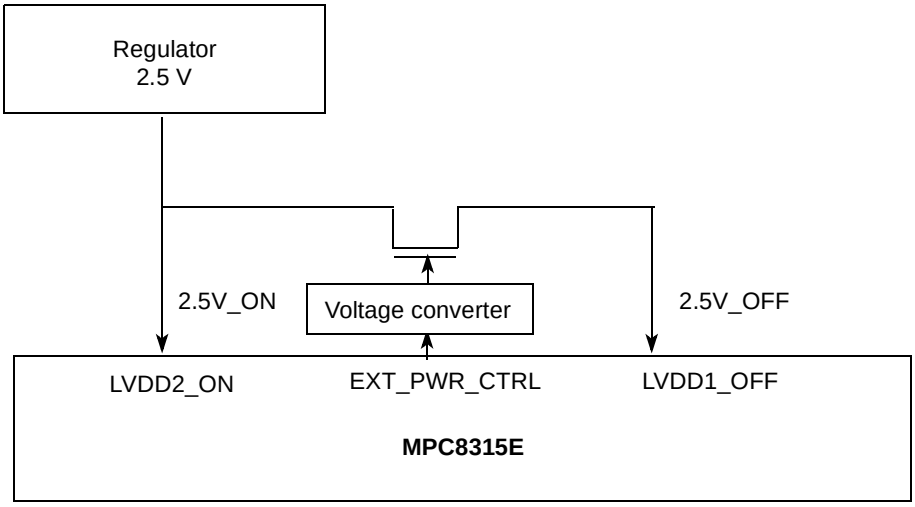


Figure 26. Switching OFF NVDD and LVDD I/O

7.16.5 I/O Switching

Figure 27 summarizes the I/O switching figures in previous sections.

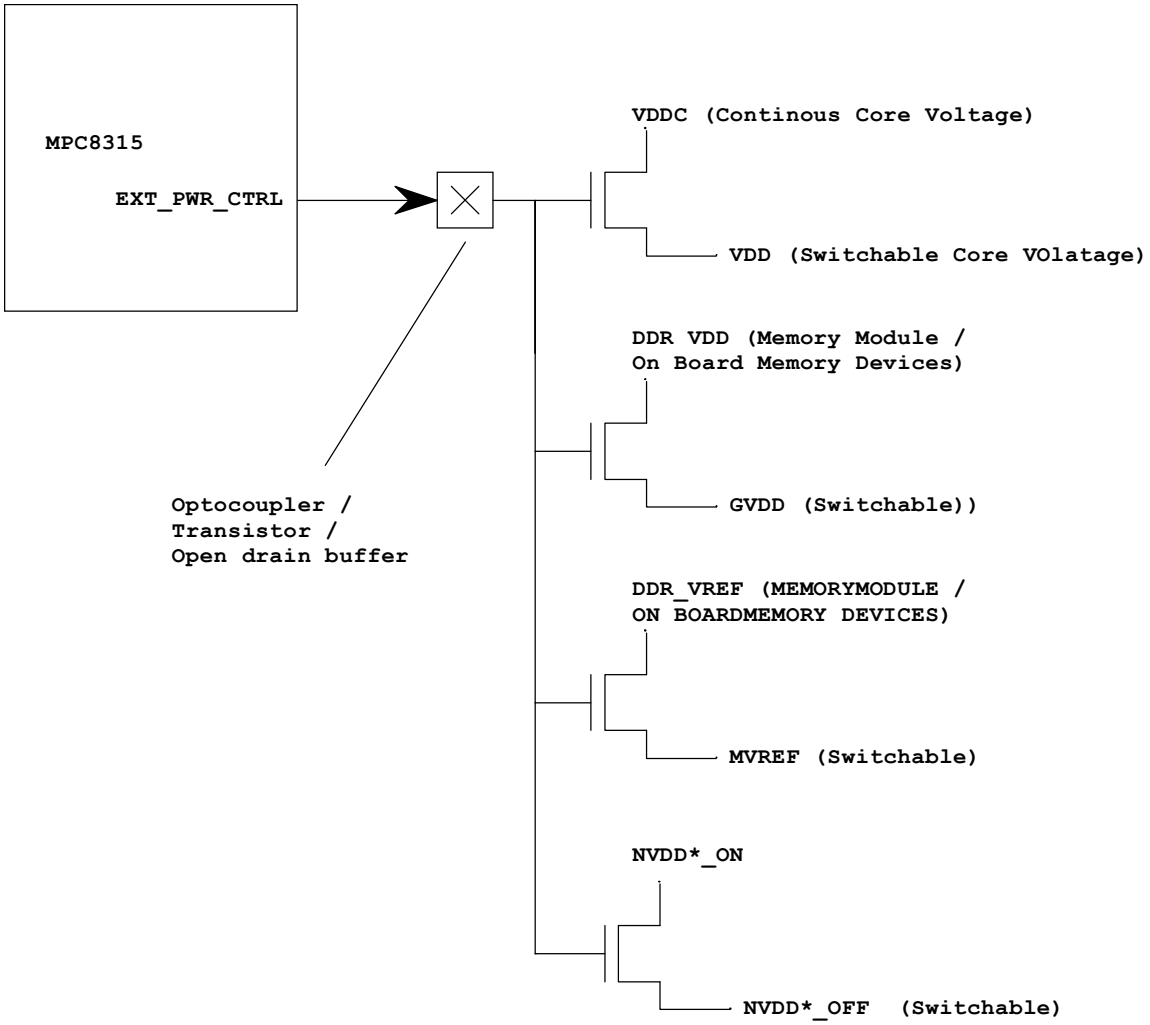


Figure 27. I/O Switching

When the I/O supplies are switched off, ensure that the peripheral connected to the switchable I/Os are not driving those I/Os. It is recommended to switch off the peripheral device along with the switchable I/O in order to avoid any damage to the devices. If the peripheral device is not switched off, please ensure that the Output pins of the peripheral device are either driven into high impedance state or to logic 0.

8 Revision History

Table 27 provides a revision history for this application note.

Table 27. Document Revision History

Rev. Number	Date	Substantive Change(s)
1	02/2012	• Updated Figure 1to match the figure in MPC8314EEC, Rev 2. • Deleted “CORE PLL(AVDD1) & SYSTEM PLL(AVDD2)” from the line “Figure 2 shows the PLL power supply filter circuit for CORE PLL(AVDD1) & SYSTEM PLL(AVDD2)” in Section 2.7, “Core PLL Power Supply Filtering”. • Changed 10 Ohm to 1 Ohm in Figure 6. • Added the following note to Table 2: All the I/Os should be interfaced with peripherals operating at same voltage levels. • Updated Figure 7 to match the figure in MPC8314EEC, Rev 2. • Replaced the following instances across the document: • all instances of SYS_CR_CLK_IN and SYS_CR_CLK_OUT with SYS_XTAL_IN and SYS_XTAL_OUT respectively. • Replaced all instances of USB_CR_CLK_IN and USB_CR_CLK_OUT with USB_XTAL_IN and USB_XTAL_OUT respectively. • In Section 4.5, “PCI Express or Ethernet Clocking”, replaced MII with RTBI in the following sentence: “When running in RGMII or MII modes (not using the SerDes) the reference clock is supplied by the GTX_CLK125 input on the eTSEC interface”. • In Table 4, changed 1.5 kOhm to 1kOhm in the second row. • In Figure 11, changed the second resistor from 10kOhm to 1kOhm. • In Table 7, changed theThermal Management details from “Tie to GND using 47K or above” to “Tie to GND using 4.7K or above”. • Made the following changes in Table 8: – In fifth column, third row, changed PCI Arbiter Control Configuration Register PM bit=1 to PCIACR[PM]=1 – In the columns corresponding to PCI_PME, changed pin type to IO and replaced “Open-drain signa” with “This pin has a weak internal pull up”. • In Table 9, changed the notes of MDQS[0:3] from “In 16 bit mode, unused MDQS pin should be grounded” to “In 16 bit mode, unused MDQS[2:3] should be grounded through 150ohm resistor”. • Made following updates toTable 11: – Added this note below the table: All local bus signals are HiZ during PORESET assertion. After PORESET de assertion, during RCW loading, the state is as shown in Reference manual "Output Signal States During Reset". – Added the note “This pin has a weak internal pull up” to the signal LGPL4/LGTA/LUPWAIT/ LFRB. • Added Table 13 from AN3362. • In Table 13, modified the note to the signal TSEC_MDIO from ‘Open drain signal’ to ‘Bidirectional signal’ • Updated the following details in Figure 19: – Replaced R381 and R319 with DNP – Replaced 200 with 200 ± 1% and 100 with 100 ± 1% • In Section 7.16.1, “Switching Off Core VDD”, removed the following bullet points: – When two regulators are used to generate VDD and VDDC individually, make sure both the voltage difference between the two are within the limits as mentioned in the Hardware specs. – Regulator:MAX1510ETB+ from Maxim • Updated TXA/RXA and TXA/RXA_b signals to “as needed” in Table 20 “if used” column. • Updated Section 2.7, “Core PLL Power Supply Filtering,” and Figure 2.
0	04/2009	• Initial public release.

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