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S12XS Family Compatibility Considerations

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1 Introduction

The S12XS family is a next generation, cost competitive MCU solution targeting existing S12 customers and emerging markets. The S12XS family features a power- and code-efficient 16-bit core, on-board data flash (D-flash), an on-board frequency-modulated PLL, and offers flexibility and compatibility with the fully featured S12XE family.

Target applications include smart junction boxes, seat controllers, HVAC, low-end engine control, body ECU, RKE receiver, door modules, and steering modules.

The S12XS is pin compatible and emulatable with the XE family. Key features of the XE-family that are not included on XS family are: XGATE coprocessor, memory protection unit, and advanced emulated EEPROM functionality. The S12XE and S12XS families give customers flexibility from 64K up to 1M flash and packages from 64 LQFP to 208 MapBGA.

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For additional information on compatibility between S12XE and S12XS families, please refer to the Freescale application note, “Using the S12XE Family as a Development Platform for the S12XS Family,” (document AN3327).

This document describes the differences and key similarities between the S12XS family members that must be considered when moving from a larger umbrella device with more memory and a larger package, to a smaller device with less memory and a smaller package.

The topics discussed are:

- Memory mapping and paging
- Peripherals
- Port integration module
- Part IDs

2 Overview of S12XS Family

This document is meant to be used in conjunction with the S12XS family data sheet located at http://freescale.com. Table 1 gives an overview of the parts, available peripherals, and package options for each of the family members.

Table 1. Family Features

Device	Package	XGATE	CAN	SPI	SCI	TIM	PIT	A/D	PWM	I/0
S12XS256	112 LQFP	Not Available	1	1	2	8ch	4ch	1/16	8ch	91
	80 QFP		1	1	2	8ch	4ch	1/8	8ch	59
	64 LQFP		1	1	2	8ch	4ch	1/8	8ch	44
S12XS128	112 LQFP		1	1	2	8ch	4ch	1/16	8ch	91
	80 QFP		1	1	2	8ch	4ch	1/8	8ch	59
	64 LQFP		1	1	2	8ch	4ch	1/8	8ch	44
S12XS64	112 LQFP		1	1	2	8ch	4ch	1/16	8ch	91
	80 QFP		1	1	2	8ch	4ch	1/8	8ch	59
	64 LQFP		1	1	2	8ch	4ch	1/8	8ch	44

3 Memory

Table 2 gives an overview of the memory sizes available for the S12XS family. Local and global memory maps are compatible across the family. Out of reset, the family has equivalent maps and default values in the memory map control (MMC) registers. For devices with smaller amounts of memory, those areas unimplemented in the map will cause a reset if accessed.

Table 2. Memory Sizes by Device

Device	Flash	ROM	RAM	Data Flash
9S12XS256	256K	—	12K	8K
9S12XS128	128K	—	8K	8K
9S12XS64	64K	—	4K	4K
3S12XS256	—	256K	12K	—
3S12XS128	—	128K	8K	—
3S12XS64	—	64K	4K	—

3.1 P-Flash (Program Flash)

The P-flash memory constitutes the main nonvolatile memory for applications. The P-Flash memory is compatible for all flash devices in the S12XS family for all memory sizes in terms of functionality for program, erase, security, and protection setup. All family members have a single physical flash block that is equivalent to the defined flash size. Table 3 shows the physical flash block sizes in correlation to the global address.

Table 3. Physical P-Flash Blocks

<table>
<tr><th>Global Address</th><th>S12XS256</th><th>S12XS128</th><th>S12XS64</th></tr>
<tr><td>0x7C_0000</td><td rowspan="9">256 KB Flash Block</td><td rowspan="3">Unimplemented</td><td rowspan="3">Unimplemented</td></tr>
<tr><td></td></tr>
<tr><td>0x7D_FFFF</td></tr>
<tr><td>0x7E_0000</td><td rowspan="6">128 KB Flash Block</td><td rowspan="3">Reserved</td></tr>
<tr><td></td></tr>
<tr><td>0x7E_FFFF</td></tr>
<tr><td>0x7F_0000</td><td rowspan="3">64 KB Flash Block[1]</td></tr>
<tr><td></td></tr>
<tr><td>0x7F_FFFF</td></tr>
</table>

1 The 9S12XS64 uses the 9S12XS128 die tested only for 9S12XS64 functionality. Accessing flash between address 0x7E_0000 through 0x7E_FFFF does not cause an access error reset of device on a S12XS64 device with part ID $C1C0. The PartID register should be verified for the actual device.

For all flash devices, programming and erase operations will be equivalent. Programming is done in phrases, or four word increments. Erase operations can be done in sectors or blocks. Simultaneous read while write and read while erase from P-flash is not available because there is only one physical block implemented on the 9S12XS family devices.

Protection is compatible for all memory sizes of the S12XS family where implemented areas are equivalent.

Security is equivalent for all S12XS family devices. The options/security byte is located at global address 0x7F_FF0F.

PPAGEs for local memory maps are compatible across all family members where implemented areas are equivalent. Global memory map maps from higher order address down to a lower order address. Accessing unimplemented P-Flash space will cause an access error. An access error will cause the part to reset.

3.2 D-Flash (Data Flash)

D-Flash will be compatible for all 9S12XS family flash devices where implemented areas are equivalent. 9S12XS256 and 9S12XS128 have an equivalent implemented amount of 8K. ROM devices do not implement data flash. The global memory map maps from a lower order address to a higher order address.

Table 4. Data Flash

<table>
<tr><th>EPAGE</th><th>Global address</th><th>9S12XS256
9S12X128</th><th>9S12XS64</th></tr>
<tr><td rowspan="2">0x00</td><td>0x10_0000</td><td rowspan="16">8 KB</td><td rowspan="8">4 KB</td></tr>
<tr><td>0x10_3FFF</td></tr>
<tr><td rowspan="2">0x01</td><td>0x10_0400</td></tr>
<tr><td>0x10_7FF</td></tr>
<tr><td rowspan="2">0x02</td><td>0x10_0800</td></tr>
<tr><td>0x10_0BFF</td></tr>
<tr><td rowspan="2">0x03</td><td>0x10_0C00</td></tr>
<tr><td>0x10_0FFF</td></tr>
<tr><td rowspan="2">0x04</td><td>0x10_1000</td><td rowspan="8"></td></tr>
<tr><td>0x10_13FF</td></tr>
<tr><td rowspan="2">0x05</td><td>0x10_1400</td></tr>
<tr><td>0x10_17FF</td></tr>
<tr><td rowspan="2">0x06</td><td>0x10_1800</td></tr>
<tr><td>0X10_1BFF</td></tr>
<tr><td rowspan="2">0x07</td><td>0x10_1C00</td></tr>
<tr><td>0x10_1FFF</td></tr>
</table>

The D-flash can be accessed on the local memory map through the 1K DFLASH window through control of the EPAGE register. The EPAGE register has a default value of 0xFE out of reset. EPAGE 0xFE is unimplemented space on the S12XS family. Therefore, when accessing the D-Flash through the 1K D-Flash window, the EPAGE register must be written to with a valid EPAGE. Accessing unimplemented D-Flash space causes an access error. An access error causes the part to reset. Table 4 shows the valid EPAGEs and corresponding global addresses.

3.3 RAM

RAM is compatible for all S12XS family devices where implemented areas are equivalent. Memory maps map from a higher-order address to lower-order address.

The RPAGE register allows the user to page 4 KB blocks into the RAM page window on the local memory map from address 0x1000 to 0x1FFF. The RPAGE default register value is 0xFD out of reset for all S12XS devices. Also, for all S12XS devices, addresses 0x2000 to 0x3FFF on the local memory map are fixed RAM pages for RPAGEs 0xFE and 0xFF. For the S12XS256, the default value of 0xFD allows for a linear address map to be accessible on the local map between addresses 0x1000 to 0x3FFF. For the S12XS128 and S12XS64 devices, RPAGE 0xFD is unimplemented space, and fixed page 0xFE (0x2000–3FFF) on the S12XS64 is unimplemented space. Accessing unimplemented space will cause an access error and the device to reset. For the S12XS128 and S12XS64, RPAGEs can be accessed through either the fixed RAM space or a valid RPAGE. Table 5 shows the location of RAM out of reset for the XS family.

Table 5. RAM Global and Local Addresses

<table>
<tr><th>Global Address</th><th>Local Address</th><th>RPAGE</th><th>S12XS256</th><th>S12XS128</th><th>S12XS64</th></tr>
<tr><td>0x0F_D000</td><td>0x1000</td><td rowspan="2">0xFD</td><td rowspan="6">12K</td><td rowspan="2">unimplemented</td><td rowspan="4">unimplemented</td></tr>
<tr><td>0x0F_DFFF</td><td>0x1FFF</td></tr>
<tr><td>0x0F_E000</td><td>0x2000</td><td rowspan="2">0xFE[1]</td><td rowspan="4">8K</td></tr>
<tr><td>0x0F_EFFF</td><td>0x2FFF</td></tr>
<tr><td>0x0F_F000</td><td>0x3000</td><td rowspan="2">0xFF[1]</td><td rowspan="2">4K</td></tr>
<tr><td>0x0F_FFFF</td><td>0x3FFF</td></tr>
</table>

[1] Accessible through RPAGE window (0x1000 to 0x1FFF) by writing a valid RPAGE value to the RPAGE register.

4 Peripherals

All peripherals are functionally compatible across the S12XS family. To maintain compatibility when developing on a larger memory and/or package option to move to a smaller device, pay careful attention to the pin-out and port routing options. A conclusive summary of the pin-outs for all three package options is available in the S12XS family can be found in the product preview, MC9S12XS256PB located at http://freescale.com. Refer to table 6 for a complete summary of port routing options.

The timer (TIM) module has eight channels available for all three package options. Channels IOC0, IOC1, and ICO2 have port-routing options (see Table 6). For the 80 QFP and 64 LQFP, if all eight PWM channels are used, then TIM channels IOC5 and IOC7 are not available simultaneously.

The 112 LQFP has 16 ATD channels available, and all other package options have eight channels. To maintain compatibility when moving to smaller package options, use ATD channels 0–7 only.

The pulse-width modulator (PWM) has eight channels available for all three package options. Channels PWM 4–7 have port routing options (see Table 6). PWM4 and PWM6 channels are available only on the 80 QFP and 64 LQFP if the port routing option is used to route to PT4 and PT6. Therefore, if all eight PWM channels are used, then TIM channels IOC5 and IOC7 are not available simultaneously for the 80 QFP and 64 LQFP.

The S12XS family has two Serial Communication Interface (SCI) modules, SCI0 and SCI1 for all three package options. SCI1 has additional port routing options available. Refer to table 6 for port routing options.

The Serial Peripheral Interface (SPI) has an additional port routing option (see Table 6).

5 Port Integration Module (PIM)

The pin functions and priorities for all S12XS devices are the same after reset or a power-on reset (POR). Port routing options for PWM channels 4–7 and TIM channels 2–0 are controlled by the Port T Routing register (PTTRR). Likewise, port routing options for SCI1 and SPI0 are controlled by the Module Routing register (MODRR). Table 6 shows the port routing options.

Table 6. Peripheral Port Routing Options[1]

	SCI1	SPI0	PWM	TIM
PM[1:0]	o			
PM[5:2]		o		
PP[2,0]	o			
PP[2:0]				o
PP[7:4]			x	
PS[3:2]	x			
PS[7:4]		x		
PT[2,0]				x
PT[7:4]			o	

[1] x denotes reset condition, o denotes possible rerouting under software control.

6 Part IDs

For the 9S12XS family, the part ID is located in two 8-bit registers: PARTIDH and PARTIDL (addresses 0x001A and 0x001B). The read-only value is a unique part ID for each device revision. Table 7 shows the assigned part ID number and mask-set number for each device.

Table 7. Part IDs

Device	Mask Set Number	Part ID
MC9S12XS256	0M05M	$C0C0
MC9S12XS128	0M04M	$C1C0
MC9S12XS64	0M04M[1]	$C1C0
	TBD	$C2C0

[1] The 9S12XS64 uses the 9S12XS128 die tested for 9S12XS64 functionality only. An actual 9S12XS64 device may be done at a later time. A product change notification will be posted in such an event. The PartID register should be verified for actual device.

7 Summary

The key differences between the devices in the S12XS family are memory mapping. Although many of the peripherals are compatible, you should focus on the default pin/port-routing aspects of the specific peripherals to enable maximum scalability with anticipated future system needs. Part IDs are specific to each device. The S12XS64 device is a special case; any errata differences should be verified and associated to the corresponding part ID.

This document is meant to be used with:

- MC9S12XS Family Reference Manual
- MC9S12XS Family Product Brief (document MC9S12XS256PB)
- S12XCPUV2 Reference Manual (document S12XCPUV2)

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