Freescale Semiconductor
Application Note

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Enhanced Serial Interface Mapping

16 E1/T1 QUICC Engine™ Solution for TDM Connectivity

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Wireless infrastructure equipment manufacturers must balance deployment costs while fulfilling demands for next generation network services. Enhanced services usually mandate increased network connection rates. Typically the physical connection from the wireless base station to the RNC is via multiple bonded E1 or T1 interfaces. A cost effective method that enhances the services' capabilities on the network is deploying additional E1 or T1 lines between the base station and the RNC. One such example is to increase the number of connections from 8 to 16 E1s. Indeed the sweet spot for equipment manufacturers is 16 E1s running bonding protocols, such as inverse multiplexing for ATM or multilink point-to-point protocol.

This application note explains how the QUICC Engine™ multichannel controller (MCC) and serial interface (SI) of the MPC8360E and MPC8568E can be configured to control 16 E1 or T1 interfaces. It is applicable for any equipment requiring up to 16 E1 or T1 interfaces with an IMA, MLPPP, or a clear channel connection scheme. It is also relevant regardless of the end product for that equipment.

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NOTE

This document mainly focuses on the E1 interface because an E1 has a higher clock rate and more 8-bit timeslots per frame. An E1 has 32 timeslots of 8 bits versus 24 for a T1. Hence, whatever is stated for an E1 interface is also true for a T1.

1 QUICC Engine Block Connection Requirements

To connect 16 E1s to the QUICC Engine block, more than 1 E1 must be multiplexed onto a QUICC Engine TDM. Figure 1 provides an example, from a hardware perspective, that realizes 16 E1 connectivity on 2 QUICC Engine TDM interfaces. It shows 16 E1s being multiplexed and frame interleaved on 2 QUICC Engine TDMs. External logic (framer) must have the capability of multiplexing more than 1 E1 on a TDM.

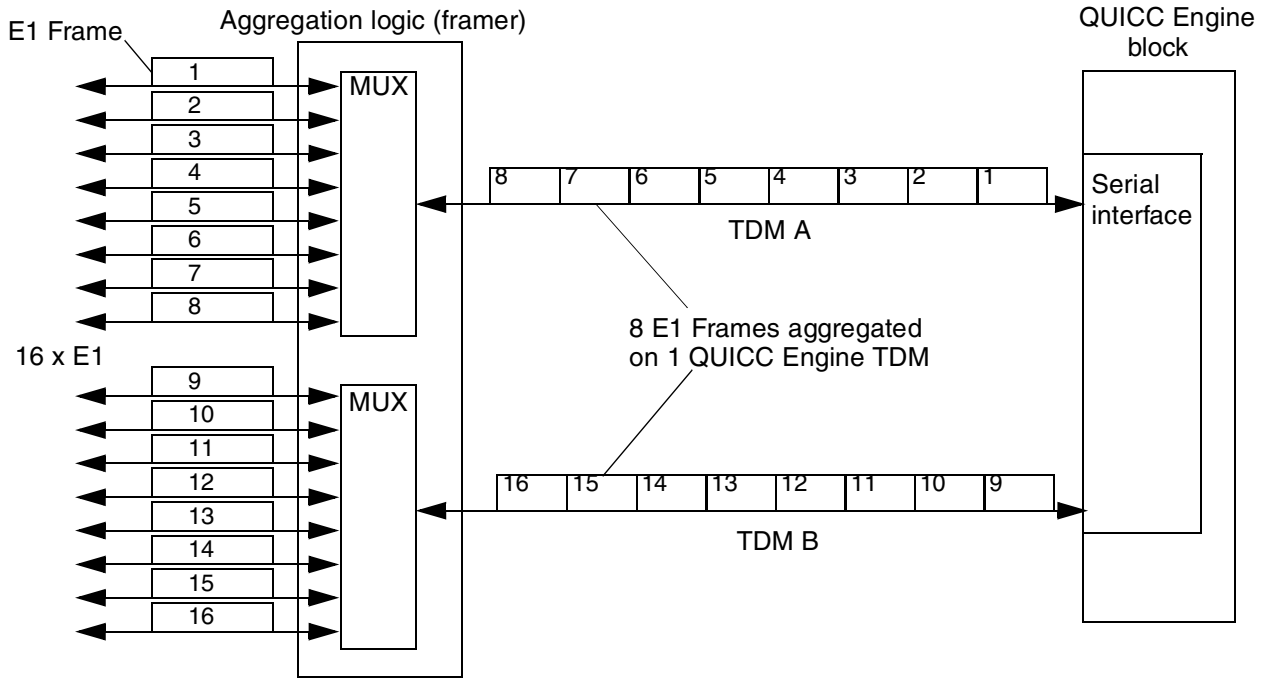

Figure 1. Sixteen E1s Multiplexed on 2 TDMs Example

The TDM clock rate must be N times the nominal E1 clock rate, where N is the number of E1s aggregated on any given TDM. Table 1 details the clock rate options for connection scenarios that realize the 16 E1 requirement.

Table 1. TDM Clock Rate for 16 E1s vs. Number of TDMs

Number of TDMs	Clock Rate Per TDM	Number of E1s on TDM
2	8x2048kHz	8
4	4x2048kHz	4
8	2x2048kHz	2

The maximum number of E1s that can be placed on 1 TDM connected to the QUICC Engine module is 8. For each of the options detailed in Table 1 the SYNC is 125µs, for example, the same rate as an E1 with 32x8-bit timeslots.

2 MCC Configuration Rules

For applications that require more E1 lines than the number of QUICC Engine TDMs, the data format on the E1 (channelized or otherwise) determines whether this is possible. To increase the QUICC Engine E1 capacity beyond the 8 E1s per 256 channel MCC, adhere to the following:

- The maximum number of E1s supported by a 256 channel MCC is 16.
- It is impossible to support 16 E1s with a configuration of 32 independent 8-bit time slots on each E1 (for example, channelized by byte timeslots).
- For N E1 links aggregated on 1 TDM, the external framer or logic must have the capability of supplying a clock at rate of N times the nominal E1 rate to the QUICC Engine TDM link(s). Note that N must be even.
- More than 1 E1 must be multiplexed onto 1 physical TDM link.
- For 16 E1s the TDM link must be clocked at a rate cognizant of Table 1, thereby increasing the number of 8-bit timeslots (64kbps) per TDM.
- The 16-bit super channel mode must be applied to as many MCC channels as possible.
- An E1 must not consume more than 16 MCC channels Transmit FIFOs.

2.1 MCC Transmitter

The MCC transmitter supports 256 logical channels for channelized TDM frame termination. Because an E1 interface has a clock rate of 2048000Hz and a frame rate of 125µs, each frame contains 32 8-bit time slots. If the data format on the E1 is channelized—each channel consuming 1 byte per E1 frame—then an MCC can support 8 E1s (8 E1s × 32 timeslots per E1 = 256 MCC channels).

The following sections show how the 256 MCC channels can be used to map 16 E1s (512 × 1-byte timeslots).

2.1.1 Interleaving Requirements for 16-bit Super Channel Mode

The key to supporting 16 E1s on the MCC is the 16-bit super channel mode. This mode allows the user to describe an E1 using 16 MCC channels (TDM data format dependent). Because the MCC supports 256 channels, the 16-bit super channel mode allows the QUICC Engine module to support 16 E1s per MCC. This is because the SI RAM can now source 2 bytes from 1 MCC channel FIFO in only 1 SI RAM entry. Consequently, the aggregation logic in Figure 1 must be capable of handling an interleaving scheme where at least 2 consecutive 8-bit timeslots from an E1 are present on a TDM; in other words, the interleaving scheme must be 2 bytes or greater amongst the E1 frames aggregated on 1 TDM. Furthermore, the interleaving scheme must be based on an even number of bytes from the TDM passed round robin to each E1. The most likely solution is to use frame based interleaving because a number of ‘off the shelf’ framers support this functionality.

2.1.2 Why Does Byte Interleaving Not Allow 16 E1s

Figure 2 shows a byte interleaving of 2 E1s on 1 QUICC Engine TDM. The timeslots on the TDM that correspond to the E1 frame on E1_A are numbered 1–32. The timeslots on the TDM that correspond to the E1 frame on E1_B are numbered 33–64. It is assumed that E1_A and E1_B are both clear channel (there is no channelization). All timeslots on E1_A carry data sourced from 1 queue, essentially 1 MCC channels buffer descriptor ring; all timeslots on E1_B carry data sourced from a different queue than E1_A.

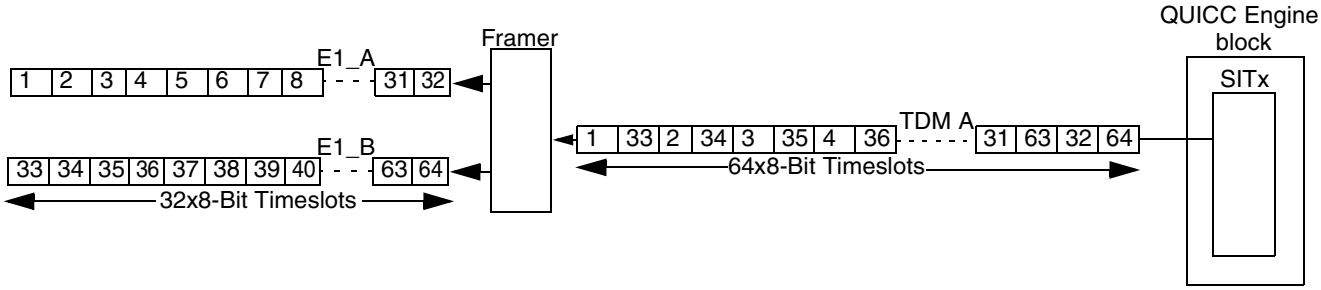

Figure 2. Byte Interleaving 2 E1s on 1 QUICC Engine TDM

Use super channeling to map the E1 frame in the QUICC Engine Transmit SI RAM. Figure 3 shows one example of SI RAM and MCC super channel table initialization, which corresponds to TDM A configuration in Figure 2.

Transmit SI RAM

0	1	2	3–10	11–13	14	15
MCC	LOOP	SUPER	MCSEL	CNT	BYT	LST
SI RAM Address						
1	0	1	0x0	0x0 [1]	1	0
1	0	1	0x1	0x0[1]	1	0
1	0	1	0x2	0x7 [2]	0	0
1	0	1	0x3	0x7[2]	0	0
1	0	1	0x4	0x7[2]	0	0
1	0	1	0x5	0x7[2]	0	0
1	0	1	0x6	0x7[2]	0	0
1	0	1	0x7	0x7[2]	0	0
...						
1	0	1	0x3C	0x7[2]	0	0
1	0	1	0x3D	0x7[2]	0	0
1	0	1	0x3E	0x7[2]	0	0
1	0	1	0x3F	0x7[2]	0	1

Super Channel Table

	0–1	2–9	10–15
		CHANNEL NO	
	MURAM_Base + SCTPBASE +		
0x0		—	
0x2		—	
0x4		0x0	
0x6		0x1	
0x8		0x0	
0xA		0x1	
0xC		0x0	
0xE		0x1	
		...	
0x78		0x0	
0x7A		0x1	
0x7C		0x0	
0x7E		0x1	

1 First byte of super channel 1-byte configuration

2 Regular (not first) byte of super channel 1-byte configuration

Figure 3. Byte Interleaved SI RAM and MCC Super Channel Initialization

Because the data format on the TDM is 2 clear channel streams of 32 1-byte timeslots, it requires 2 MCC super channels. Because the data is byte interleaved on the TDM, the SI RAM must be configured for timeslots of size 1 byte; all entries in the SI RAM must be programmed for 1 byte and super channel. Byte interleaving does not allow the use of 16-bit super channel mode because the TDM uses a scheme of sourcing 1 byte from each MCC super channel round robin, for example, channel 0, channel 1, channel 0, channel 1, continuing in this fashion.

Note that each entry in the SI RAM has a unique MCSEL value, thus each entry consumes 1 MCC channels Transmit FIFO. 64 MCC channels are consumed because there are 64 entries in the SI RAM. Therefore 32 MCC channels are required for each E1 resulting in maximum of 8 E1s for a byte interleaved E1 aggregation scheme.

Also this configuration will require that the MCCF is programmed to provide 64 channels to TDM A. The corresponding SIxMR must be programmed such that 64 SI RAM entries are provided to TDM A in the SI RAM.

NOTE

Figure 2 uses MCC channel 0 for E1_A and MCC channel 1 for E1_B. The channel specific parameters (CSP) for the super channel that provides data for E1_A are at MCC channel 0 offset in MURAM; for E1_B the CSP are at MCC channel 1 offset. This is only to clarify the example; it is permissible to use another MCC channels CSP in the first timeslot for each super channel. This may be necessary depending on the protocol for the MCC channel. For example, MLPPP and Serial ATM channels require 256 bytes of CSP, and as such MCC channel 1 cannot be used to hold the CSP for E1_B due to CSP overlap caused by MCC channel 0. It is easily avoided by choosing MCC channels that do not overlap when taking into account the protocol-dependent CSP configuration.

2.1.3 Interleaving Based on 2 Bytes

Figure 4 shows an alternative interleaving on the TDM with the same configuration of timeslots on E1_A and E1_B of Figure 2. This time the TDM is interleaved 2 bytes round robin.

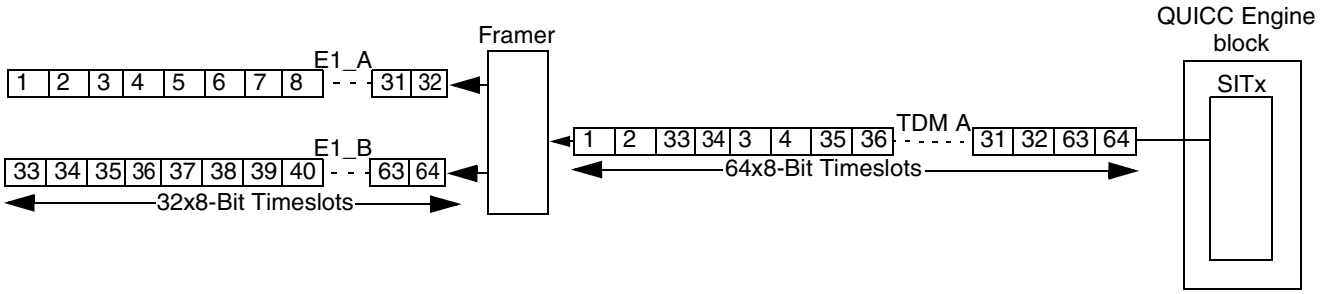

Figure 4. Interleaving 2 E1s on 1 QUICC Engine TDM 2 Bytes Round Robin

Use super channeling to map the E1 frame in the QUICC Engine Transmit SI RAM because each E1 is a clear channel. Figure 5 shows one example of SI RAM and MCC super channel table initialization that corresponds to TDM A configuration in Figure 4.

Transmit SI RAM

0	1	2	3–10	11–13	14	15
MCC	LOOP	SUPER	MCSEL	CNT	BYT	LST
SI RAM Address						
1	0	1	0x0	0x1 [1]	1	0
1	0	1	0x1	0x1[1]	1	0
1	0	1	0x2	0x1 [2]	0	0
1	0	1	0x3	0x1[2]	0	0
1	0	1	0x4	0x1[2]	0	0
1	0	1	0x5	0x1[2]	0	0
1	0	1	0x6	0x1[2]	0	0
1	0	1	0x7	0x1[2]	0	0
...						
1	0	1	0x1E	0x1[2]	0	0
1	0	1	0x1F	0x1[2]	0	1

Super Channel Table

	0–1	2–9	10–15
		CHANNEL NO	
		MURAM_Base + SCTPBASE +	
0x0		—	
0x2		—	
0x4		0x0	
0x6		0x1	
0x8		0x0	
0xA		0x1	
0xC		0x0	
0xE		0x1	
		...	
0x3C		0x0	
0x3E		0x1	

1 First 2 bytes of super channel

2 Regular (not first) 2 bytes of super channel

Figure 5. 2 Byte Interleaved SI RAM and MCC Super Channel Initialization

The 16-bit super channel mode is used because the data on the TDM is interleaved every 2 bytes; 1 SI RAM entry describes 2 bytes on the TDM. 2 bytes are extracted from an MCC Transmit channels FIFO that corresponds to the current SI RAM entry's MCSEL field. Each SI RAM entry fills 2 bytes of the TDM frame. The benefits are twofold:

1. TDM A in Figure 4 requires 32 MCC channels to describe the 2 E1s. MCCF should be programmed for 32 channels assigned to TDM A.
2. The number of SI RAM entries and super channel entries is halved versus Figure 3.

This interleaving scheme will allow the QUICC Engine block to support 16 E1s.

2.1.4 Frame Interleaving

Figure 6 shows another alternative interleaving scheme on the TDM with the same configuration of timeslots on E1_A and E1_B in Figure 2, but the TDM is frame interleaved.

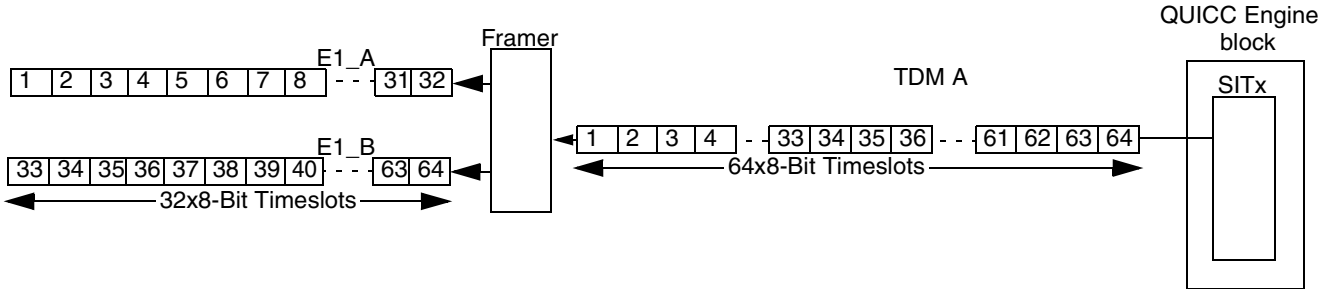

Figure 6. Interleaving 2 E1s on 1 QUICC Engine TDM 32 Bytes Round Robin

Use super channeling to map the E1 frame in the QUICC Engine Transmit SI RAM because each E1 is a clear channel. Figure 7 shows one example of SI RAM and MCC super channel table initialization that corresponds to TMDATMDA configuration in Figure 6.

Transmit SI RAM

0	1	2	3–10	11–13	14	15
MCC	LOOP	SUPER	MCSEL	CNT	BYT	LST
SI RAM Address						
1	0	1	0x0	0x1 [1]	1	0
1	0	1	0x2	0x1 [2]	0	0
1	0	1	0x3	0x1[2]	0	0
1	0	1	0x4	0x1[2]	0	0
Each subsequent entry incrementing MCSEL by 1 until:						
1	0	1	0x10	0x1[2]	0	0
1	0	1	0x1	0x1[1]	1	0
1	0	1	0x11	0x1[2]	0	0
1	0	1	0x12	0x1[2]	0	0
Each subsequent entry incrementing MCSEL by 1 until:						
1	0	1	0x1E	0x1[2]	0	0
1	0	1	0x1F	0x1[2]	0	1

Super Channel Table

	0–1	2–9	10–15
		CHANNEL NO	
	MURAM_Base + SCTPBASE +		
0x0		—	
0x2		—	
0x4		0x0	
0x6		0x0	
	0x0 until:		
0x20		0x0	
0x22		0x1	
0x24		0x1	
	0x1 until:		
0x3C		0x1	
0x3E		0x1	

1 First 2 bytes of super channel

2 Regular (not first) 2 bytes of super channel

.

Figure 7. Frame Interleaved SI RAM and MCC Super Channel Initialization

Frame interleaving also allows the QUICC Engine block to support 16 E1s. Note that the SI RAM entry with MCSEL = 1 is no longer the second entry in the table; the entry with MCSEL = 1 corresponds to the first timeslot for E1_B. This ensures that the super channel for E1_B uses the CSP offset for MCC channel 1, which guarantees the same MCC CSP configuration as the example in Section 2.1.3, “Interleaving Based on 2 Bytes”. The MCC channels FIFOs used for E1_A are 0 (CSPs reside at this channel’s offset in MURAM), 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16; the MCC channels FIFOs used for E1_B are 1 (CSPs reside at this channels offset in MURAM), 17, 18, 19, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 30, and 31.

Only the root channel programming is significant in the SI RAM. The root channel is the MCC channel where the CSP reside. The super channel for E1_A could also be configured as follows:

- MCC channel 0 as the root (entry with first programming in SI RAM)
- An arbitrary assignment of another 15 MCC channels excluding channel 1

MCC channel 1 is excluded because it is the root channel where the CSPs reside for E1_B. It would use the remaining 15 MCC channels assigned to this TDM A via MCCF in no specific order. The user can decide under which MCC channel offset the CSPs reside.

2.2 MCC Receiver

Supporting 16 E1s on the receiver is simpler than with the transmitter. The receiver does not need any super channel programming. To support the frame interleaved configuration of the TDM shown in Figure 6, Table 2 details the SI RAM programming. It is assumed that the CSPs for E1_A are at MCC channel 0 offset; for E1_B the CSPs are the offset for MCC channel 1 in the MURAM.

Only 2 MCC channels are required (1 for each E1 stream).

Table 2. Frame Interleaving of 2 E1s on 1 TDM SI RAM Configuration for Receiver

0	1	2	3–10	11–13	14	15
MCC	LOOP	SUPER	MCSEL	CNT	BYT	LST
16 entries of:						
1	0	0	0x0	0x1	1	0
15 entries of:						
1	0	0	0x1	0x1	1	0
1 entry of:						
1	0	0	0x1	0x1	1	1

3 ATM Cell Mapping

The ATM Forum specification af-phy-0064.000 and the ITU-T G.804 specification define a TDM frame format for carrying 53 byte ATM cells over an E1 interface. This frame format is shown in Figure 8.

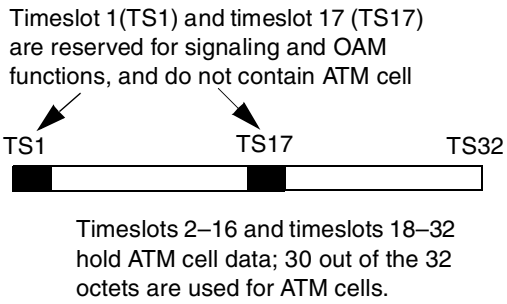

Figure 8. ATM Cell E1 TDM Frame Format

Assuming a frame based interleaving scheme with 2 E1s on 1 TDM, the TDM would be constructed as shown in Figure 9.

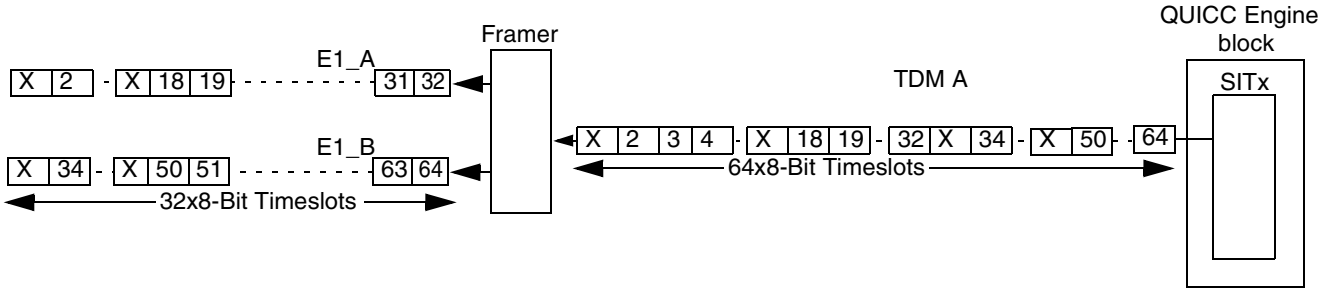

Figure 9. Interleaving 2 E1s on 1 QUICC Engine TDM 32 Bytes Round Robin for ATM Cells

The TDM contains 2 ATM cell streams, each stream sourced from a dedicated TC layer. The timeslots marked ‘X’ are the control and signaling slots shown in Figure 8 (timeslot 1 and timeslot 17). E1_A contains TDM A timeslots 1–32 where timeslot 1 and timeslot 17 are typically not sourced from any QUICC Engine peripheral (MCC nor UCC), and these slots in the SI RAM are programmed for no peripheral. The ATM cell data is in timeslots 2–16 and timeslots 18–32.

Similarly E1_B comprises timeslot 33 (not sourced from the SI), timeslots 34–48 (ATM cell data), timeslot 49 (not sourced from the SI), and timeslots 50–64 (ATM cell data).

This TDM configuration presents one issue, namely the slots that contain the ATM cell data are in banks of 15 octets and it is impossible to describe the TDM using only the 16-bit super channel mode. Therefore in order to map this TDM in the SI RAM a mix of 8- and 16-bit super channels must be used. In order to ensure that 16 E1s can be supported the mix must not consume more than 16 MCC channels per E1. This can be achieved as follows:

- Timeslots 2–15 sourced from 7 MCC channels in 16-bit super channel mode
- Timeslot 16 sourced from 1 MCC channel in 8-bit super channel mode
- Timeslots 18–31 sourced from 7 MCC channels in 16-bit super channel mode
- Timeslot 32 sourced from 1 MCC channel in 8-bit super channel mode

E1_A can be constructed using 16 MCC channels, 14 channels in 16-bit super channel mode and 2 channels in 8-bit super channel mode. This constitutes the 30 octets on the TDM that contain ATM cell data for E1_A.

E1_B uses an identical configuration scheme (in terms of MCC channel usage) as E1_A, and it too implements 16 MCC channels. This scheme meets the requirement for 16 E1 connectivity. Figure 10 shows the SI RAM and super channel table initialization.

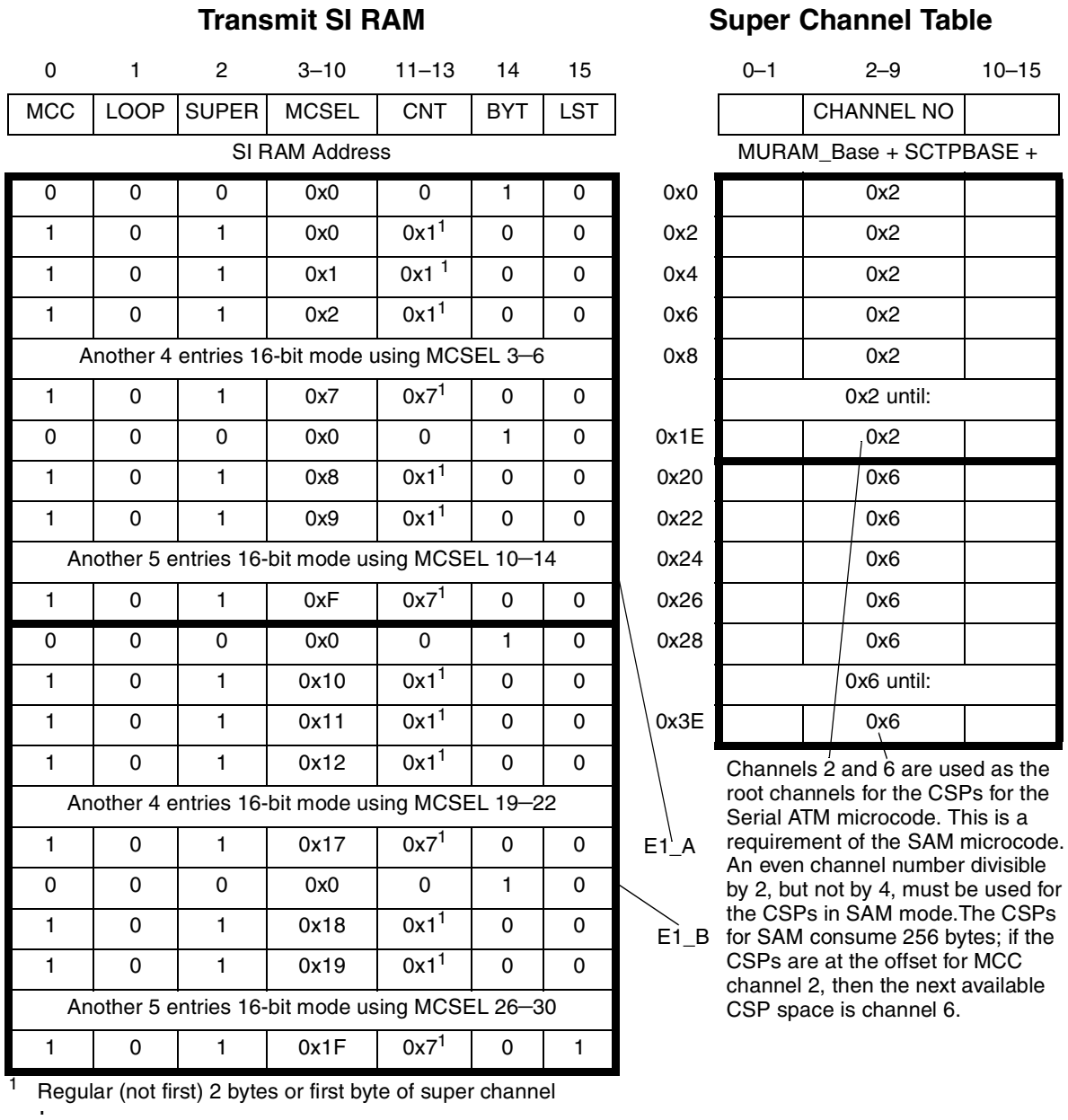

Figure 10. Frame Interleaved SI RAM and MCC Super Channel Initialization for ATM Cells

Programming an entry with the first timeslot of super channel is optional, all entries can programmed for ‘not the first entry’ for the super channel as follows:

MCC	LOOP	SUPER	MCSEL	CNT	BYT	LST
1	0	1	XX	0x1/0x7	0	0

This is possible because the ATM cell start location on the E1 is not fixed. The ATM cell can start at any offset within the E1 frame, and because the cell is 53 bytes, the offset changes frame by frame. There is no requirement to ensure that the ATM cell starts on a specific octet or bit within the E1. Generally the first slot for the super channel option merely ensures that the data starts on this octet of the TDM frame, and is optional for all of the examples provided in this document. It is only relevant for the first TDM frame transmitted by the QUICC Engine module where the receiving entity expects the data to start in a specific timeslot on the TDM.

The MCC channels containing ATM cell data for E1_A in Figure 9 are as follows:

- MCC Channels 0–6 in 16-bit mode fill E1_A timeslots 2–15
- MCC Channel 7 in 8-bit mode fills E1_A timeslot 16
- MCC Channels 8–14 in 16-bit mode fill E1_A timeslots 18–31
- MCC Channel 15 in 8-bit mode fills E1_A timeslot 32

E1_B uses 16 MCC channels as follows:

- MCC Channels 16–22 in 16-bit mode fill E1_B timeslots 2–15 (timeslots 34–47 in Figure 9)
- MCC Channel 23 in 8-bit mode fills E1_B timeslot 16 (timeslot 48 in Figure 9)
- MCC Channels 24–30 in 16-bit mode fill E1_B timeslots 18–31 (timeslots 50–63 in Figure 9)
- MCC Channel 31 in 8-bit mode fills E1_B timeslot 32 (timeslot 64 in Figure 9)

This configuration allows 2 ATM cell streams to be mapped in the SI RAM using 32 transmit MCC channels. Note that for each individual ATM cell stream there are 2 entries in the SI RAM (Figure 10) that are not sourced from any QUICC Engine peripheral. The SI fills these slots will all 1s. Normally the framer device fills these timeslots with signaling and/or control information at the line interface, and typically they are not selective on the TDM. If the user requires that these timeslots (timeslot 1 and timeslot 17 in Figure 8) are sourced from the QUICC Engine module then it is impossible to use the MCC because 16 MCC channels are required to map the 30 timeslots containing ATM cell data. If the MCC is used, more than 16 MCC channels would be required per E1 and 16 E1s could not be supported.

If timeslot 1 and timeslot 17 of the E1 carry data that is sourced from the QUICC Engine block, it is recommended that the UCC is used in QMC mode. It is also recommended that 8 E1s are aggregated onto 2 QUICC Engine TDMs because this allows the minimum number of UCCs for QMC (essentially 2 UCCs, 1 for each TDM). This will allow 16 E1s to be supported with a configuration compliant with ATM Forum specification af-phy-0064.000 and the ITU-T G.804 specification regardless of timeslot 1 and timeslot 17 implementation.

Note that the super channel table configuration shows 16 MCC channels rooted to MCC channel 2 and 16 routed to MCC channel 6. These channel numbers are used because the Serial ATM Microcode on the QUICC Engine module requires it. The data for MCC channels 0–15 is sourced from the CSPs of MCC channel 2, and the data for MCC channels 16–31 is sourced from MCC channel 6.

The following must be taken into account for MCC and SI register initialization:

- As Figure 9 shows, if both 2 E1s on 1 TDM and every E1 need 16 MCC channels, the MCCF must be configured to provide 32 MCC channels to this TDM.
- Each E1 requires 18 SI RAM entries (16 as shown above for the ATM cell data and 2 for control and signaling slots) so the minimum number of entries that will allow the mapping of 2 E1s is 64. The SIxMR must be programmed to provide 64 entries to this TDM.
- To support 16 E1s, another 7 TDMs with the same MCC resource usage are required. Alternatively more E1s can be aggregated on this TDM (up to 8, in which case 2 TDMs are required; see Table 1). For every E1 aggregated no more than 16 MCC channels may be used. SIxMR and MCCF must be programmed to provide sufficient numbers of SI RAM entries and MCC channels respectively to each TDM based on the number of aggregated E1s.

3.1 MCC Receiver Configuration for ATM Cell Mapping

If the TDM A configuration of Figure 9 is also applied to the MCC receiver—and it is assumed that MCC channels 2 and 6 are used to hold the CSPs for Serial ATM initialization—then the result is the following SI RAM configuration shown in Table 3.

Table 3. Frame Interleaving of 2 E1s on 1 TDM Carrying 2 ATM Streams for Receiver

0	1	2	3–10	11–13	14	15
MCC	LOOP	SUPER	MCSEL	CNT	BYT	LST
1 entry of:						
0	0	0	0x0	0x0	1	0
7 entries of:						
1	0	0	0x2	0x1	1	0
1 entry of:						
1	0	0	0x2	0x0	1	0
1 entry of:						
0	0	0	0x0	0x0	1	0
7 entries of:						
1	0	0	0x2	0x1	1	0
1 entry of:						
1	0	0	0x2	0x0	1	0
1 entry of:						
0	0	0	0x0	0x0	1	0
7 entries of:						
1	0	0	0x6	0x1	1	0
1 entry of:						
1	0	0	0x6	0x0	1	0
1 entry of:						

Table 3. Frame Interleaving of 2 E1s on 1 TDM Carrying 2 ATM Streams for Receiver (continued)

0	1	2	3–10	11–13	14	15
0	0	0	0x0	0x0	1	0
7 entries of:						
1	0	0	0x6	0x1	1	0
1 entry of:						
1	0	0	0x6	0x0	1	1

Super channeling is not required on the receiver and only 2 MCC channel Rx FIFOs are required, namely the channels that correspond to the offset of the CSPs for each ATM stream (for example channels 2 and 6).

4 MLPPP Mapping

As with the ATM configuration, the format of the data on the QUICC Engine TDM determines the number of E1s that can be supported for MLPPP. An MCC channel operates in MLPPP mode based on the configuration of the CSPs and not the data format on the TDM.

For clear channel configuration of MLPPP links at the TDM and SI RAM level (all 32 channels on the E1 carrying data for 1 MLPPP link), see Section 2.1.4, “Frame Interleaving”. If the MLPPP link is present on an E1 with timeslot 1 and timeslot 17 used for control and signaling, then the SI initialization in Section 3, “ATM Cell Mapping” is also relevant for MLPPP.

It is possible to support 16 E1s carrying a proprietary MLPPP link mapping on the QUICC Engine TDMs. This can be achieved if there are no inter-operability constraints with other vendors’ end equipment. This allows the full E1 to be used in the most convenient manner for the application.

Figure 11 shows a QUICC Engine TDM carrying aggregated data for 2 E1s. The data on the TDM is fed by 4 MCC super channels running MLPPP. Each MLPPP link consumes 16 timeslots as follows:

- MLPPP Link1 requires 16 octets of TDM A and uses timeslots 1–16
- MLPPP Link2 requires 16 octets of TDM A and uses timeslots 17–32
- MLPPP Link3 requires 16 octets of TDM A and uses timeslots 33–48
- MLPPP Link4 requires 16 octets of TDM A and uses timeslots 49–64

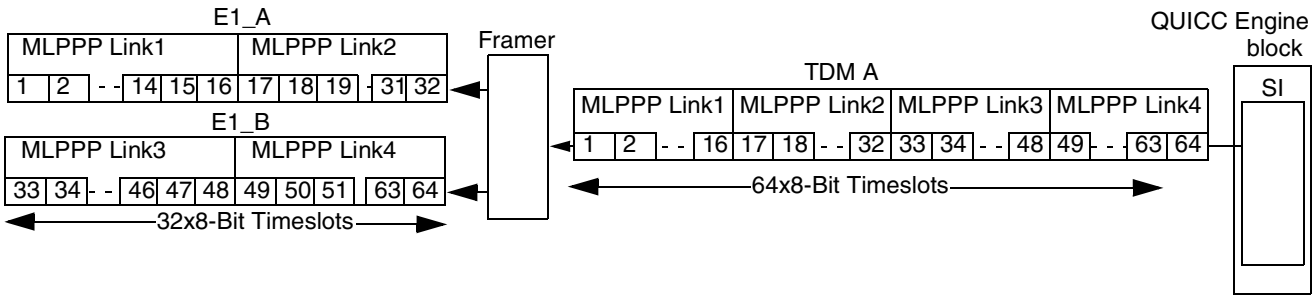

Figure 11. Interleaving 2 E1s Carrying 4 MLPPP Links

The bundling of these MLPPP links is a function of the MLPPP microcode parameters and not the SI RAM initialization. It is assumed that the 4 links form a bundle in the SI RAM configuration for the scenario shown in Figure 12.

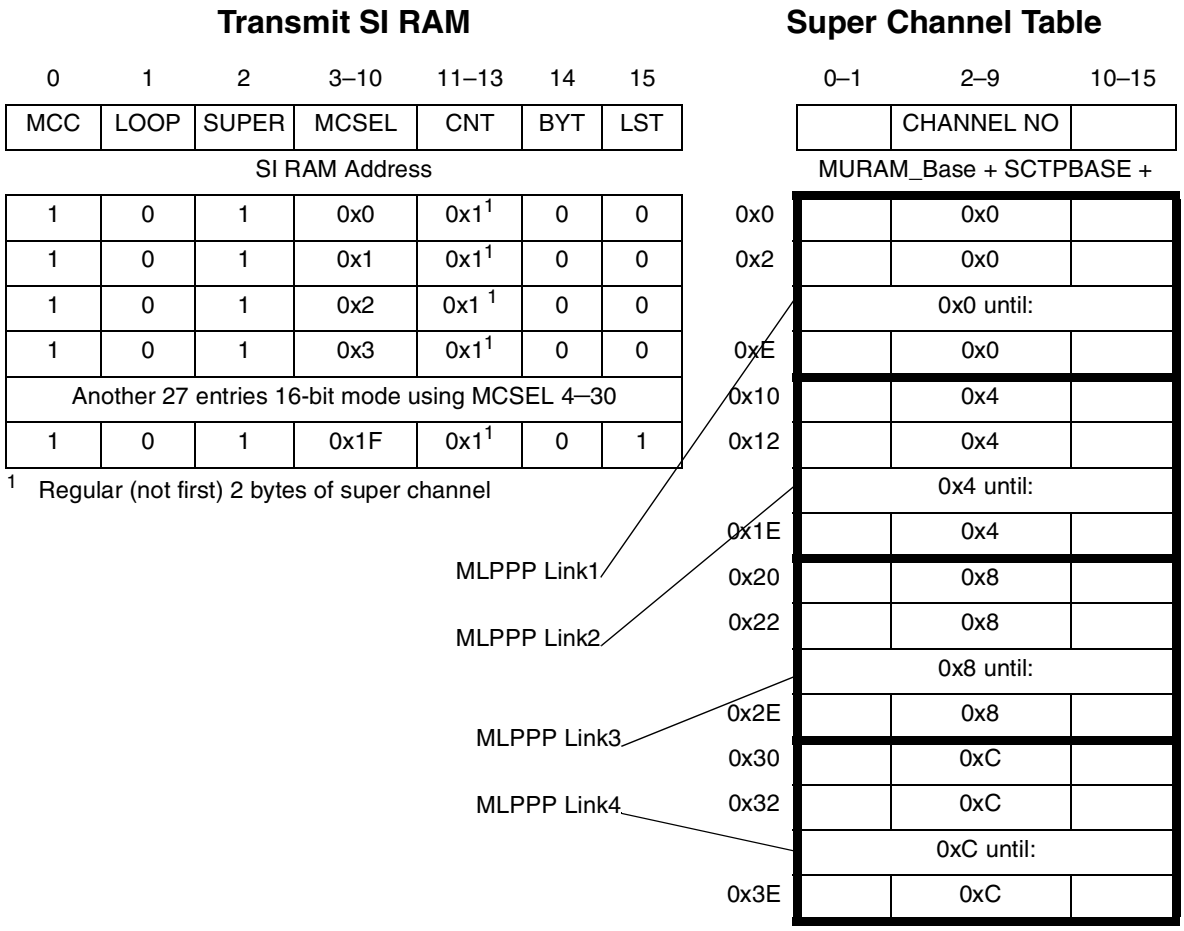

Figure 12. 4 MLPPP Links on 1 QUICC Engine TDM SI RAM Example

32 MCC channels are used to map the 2 E1s in the SI RAM. Because MLPPP does not require any slot synchronization, there is no need to use the first slot in the super channel programming option in the SI RAM. HDLC framing will handle the synchronization at the receiving end. The SI RAM is configured as 32 MCC channels in 16-bit super channel mode. The super channel table is used to define how many 2-byte slots are assigned to each MLPPP Link. As with Serial ATM, an MLPPP enabled MCC channel requires 256 bytes CSP space; this time 256-byte alignment is required. In order to prevent CSP overlap, the CSPs have been programmed to reside at the offsets for MCC channels 0, 4, 8, and 12. The MLPPP links use the MCC resources as follows:

- MLPPP Link1 uses MCC channels 0–7 in 16-bit mode to form the super channel; the base of the CSP is resident at the offset for MCC channel 0 in the MURAM
- MLPPP Link2 uses MCC channels 8–15 in 16-bit mode to form the super channel; the base of the CSP is resident at the offset for MCC channel 4 in the MURAM

- MLPPP Link3 uses MCC channels 16–23 in 16-bit mode to form the super channel; the base of the CSP is resident at the offset for MCC channel 8 in the MURAM
- MLPPP Link4 uses MCC channels 24–31 in 16-bit mode to form the super channel; the base of the CSP is resident at the offset for MCC channel 12 in the MURAM

The user is free to use the other 7 TDMs either in the same manner as TDM A in Figure 11 or a different configuration, either a proprietary or standard body compliant. 16 E1s can be supported if no more than 16 MCC channels are used to describe each E1.

5 Revision History

Table 4 provides a revision history for this application note.

Table 4. Document Revision History

Rev. Number	Date	Substantive Change(s)
1	11/09/2007	Initial public version.

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