Freescale Semiconductor
Application Note

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Migrating from the MC68HC908QY to the MC9S08SH

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1 Introduction

Freescale Semiconductor's MC9S08SH[1] represents a simple, low-cost, high-performance upgrade path from the MC68HC908QY family. The MC9S08SH shares common modules with other HCS08 series. Upgrading to the MC9S08SH also enables easy migration among other HCS08 series as applications evolve.

This document introduces new features in the MC9S08SH and highlights differences between the MC9S08SH and MC68HC908QY. For in-depth implementation of MC9S08SH, please consult datasheet.

Contents

1. The MC9S08SH family mentioned in this document applies only to the MC9S08SH4 and MC9S08SH8 MCUs. Future MCUs in this family may have additional or different features.

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NOTE

If any other Freescale document contains information conflicting with the device data sheet, the data sheet is considered to have the most current and correct data. Except for mask set errata documents

2 Feature Comparisons

MCU Features		MC68HC908			MC9S08	
		QY1	QY2	QY4	SH4	SH8
Core		HC08			S08	
Clock source options	Built-in	12.8 MHz (generates up to 3.2 MHz internal bus frequency)			40 MHz (generates up to 20 MHz internal bus frequency)	
	External	Yes			Yes[1]	
Development support		MON (monitor module)			BDC (background debug controller) and DBG (on-chip debug module)	
Power supply		2.7 V to 5.5 V			2.7 V to 5.5 V	
RAM size (Bytes)		128			256	512
Flash size (Bytes)		1536	1536	4096	4096	8192
Power-saving modes		Wait, stop			Wait, stop2, stop3	
COP		Yes			Yes	
Low voltage detection		Yes (LVI)			Yes (LVD)	
ADC channels		4 (8-bit resolution)[2]			4/8/12 (10-bit resolution)	
Keyboard interrupts or pin interrupts		6			4/8 (depends on packages)	
Timer pulse-width modulator (TPM)		2-ch 16-bit (TIM1)			2-ch 16-bit (TPM1)	
					2-ch 16-bit (TPM2)[3]	
Modulo timer (MTIM)		No			Yes	
Inter-integrated circuit (IIC)		No			Yes	
Analog comparator (ACMP)		No			Yes	
Serial communications interface (SCI)		No			Yes[4]	
Serial peripheral interface (SPI)		No			Yes[5]	
Auto wakeup (AWU)		Yes			Yes (using RTC)	
Package options		16-pin PDIP/SOIC/TSSOP			8-pin NB SOIC 16-pin TSSOP 20-pin PDIP/TSSOP/SOIC 24-pin QFN	

1 8-pin packages do not support an external clock source. FBE and FEE modes are not available.

2 ADC is available only on the MC68HC908QY2 and MC68HC908QY4.

3 8-pin packages have only one channel for TPM2.

[4] SCI is not available in an 8-pin package.
[5] SPI is not available in an 8-pin package.

Benefits for migrating to the MC9S08SH family:

- Cost-effective
- Faster internal clock source and CPU
- An advanced I/O that enables slew rate control and drive strength control
- Up to four times more RAM space
- Up to 8 Kbytes of internal flash space
- Improved EMC
- Fast ADC with a 10-bit resolution
- A built-in temperature sensor in the ADC module
- A non-intrusive on-chip debugging system
- A more accurate internal clock source at a 2% deviation over operational temperature and voltage range
  - Temperature range, –40 to 85 °C ambient or –40 to 125 °C ambient
  - Operating voltage, 2.7 V to 5.5 V
- Two additional 16-bit timer modules available in a 16-pin or 20-pin package
- One additional 8-bit modulo timer (MTIM)
- Dedicated communication SCI, SPI, and IIC modules
- Built-in analog comparator (ACMP)

Potential incompatibilities of migrating to the MC9S08SH family:

- Pin-out differences
- Clock generation differences

3 Pin-to-Pin Conversion

The MC9S08SH is available in 8-pin (NB SOIC), 16-pin (TSSOP), 20-pin (PDIP/SOIC/TSSOP), and 24-pin (QFN) packages. The MC68HC908QY is available only in 16-pin (PDIP/SOIC/TSSOP) packages.

NOTE

The 16-pin PDIP and SOIC are not available in the MC9S08SH.

The MC9S08SH has pin-out differences, making layout changes necessary. Although, the multiplexed functions on each pin from the MC68HC908QY are different than the MC9S08SH, the available functions are similar.

Figure 1 and Figure 2 show the pin layouts for the 16-pin packages between the MC68HC908QY and MC9S08SH.

For all available package layout diagrams, please refer to the MC68HC908QY4 and MC9S08SH8 data sheet.

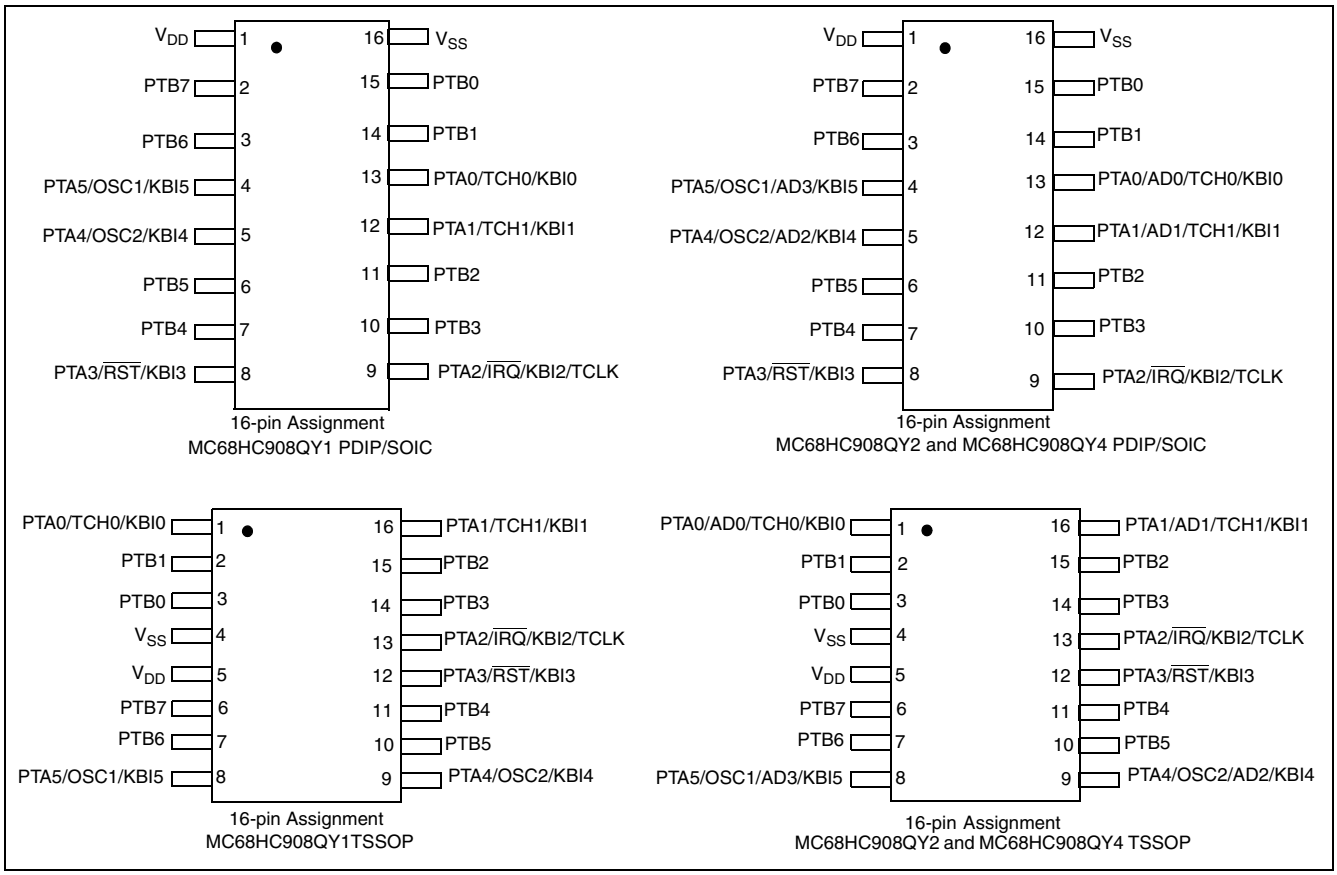

Figure 1. 16-Pin Packages of the MC68HC908QY

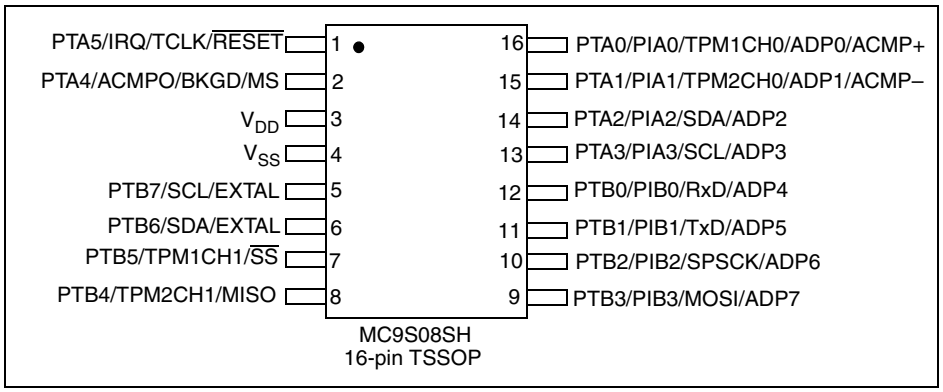

Figure 2. 16-Pin Package of the MC9S08SH

4 Interrupt Request (IRQ)

The MC68HC908QY interrupt request ($\overline{\text{IRQ}}$) function responds to only falling-edge events, or falling-edges and low-level events. The MC9S08SH IRQ function has selectable internal pullup or pulldown modes allowing responses for falling-edge, low-level, rising-edge, and high-level sensitive events. The interrupt request function for both the MC68HC908QY and the MC9S08SH are default to trigger at falling edges out of reset.

The MC68HC908QY has the $\overline{\text{IRQ}}$ and reset ($\overline{\text{RST}}$) on separate pins. The MC9S08SH has IRQ and $\overline{\text{RESET}}$ multiplexed on the same pin. For example, when $\overline{\text{RESET}}$ is enabled on the 16-pin package pin 1, the IRQ loses its functionality to $\overline{\text{RESET}}$. This is because $\overline{\text{RESET}}$ has a higher functional priority than the IRQ on pin 1. To compensate the loss of the IRQ function, use the keyboard interrupt (KBI) from other pins as an IRQ. The enhanced KBI for the MC9S08SH has a similar functionality to an IRQ that triggers interrupts after detecting rising-edge, falling-edge, high-level, or low-level events. The MC68HC908QY $\overline{\text{IRQ}}$ settings are configured through the INTSCR and CONFIG2 registers. The MC9S08SH IRQ settings are configured through the IRQSC.

5 Watchdog Computer Operating Properly (COP)

When the application software fails to execute in the expected time frame, both the MC9S08SH and MC68HC908QY have a COP to force a system reset back to a safe starting point.

The COP in the MC68HC908QY runs from one oscillator output signal (BUSCLKX4). The system clock also shares this signal.

The COP in the MC9S08SH has a software selectable clock source to run from either the bus clock or a low power internal 1 kHz clock source. The benefit of using the 1 kHz clock source is the independency from the system clock. If the system clock is out of order, the COP remains able to force a reset. The MC68HC908QY COP can rely only on the system clock.

6 Development Support

The MC68HC908QY uses a monitor module (MON). The MC9S08SH uses a background debug mode (BDM) for development support. The hardware that supports the BDM consists of a background debug controller (BDC) and an on-chip debug system (DBG).

Both BDM and MON modules provide ways to analyze an MCU operation during software development, such as debugging the application code.

The MC9S08SH BDC has the following benefits over the MC68HC908QY MON:

- The BDM is a single-pin interface that simplifies the hardware set up process. The MON uses only one pin to communicate, but requires several pins to be controlled to enter MON mode.
- The BDM has a self-clocking capability and does not require a specific baud rate to communicate to the MCU.
- The BDM can read the MCU address in real time while the application is running. An MC68HC908QY must halt the application to read the memory address contents.

- The BDM requires only one power source V_{DD} to enter active mode. MON requires two power sources, one to the V_{DD} pin and the other to the $\overline{IRQ}$ pin.

Useful application notes:

- *AN3335 — Introduction to HCS08 Background Debug Mode*
- *AN2497 — HCS08/RS08 Background Debug versus HC08 Monitor Mode*
- *AN2596 — Using the HCS08 Family On-Chip In-Circuit Emulator (ICE)*

7 Voltage Supply Range

Both the MC68HC908QY and MC9S08SH have the same operating voltage range, from 2.7 V to 5.5 V. The MC9S08SH is part of the HCS08 family. It can operate in low-voltage/low-power performance without sacrificing CPU performance. The bus speed in the MC68HC908QY is voltage dependent. The MC9S08SH can maintain maximum bus speed across the entire voltage operating range (2.7 V – 5.5 V).

8 Low-Voltage Detect System

Both the MC9S08SH and MC68HC908QY have systems to protect against low-voltage conditions, preserve memory contents, and control the MCU operation during supply voltage variations. The MC9S08SH uses a low-voltage detect (LVD) module. The MC68HC908QY uses a low-voltage inhibit (LVI) module.

The LVI and LVD have two low voltage detection points:

- The LVD and LVI modules can be configured to force a reset when the V_{DD} voltage falls below the trip falling voltage.
- The MC9S08SH LVD typical trip falling voltage is 2.56 V or 4.0 V
- The MC68HC908QY LVI typical trip falling voltage is 2.55 V or 4.2 V
- The MC68HC908QY LVI has a LVIOUT flag to indicate the V_{DD} falls below the reset voltage trip point. The MC9S08SH LVD does not have this flag. Instead, the LVD has a LVWF flag to indicate a low voltage warning point that is above the reset voltage trip point.

Key enhancements of the MC9S08SH LVD:

- The MC9S08SH has four selectable low voltage warning (LVW) thresholds: VLVW0, VLVW1, VLVW2, and VLVW3. Please see the values in the data sheet. The LVW point is above the reset trip falling voltage. When the supply voltage falls below the LVW point, the LVWF flag is set.
- The MC9S08SH low voltage warning flag (LVWF) can be configured to generate an interrupt when a LVW point is detected (LVWF=1). This gives the user the option to implement ISR routine to manage the low power condition. The MC68HC908QY LVI does not have an interrupt. The LVI can only set the LVIOUT flag or force reset.
- The MC9S08SH LVD is configured using the system power management status and controls registers, SPMSC1 and SPMSC2. The MC68HC908QY LVI is configured using the CONFIG1 register.

Useful application notes:

- *AN3305 — On-Chip System Protection Basics for HCS08 Automotive Microcontrollers*

9 Power-Saving Modes

The MC68HC908QY has wait and stop modes.

The MC9S08SH has wait, stop2, and stop3 modes.

- Wait — Both the MC68HC908QY and MC9S08SH have wait mode and are functionally equivalent. In this mode, the CPU clock is turned off to reduce power. The MCU in wait mode consumes less power than the run mode. Both parts enter wait mode by executing an assembly wait instruction in the software code. All modules that have interrupt capability in MC9S08SH can exit wait mode returning to run mode. Exiting wait mode is done by evoking an interrupt triggered by a module active under this mode. After exiting from wait via an interrupt, the MCU services the interrupt with a corresponding interrupt service routine (implemented by the user). After the interrupt is serviced, the MCU continues operation at the instruction code following the wait command. The RAM content and peripheral register configurations are on hold in the state they are in prior to executing the wait command. These states are maintained and resume after the MCU exits from wait mode. Wait mode can also exit with system resets. Upon exit by a reset, the MCU restarts at the beginning of the software program where the reset vector returns to the application start-up routine. RAM data is unaffected by any reset, provided the application reset vector start-up routine does not initialize RAM spaces and the supply voltage does not drop below the RAM retention voltage (VRAM = 1 V as specified in the datasheet Rev. 3). However if exit with the power-on RESET, all I/O, register content, and RAM will be lost.
- Stop3 — is the same as the MC68HC908QY stop mode. In this mode, the regulator is put into a loose regulation mode in which it consumes less current then wait mode, but can also support the static state of RAM and registers. A difference between stop3 and the M68HC08 stop mode is; how stop recovery is managed. Stop recovery on the MC68HC908QY is a timed event lasting 32 or 4096 oscillator cycles, plus the time the oscillator source uses to start. On the MC9S08SH, stop recovery is based on the voltage regulator’s time to power up and return to full regulation.
- Stop2 — this mode uses less power than stop3. This is the lowest power mode available for the MC9S08SH and is not available in the MC68HC908QY. Stop2 is a partial power-down mode in which most internal systems are turned off, but RAM remains powered. The registers values after exiting from stop2 mode are not kept. They must be re-initialized with the content that was manually saved on the RAM prior to entering stop2. RAM is powered in this mode and register values can be saved and restored. The internal voltage regulator is also turned off in this mode. The I/O pins remain latched in the state they were in upon entering stop2. Existing stop2 always recovers from the reset vector. To distinguish a stop2 recovery from a normal reset, examine the status of the partial power down flag (PPDF) in the system power management status and control register 2 (SPMSC2). This flag is set upon waking up from stop2 and can direct user code to a stop2 recovery routine. PPDF remains set and the I/O pins remain latched until a 1 is written to the partial power down acknowledge (PPDACK) bit in SPMSC2.

For more information on HCS08 stop modes see:

- *HCS08QRUG — HCS08 Peripheral Module Quick Reference*
- *AN2493 —MC9S08GB/GT Low-Power Modes*

10 Auto Wakeup (AWU) vs. Real-Time Counter (RTC)

Both the MC9S08SH RTC and the MC68HC908QY AWU provide clocking mechanisms to generate periodic interrupts to wake the MCU from a low-power mode.

The MC68HC908QY AWU is active only in stop mode and shares the KBI interrupt vector. The AWU has only two selectable interrupt periods (650 ms or 16 ms when the V_{DD} = 5 V, 875 ms or 22 ms when the V_{DD} = 3 V).

The MC9S08SH RTC is active for all modes (run, wait, stop2, and stop3). The RTC interrupt vector is independent from the KBI interrupt vector. The RTC operates using either the low power 1 kHz internal clock (LPOCLK), the 32 kHz internal reference clock (ICSIRCLK), and the external clock (ERCLK). The RTCLKS bits in the RTCSC register are used to select the clock source. The three clock sources can be used in run, wait, or stop3 mode. The RTC is active in stop2 only when the internal 1 kHz clock source is selected. In this case, the RTC can wake the MCU from stop2 mode. The RTC has sixteen selectable interrupt periods for each clock source. See Table 1.

Table 1. Prescaler Period

RTCPS	1 kHz Internal clock (RTCLKS = 00)	1 MHz External clock (RTCLKS = 01)	32 kHz Internal clock (RTCLKS = 10)	32 kHz Internal clock (RTCLKS = 11)
0000	Off	Off	Off	Off
0001	8 ms	1.024 ms	250 µs	32 ms
0010	32 ms	2.048 ms	1 ms	64 ms
0011	64 ms	4.096 ms	2 ms	128 ms
0100	128 ms	8.192 ms	4 ms	256 ms
0101	256 ms	16.4 ms	8 ms	512 ms
0110	512 ms	32.8 ms	16 ms	1.024 s
0111	1.024 s	65.5 ms	32 ms	2.048 s
1000	1 ms	1 ms	31.25 µs	31.25 ms
1001	2 ms	2 ms	62.5 µs	62.5 ms
1010	4 ms	5 ms	125 µs	156.25 ms
1011	10 ms	10 ms	312.5 µs	312.5 ms
1100	16 ms	20 ms	0.5 ms	0.625 s
1101	0.1 s	50 ms	3.125 ms	1.5625 s
1110	0.5 s	0.1 s	15.625 ms	3.125 s
1111	1 s	0.2 s	31.25 ms	6.25 s

Besides the comparable functionalities to the AWU, RTC also has the following additional features:

- 8-bit up-counter
- 8-bit modulo match limit
- Software controllable periodic interrupt on match
- Three software selectable clock sources for input to the prescaler with selectable binary-based and decimal-based divider values
- Three software selectable clock sources for input to prescaler with selectable binary-based and decimal-based divider values:
  - Free running internal 1 kHz low-power oscillator (LPO) clock source for cyclic wakeup without external components. Ability to operate in all MCU modes
  - External clock source (ERCLK) for precise time base, time-of-day, calendar, or task scheduling functions
  - 32 kHz internal clock (IRCLK) for accuracy with only a 2% deviation over the comparable of the external clock source

11 Peripherals

11.1 Clock Sources

Both the MC68HC908QY and MC9S08SH run from an external clock source or a built-in internal clock source. The MC68HC908QY configures the system clock source via the oscillator (OSC) module. The MC9S08SH uses the internal clock source (ICS) module.

The MC68HC908QY built-in internal clock has a 5% of deviation. The MC9S08SH built-in internal clock has a 2% of deviation, offering a more accurate clock source.

The MC68HC908QY supports the external clock source with either an external oscillator, crystal, ceramic resonator, or resister-capacitor (RC) circuit. The MC9S08SH supports external clock sources similar to the MC68HC908QY, but the MC9S08SH does not support the RC circuit as an external clock source.

In the MC68HC908QY, the internal bus clock frequency is always one fourth of any of the OSC source options. In the MC9S08SH, the internal bus clock frequency is always one half of the ICSOUT. The ICSOUT speed can be further reduced by configuring the BDIV, that decreases the bus frequency.

The MC68HC908QY is limited to run at a maximum of 8 MHz bus speed. When the MC68HC908QY OSC is configured to use the internal oscillator, the maximum bus speed (INTCLK divided by 4) is limited to 3.2 MHz. To run at a maximum of 8 MHz bus speed, the MC68HC908QY OSC module requires the V_{DD} at 5 V and incorporates an external 32 MHz reference clock such as the canned crystal oscillator. When the V_{DD} is at 3 V, the MC68HC908QY OSC can run only at a maximum of 4 MHz bus speed with a 16 MHz external reference clock. The external reference clock requires a larger board design and higher power supply. When the internal clock source is used, the MC68HC908QY bus frequency is limited to either 1 MHz, 2 MHz, and 3.2 MHz.

The MC9S08SH eliminates the need for an external oscillator by providing an internal ICS module capable of a higher bus frequency and accuracy. After porting to the MC9S08SH, applications can run up

to a maximum of 20 MHz bus speed (ICSOUT/2) using only the internal clock. The MC9S08SH ICS can maintain maximum bus speed across the entire voltage operating range (2.7 V – 5.5 V). The MC9S08SH also supports the external clock source. In Figure 3, solid intervals are the possible bus frequency if ICS is using the internal reference clock running in FLL engaged internal (FEI) mode. The bus frequency is available within the interval of 2 to 2.5 MHz, 4 MHz to 5 MHz, 8 MHz to 10 MHz, and 16 MHz to 20 MHz.

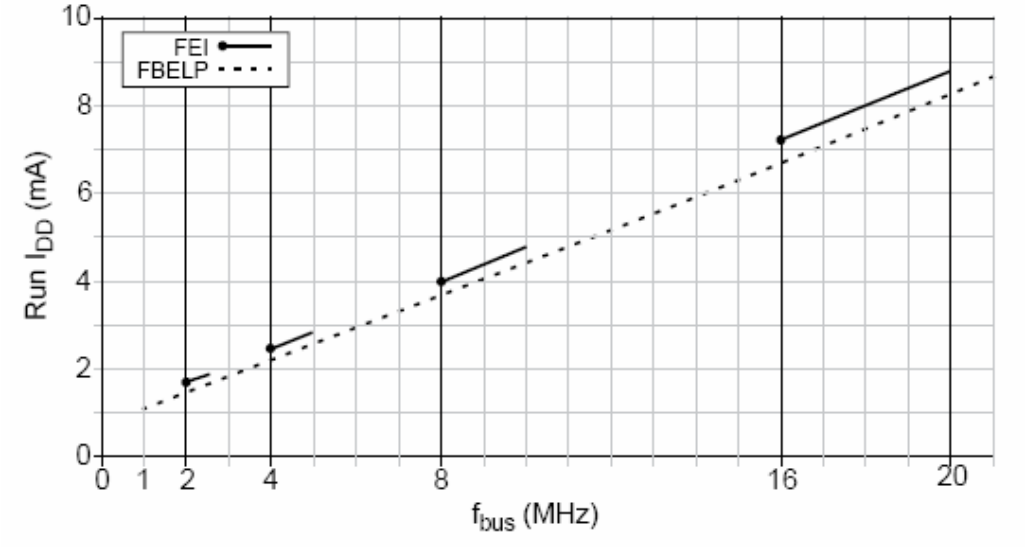

Figure 3. MC9S08SH Typical Run I_{DD} vs. Bus Frequency (V_{DD} = 5 V) (Referenced from data sheet Figure A-5.)

11.2 Timer Pulse-Width Modulator (TPMV3)

Table 2. Key Differences Between the MC9S08SH and MC68HC908QY4

Timer	MC9S08SH	MC68HC908QY
Quantity	Two timers (TPM1 and TPM2)	Only one timer (TIM)
TPM external input clock source	TCLK	TCLK
Counter mode	Up/down counter	Only up counter
Output compare	Yes	Yes
Input capture	Yes	Yes
PWM edge-aligned	Yes	Yes
PWM center-aligned	Yes	No
Clock sources	3	2
Operating modes	Run, wait	Run, wait
Clock prescalers	8 (divide by 1, 2, 4, 8, 16, 32, 64, or 128)	7 (divide by 1, 2, 4, 8, 16, 32, or 64)

The MC9S08SH uses a new timer called the timer/PWM module (TPM) designed for the HCS08 family. It performs all the functions of the M68HC08 family's timer interface module (TIM) used by the MC68HC908QY. The HCS08 TPM also reduces the complexity of the M68HC08 TIM functions and improves the use of the MCU resources.

NOTE

In the MC9S08SH, the ACMP module can be configured to connect the ouput of the analog comparator to TPM1 input capture channel 0 by setting ACIC in SOPT2. With ACIC set, the TPM1CH0 pin is not available externally regardless of the configuration of the TPM1 module for channel 0.

Key enhancements of the MC9S08SH timer:

- All MC9S08SH8 MCUs have two TPM modules. Each TPM module contains one or two TPM channels depending on the package's pin count. The 16-pin, 20-pin, and 24-pin packages each have a total of four TPM channels (two channels for each of the TPM1 and the TPM2). The 8-pin package has two channels. All MC68HC908QY packages have only two channels.
- The TPM has an up/down count mode. The TIM counts only up. Center-aligned PWM signals are created with the TPM. This is not possible with the TIM.
- The TPM clock source can be selected from either the bus clock, external clock TCLK (also called TPMCLK), or the fixed system clock (XCLK). The TIM clock source is limited to the bus clock or an external clock.
- The selected TPM clock source is divided by eight prescalers: 1, 2, 4, 8, 16, 32, 64, or 128. The TIM clock source has seven prescalers: 1, 2, 4, 8, 16, 32, and 64.
- Any single channel can be configured for the buffered PWM on the TPM. The TIM requires two channels to generate a buffered PWM.
- The register interface has been modified to make programming the TPM easier.

Please refer to *AN2717 — M68HC08 to HCS08 Transition* section 6.4. This section provides steps to configure the TPM that are applicable to the MC9S08SH TPM.

11.3 Modulo Timer (MTIM)

The modulo timer (MTIM) is new for the HCS08 family of MCUs. No equivalent peripheral exists on any variant of the MC68HC908QY. Timer system features include:

- 8-bit up-counter
  - — Free-running or 8-bit modulo limit
  - — Software controllable interrupt on overflow
  - — Counter reset bit (TRST)
  - — Counter stop bit (TSTP)
- Four software selectable clock sources for input to prescaler:
  - — System bus clock — rising edge
  - — Fixed frequency clock (XCLK) — rising edge
  - — External clock source on the TCLK pin — rising edge
  - — External clock source on the TCLK pin — falling edge
- Nine selectable clock prescale values:
  - — Clock source divided by 1, 2, 4, 8, 16, 32, 64, 128, or 256
- MTIM can be configured to run in wait mode

11.4 Analog-to-Digital Converters

Table 3. Key Differences Between the MC9S08SH and MC68HC908QY

Analog-to-Digital Converters	MC9S08QSH	MC68HC908QY
Resolution	10-bit or 8-bit	8-bit only
Conversion clock frequency	Up to 8 MHz	Up to 1 MHz
Built-in temperature sensor	Yes	No
Hardware trigger	Yes	No
Automatic compare function	Yes	No
Operating modes	Run, wait, stop3	Run, wait
Bandgap voltage reference	Yes	No
Clock sources	3	2
ADC pin control	Yes	No
Single conversion time (max)	~3.1 μs (8-bit); ~3.5 μs (10-bit)	~16 μs (8-bit)
Clock prescalers	4 (divide by 1, 2, 4, or 8)	5 (divide by 1, 2, 4, 8, or 16)

Key enhancements of the MC9S08SH ADC:

- Output is formatted in a 10- or 8-bit right-justified format.
- A temperature sensor is included in the MC9S08SH ADC module. The temperature sensor output is attached to one of the ADC analog input channels (AD26). *AN3031 — Temperature Sensor for the HCS08 Microcontroller Family* has useful guidelines for implementing the temperature sensor feature.
- The MC9S08SH ADC hardware trigger (ADHWT) is output from the real-time counter (RTC). The RTC counter is clocked by the ICSERCLK, ICSIRCLK, or a nominal 1 kHz clock source. When enabled, the hardware trigger initiates a conversion on an RTC overflow.
- The automatic compare function of the MC9S08SH can be configured to check for an upper or lower limit. If the compare condition (either upper or lower limit) is met and the ADC interrupt is enabled, the conversion complete flag (COCO) is set and an interrupt occurs. If the compare condition is not met, the conversion complete flag is not set. The automatic compare function monitors a voltage on a channel in either wait or stop3 mode. When the compare condition is met, the resulting ADC interrupt (if enabled) wakes the MCU.
- The ADC's clock source can be selected from either the MCU bus clock, the bus clock divided by two, the local asynchronous clock (ADACK) within the module, or the alternate clock (ALTCLK). The alternate clock for the MC9S08SH MCU devices is the external reference clock (ICSERCLK).
- The ADACK is within the ADC module. When the ADACK is selected as the clock source, this clock remains active while the MCU is in wait or stop3 mode and allows conversions in these modes for lower noise operation. The ADC with ADACK selected can also wake the MC9S08SH from wait and stop3 modes.
- The APCTL registers are used to disable the digital input buffers on selected pins. When a pin is configured as an ADC channel through the ADCH bits (the ADCSC1 register), the corresponding pin is automatically configured as an input, but the digital input circuitry remains operating and can interfere the incoming analog signal the ADC is trying to measure. By using the APCTL register, the input circuitry can be disabled to minimize interference. There is an option not to use this function, but using the APCTL is highly recommended.

Please refer to *AN2717 — M68HC08 to HCS08 Transition* section 6.9. This section details the ADC module that is generally used in the HCS08 MCUs.

11.5 Parallel Input/Output Control

Key enhancements of the MC9S08SH I/O pins:

- Ganged output — The MC9S08SH8 devices contain a feature that allows up to eight port pins to be tied together externally allowing higher output current drive.
- Each port pin can be enabled for slew rate control by setting the corresponding bit in the PTxSEn register. Slew rate control limits an output signal transition rate to reduce EMC emissions. Slew rate control has no effect on pins that are configured as inputs.
- Each output pin can be enabled for high output drive strength by setting the corresponding bit in the PTxDSn register. Enabling the high drive strength function allows a pin to source and sink a greater current. The user must ensure that the total current source and sink limits for the MCU are

not exceeded. The drive strength selection affects the DC behavior of I/O pins. The AC behavior is also affected. High drive allows a pin to drive a greater load with the same switching speed as a low-drive-enabled pin into a smaller load. Enabling pins as high drive increases current output and may increase EMC emissions.

11.6 KBI/Pin Interrupts

The MC9S08SH incorporates the KBI features into the parallel input/output control logic. Instead of the KBI, the MC9S08SH names it as Pin Interrupts.

The MC68HC908QY KBI and MC9S08SH Pin Interrupts function can be enabled or disabled individually on their associated pins. Key differences are:

- The MC9S08SH has up to eight external interrupt pins. The MC68HC908QY has four KBI pins.
- The MC9S08SH port A[3:0] and port B[3:0] pins can be configured as external interrupt inputs. These interrupts can mimic IRQ functions to wake the MCU from stop3 and wait modes.
- The MC9S08SH external interrupt pins can be configured for falling edge, falling edge and level, rising edge, or rising edge and level sensitivity. The MC68HC908QY KBI provides only falling edge or falling edge and level sensitivity.
- Each port pin interrupt can be independently enabled or disabled via the PTxPS register. Pin interrupts as edge-sensitive or edge-and-level-sensitive can be set via the PTxMOD bit from the PTxSC register. Polarity of the edge-or edge-and-level sensitivity is set using the PTxESn bits in the register PTxES register.

11.7 Analog Comparator (ACMP)

The analog comparator (ACMP) is new for the HCS08 family MCUs. No equivalent peripheral exists on any variant of the MC68HC908QY. The analog comparator can be used to compare two external analog input voltages applied to the ACMP+ and ACMP–. It can also be used to compare an analog input voltage applied to the ACMP– with an internal bandgap reference voltage. The comparator output is indicated by the analog comparator flag (ACF) from the ACMPxSC register. The ACF is high if the non-inverting input is greater than the inverting input, and is low when the non-inverting input is less than the inverting input. The comparator output can also be driven onto the ACMPO pin by setting ACOPE to 1.

The ACMP has the following features:

- Full rail-to-rail supply operation
- Selectable interrupt on rising edge, falling edge, or either rising or falling edges of comparator output
- Option to compare to fixed internal bandgap reference voltage
- Option to allow comparator output to be visible on a pin, ACMPO
- Can operate in stop3 mode

11.8 Inter-Integrated Circuit (IIC)

The inter-integrated circuit (IIC) module is new on the MC9S08SH. No equivalent peripheral exists on any variant of the MC68HC908QY. The IIC is a 2-wire communication bus for efficient inter-IC control. The IIC bus physically consists of a serial data line (SDA) and serial clock line (SCL). Every IIC embedded device connected to the bus has its own unique address. Each of these devices can act as a receiver and/or transmitter, depending on the functionality.

Maximum communication length and the number of connected devices are limited by a maximum bus capacitance of 400 pF.

The IIC includes these distinctive features:

- Configurable to either master or slave
- Compatible with IIC bus standard and operates up to 100 kbps with maximum bus loading and timing
- Multi-master operation allowing more than one IIC device capable of initiating a data transfer connection on the same bus
- Software programmable for one of 64 different serial clock frequencies
- Software selectable acknowledge bit
- Interrupt driven byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated start signal generation
- Acknowledge bit generation/detection
- Bus busy detection that notifies when the bus is clear for new transmission
- General call recognition
- A 10-bit address extension that gives more address combinations than the standard 7-bit; this allows more nodes to be connected on the same IIC bus

11.9 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) module is new on the MC9S08SH. No equivalent peripheral exists on any variant of the MC68HC908QY. Unlike IIC, SPI lacks a built-in device addressing functionality. The SPI requires more effort and more hardware resources than the IIC when more than one slave is involved. But the SPI is simpler and has less overhead than the IIC in point-to-point data streaming communication (single master, single slave). The SPI duplex capability also allows application simultaneously sending samples in and out.

The SPI includes these distinctive features:

- Master or slave mode operation
- Full-duplex or single-wire bidirectional option
- Programmable transmit bit rate

- Double-buffered transmit and receive
- Serial clock phase and polarity options
- Slave select output
- Selectable MSB-first or LSB-first shifting

11.10 Serial Communications Interface (SCI)

The serial communications interface (SCI) module is new on the MC9S08SH. No equivalent peripheral exists on any variant of the MC68HC908QY.

Features of the SCI module include:

- Full-duplex, standard non-return-to-zero (NRZ) format
- Double-buffered transmitter and receiver with separate enables
- Programmable baud rates, 13-bit modulo divider
- Interrupt-driven or polled operation:
  - Transmit data register empty and transmission complete
  - Receive data register full
  - Receive overrun, parity error, framing error, and noise error
  - Idle receiver detect
  - Active edge on receive pin
  - Break detect supporting LIN
- Hardware parity generation and checking
- Programmable 8-bit or 9-bit character length
- Receiver wakeup by idle-line or address-mark
- Optional 13-bit break character generation / 11-bit break character detection
- Selectable transmitter output polarity

12 Conclusion

Freescale's MC9S08SH offers similar functions and allows easy migration from MC68HC908QY modules. The MC9S08SH enhancements include:

- A faster internal clock source
- Four times the RAM size
- Lower power consumption mode
- A user friendly background debugger controller
- Enhanced ADC with a built-in temperature sensor
- I/O drive strength and slew rate controls
- Dedicated SCI/SPI/IIC communication modules
- KBI rising/falling-edge detections
- Two extra 8-bit modulo counters (from RTC and MTIM)
- Two 16-bit TPM timer modules capable of a PWM center-aligned output signal

These upgrades allow programmers or designers to enhance the applications by migrating to the cost-effective MC9S08SH.

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