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Freescale Semiconductor
Application Note

MC13783 Switcher Settings to Optimize ±1MHz ModORFS Performance

by: Power Management and Audio Application Team

1   Introduction

On platforms using the MC13783 power management IC and RFX300-30 RF transceiver, the transceiver may be supplied by DC/DC converters (switchers) from the MC13783. These switchers are driven by a common circuitry which is composed of a ~1MHz PLL and a phase shifter.

The objective of this application note is to provide the customer with recommendations concerning MC13783 switcher supply settings which could degrade Output RF Modulation Spectrum performance on the RFX 300-30 platform. Measurements will outline the benefit of changing the default MC13783 Switcher PLL frequency to an optimized one.

2   RFX300-30 Power Supply Interface

Figure 1 shows the interconnections between MC13783 and RFX300-30 circuits. This configuration used two Switchers (SW1 and SW2) from the MC13783. SW1 and SW2 feed different RFX300-30 blocks:

Contents

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SW1 (default 1.25 V):

- Digital: Rx digital core, HC12 Memory, Small Dig Core
- TxBB: Tx Digital Core

SW2 (default 1.8V):

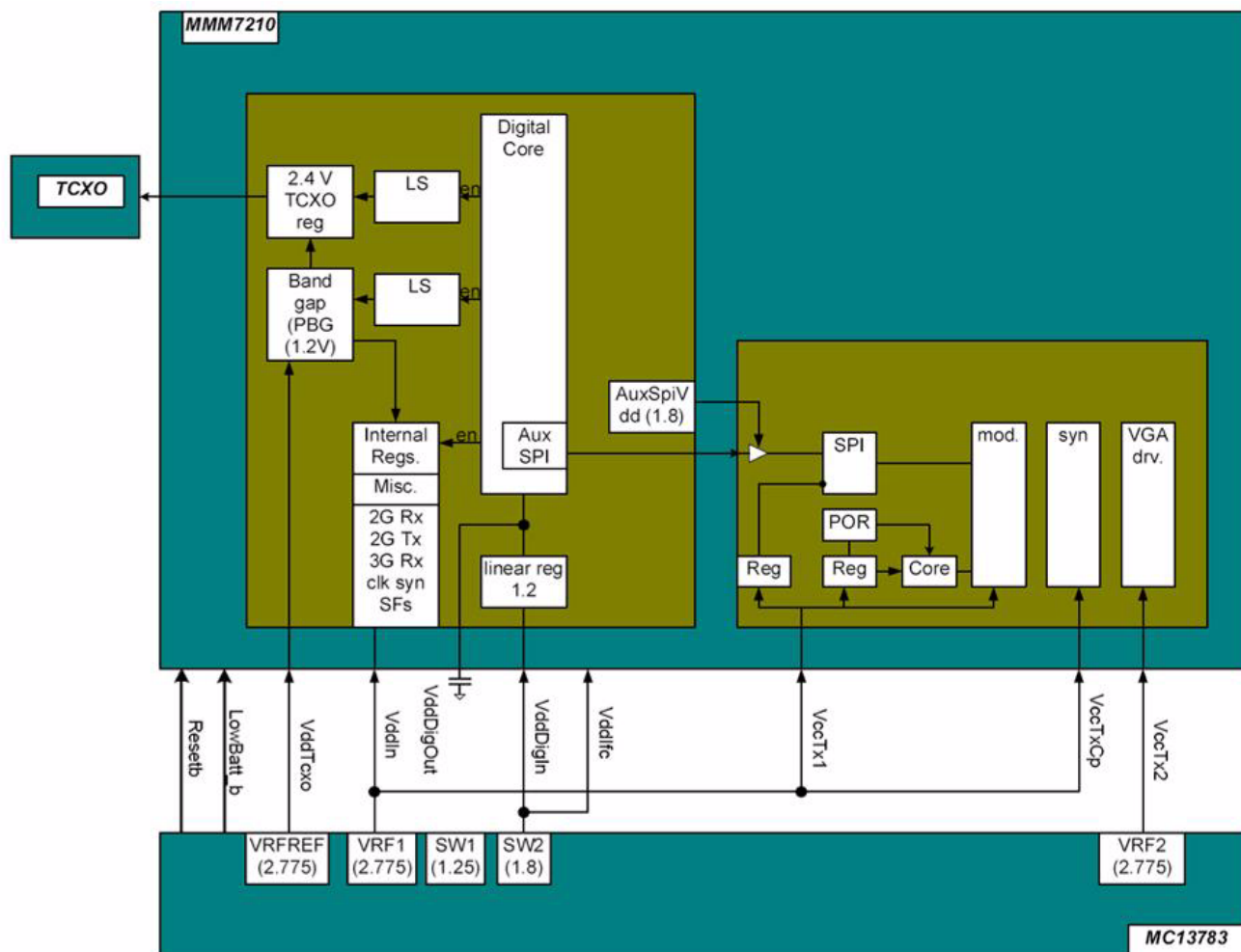- BB Interface: BBIO_2G_3G, BB_IFC_GPIO, BB_IO_SPI, BB_IO_Strobe

Figure 1. Power Connect with Core Supply from External Switching Regulator

3 MC13783 Buck Switchers Architecture and Control

3.1 Switcher Architecture

Figure 2 and Figure 3 display the switcher schematic and waveforms for transistor switched output voltage (VD), Inductor voltage (VL), Output Voltage (VO) and Inductor current (IL). The signal VD is a

rectangular signal with a frequency near 1MHz (setup by the PLLX register) and a variable duty-cycle, controlling by voltage output and depending on load current.
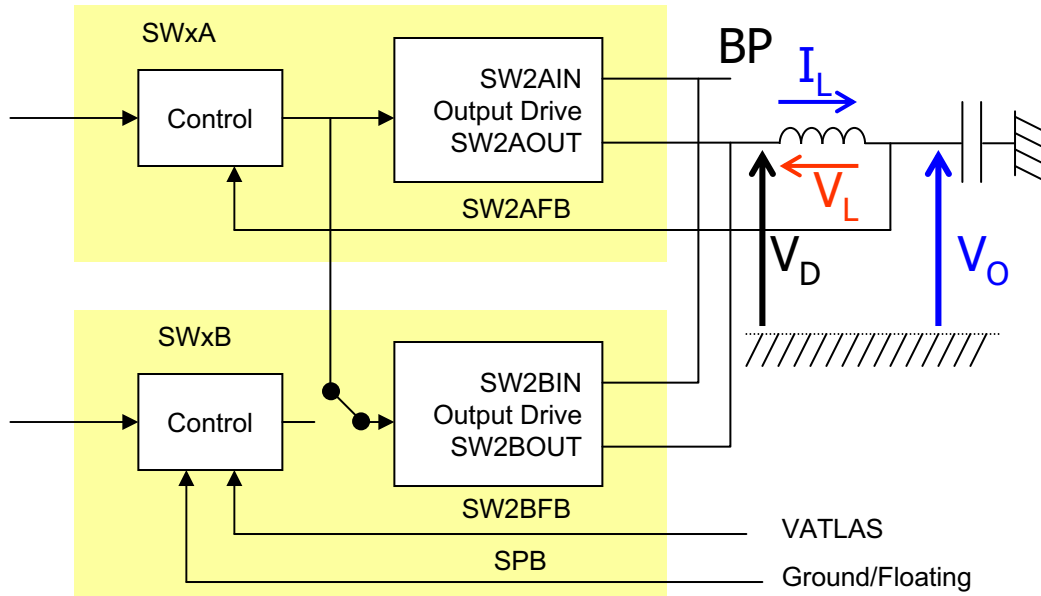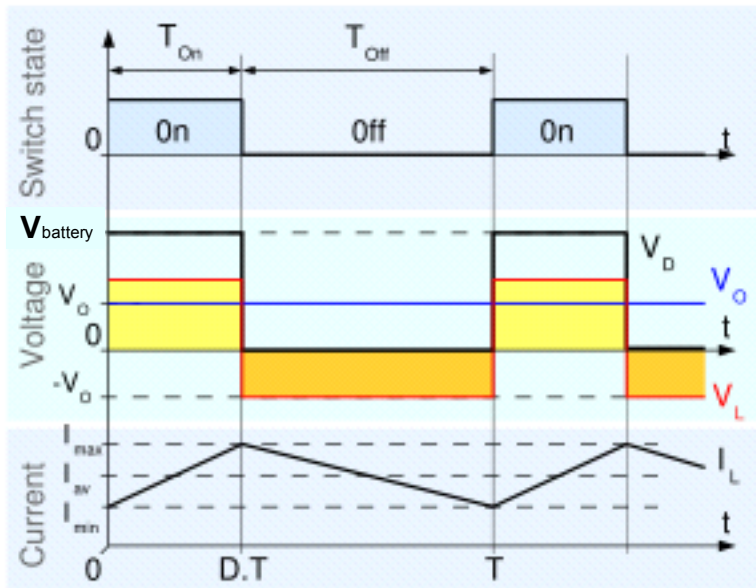

Figure 2. Switcher Architecture

Figure 3. Switched Power Waveform

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3.2 Switcher Control

The switchers are driven by common circuitry which is composed of a PLL and a phase shifter. The PLL generates an effective 1.048MHz signal based upon the 32.768 kHz oscillator signal by multiplying it by 32. Internally, the PLL may generate higher clock frequencies for its proper use or for use by other blocks such as the ADC core. To reduce spurious signals for certain radio channels, the PLL can be programmed via PLLX[2:0] to different values.

Table 1. PLL Multiplication Factor

PLLX[2:0]	Multiplication Factor	Switching Frequency (Hz)	ADC Core Frequency (MHz)
000	28	917 504	1.835
001	29	950 272	1.901
010	30	983 040	1.966
011	31	1 015 808	2.032
100	32	1 048 576	2.097
101	33	1 081 344	2.163
110	34	1 114 112	2.228
111	35	1 146 880	2.294

During normal operation, several power modes will exist depending on the loading:

- For medium and full loading, a synchronous PWM control is the most efficient while maintaining a constant frequency (phone active mode).
- For low loading (50 mA max, phone standby mode), PFM (pulse frequency modulation) mode is used.

Two PWM modes are available: the first mode sacrifices low load efficiency for a continuous switching operation. The second mode offers better low load efficiency by allowing the absence of switching cycles at low output loading. This "pulse skipping" feature improves efficiency by reducing dynamic switching losses simply by switching less often.

Table 2. Switching Mode Setup

Parameter	Value	Function
SWxyMode[1:0] SWxySTBYMODE[1:0]	00	OFF
	01	PWM mode No Pulse Skipping
	10	PWM mode Pulse Skipping Allowed
	11	Low Power PFM mode

PWM mode No Pulse Skipping is the default mode at power-up.

3.3   Measurements

The plot in Figure 4 gives the spectrum measured by coupling with an active probe placed near switchers output. The fundamental frequency (fo) is the switcher frequency (1 MHz) and all harmonics (n*fo) are present with a high level at the switchers output (Figure 4). Near RFX300-30, the fundamental is still present (Figure 5).
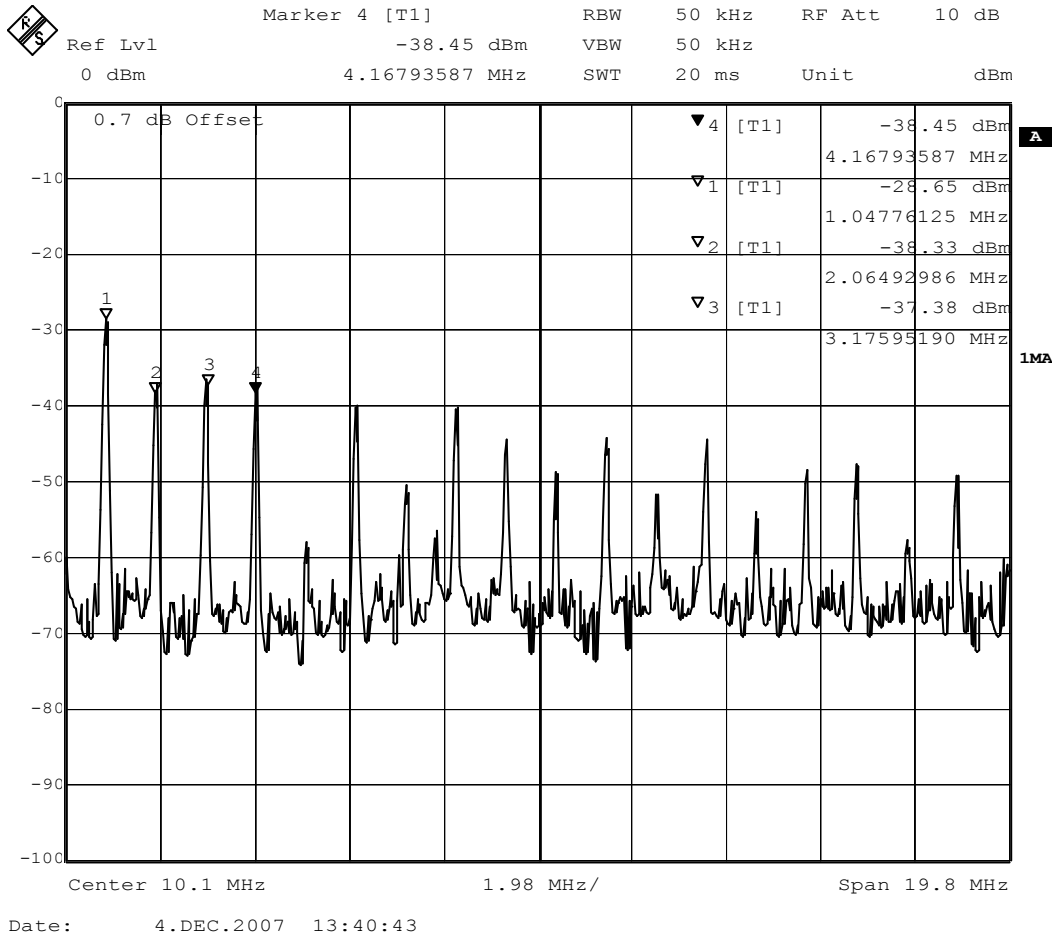

Figure 4. Switchers Output Spectrum

Figure 5 shows the switchers output near RFX300-30, with all shielding:
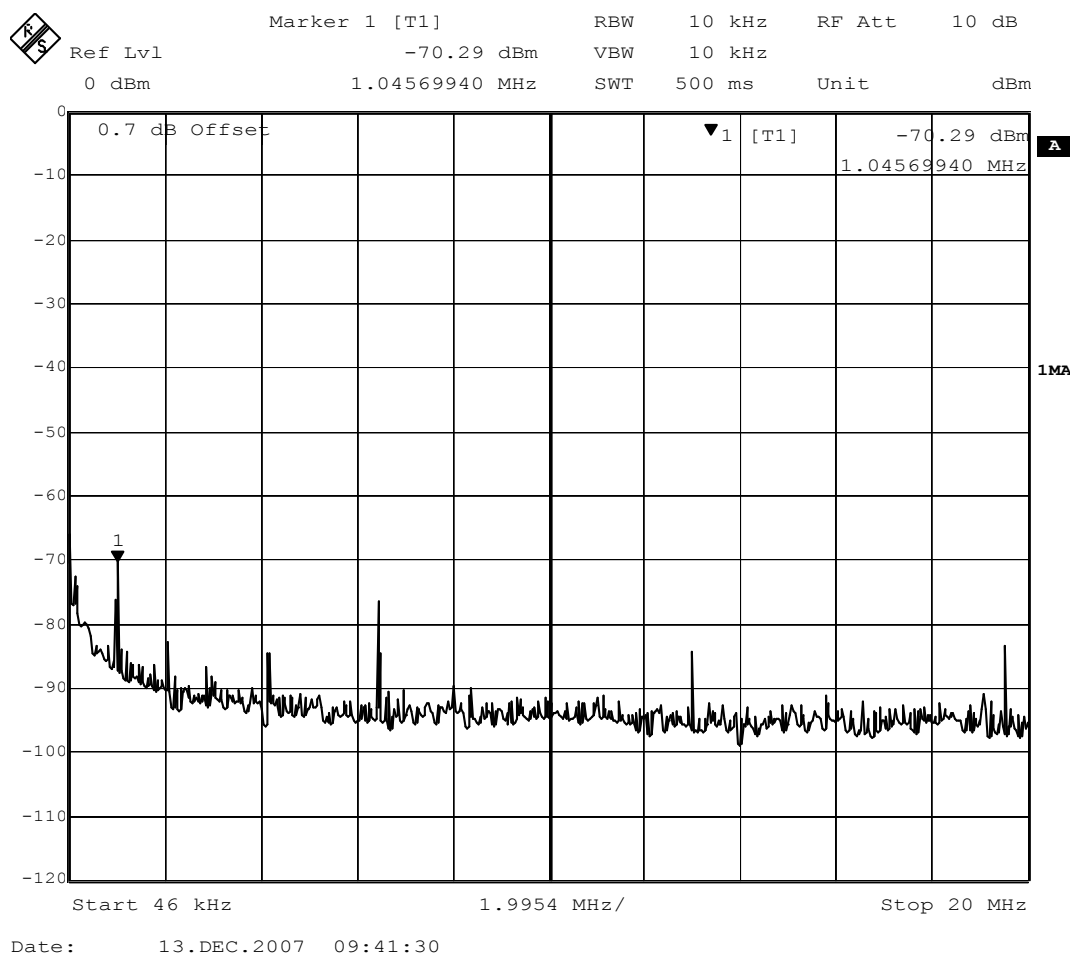

Figure 5. Switcher Power Supply Spectrum Near RFX300-30 on Power Supply Lines

3.4   Possible Issue

ADCs use the same PLL as the switcher and then, conversion time depends of PLL frequency. Table 3 gives the conversion time:

Table 3. Switching Mode Setup

Measure	Value	Minimum	Typical	Maximum	Units
Conversion Time per channel	PLLX[2.0]=000	–	–	12.0	µs
	PLLX[2.0]=100	–	–	10.5	µs
	PLLX[2.0]=111	–	–	9.6	µs

Delta conversion times are very small +1.5 to -2.1 µs and negligible for typical ADC applications (temp sensor, current drain and voltage measurement).

4 MC13783 Recommendations to Improve the 2G Transmission Output RF Modulation Spectrum

4.1 Principles of Output RF Modulation Spectrum Specification

In 2G transmission, two kinds of spectra are measured and specified, because of the 'bursty' nature of the signal:

- spectrum due to power ramping up and down (switching spectrum)
- spectrum due to modulation process (modulation spectrum)

The modulation spectrum is measured at the spectrum analyzer with zero frequency scan, filter bandwidth and video bandwidth of 30 kHz from 100 kHz to 1800 kHz below and above the carrier, with averaging done over 50% to 90% of the useful part of the burst (excluding midamble) and then averaged over 50 or 200 such burst measurements.

The switching spectrum is measured at the spectrum analyzer with zero frequency scan, filter bandwidth of 30 kHz and video bandwidth of 100 kHz from 400 kHz to 1800 kHz below and above the carrier, in peak hold mode.

Modulation spectrum specifications are the most difficult to meet with regards to the impact of spurious emissions.

Table 4, Table 5, and Table 6 give the 3GPP Modulation Spectrum specifications:

Table 4. GSM 900 and GSM 850 Modulation ORFS 3GPP Specification (05.05)

Power Level	Power Levels in dB Relative to the Measurement at FT				
	Frequency Offset (kHz)				
(dBm)	0-100	200	250	400	600 to <1800
39	+0.5	-30	-33	-60	-66
37	+0.5	-30	-33	-60	-64
35	+0.5	-30	-33	-60	-62
≤33	+0.5	-30	-33	-60	-60
The values above are subject to the minimum absolute levels (dBm) below.					
	-36	-36	-36	-36	-51

Table 5. DCS 1 800 Modulation ORFS 3GPP Specification (05.05)

Power Level	Power Levels in dB Relative to the Measurement at FT				
	Frequency Offset (kHz)				
(dBm)	0-100	200	250	400	600 to <1800
≤36	+0.5	-30	-33	-60	-60
The values above are subject to the minimum absolute levels (dBm) below.					
	-36	-36	-36	-36	-56

Table 6. PCS 1 900 Modulation ORFS 3GPP Specification (05.05)

Power Level	Power Levels in dB Relative to the Measurement at FT					
	Frequency Offset (kHz)					
(dBm)	0-100	200	250	400	600 to <1200	1200 to <1800
≤33	+0.5	-30	-33	-60	-60	-60
The values above are subject to the minimum absolute levels (dBm) below.						
	-36	-36	-36	-36	-56	-56

Modulation spectrum at the offset of ±0.8 MHz to ±1.2 MHz will then be degraded when using MC13783 buck switchers.

5 Optimization of PLLX Frequency Regarding Output RF Modulation Spectrum

Output RF modulation measurements on different hardware (Daughter Card and portable) show that the impact of switcher pollution was more significant in a portable environment due to higher integration. Because of this, measurements obtained in a portable environment are presented in Table 7 for most critical power levels (mid power in this case) and without any shield on RFX300-30 and MC13783 parts.

The default frequency used by the MC13783 to control switchers is 1.048 576 MHz (PLLX=4). PWM mode with No Pulse skipping is used (no significant improvements seen with Pulse Skipping enabled).

Figure 6 shows our hardware following Modulation ORFS for a mid-power GMSK Band 850 (ARFCN 128) burst. This spectrum shows -61.9 dBc of Modulation ORFS, which gives only a 1 dB margin with the 3GPP specification (51 dBm).

MODORFS have been measured for each PLLX frequency that can be programmed. Table 7 shows the max level measured at offsets of ±1 MHz or ±1.2 MHz.
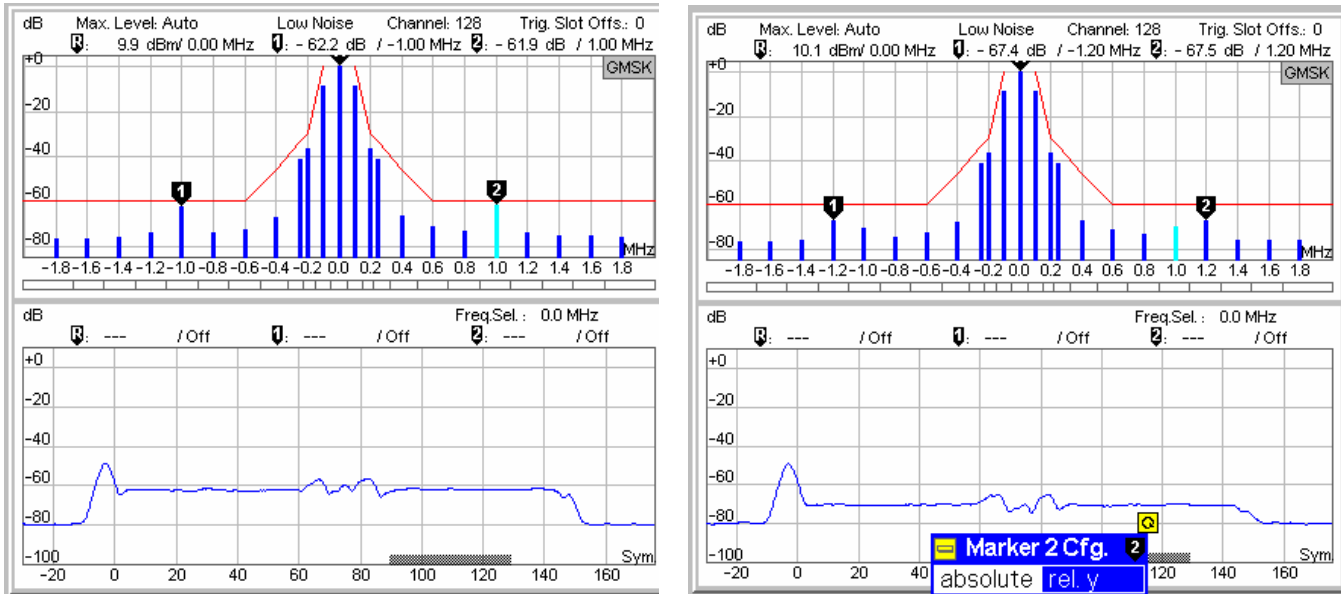
Figure 6. Output RF Modulation Spectrum with Default PLLX Frequency (1.048 576 MHz) and Optimized Frequency (1 114 112 MHz) (P2C - Board n°158 Python 2.1 Falcon 2.1)

Table 7. MODORFS @±1MHz or ±1.2MHz with PLLX Frequency Variation (P2C - Board n°158 Python 2.1 Falcon 2.1)

Frequency (Hz)	PLLX[2:0]	MODORFS @-1MHz (dBc)	MODORFS @-1MHz (dBc)	MODORFS @-1.2MHz (dBm)	MODORFS @-1.2MHz (dBm)
917 504	000	-65.2	-65.1	–	–
950 272	001	-61.3	-61.1	–	–
983 040	010	-59.8	-59.7	–	–
1 015 808	011	-60.4	-60.3	–	–
1 048 576	100	-62.2	-61.9	–	–
1 081 344	101	-66.7	-66.7	–	–
1 114 112	110	–	–	-67.4	-67.5
1 146 880	111	–	–	-63.7	-64.1

Lowest MODORFS levels are obtained at a frequency of 1 114 112 Hz, which enables a 5.5 dB improvement (Table 7). This is because this frequency maximizes the interval to the nearest frequency offset (±1.2 MHz), which is 85 888 Hz. On an identical hardware version used with shields, we were able to see 3 dB improvements, which indicate that some of pollution is caused by radiated emissions.

In order to ensure an optimum Modulation Spectrum and to pass 3GPP and customer specifications in all conditions, our recommendation is to use PLLX=6 setting to minimize the impact of signal pollution caused by MC13873 switchers.

6 Revision History

Table 8 summarizes revisions to this document.

Table 8. Revision History

Location	Revision
	This is the initial release of this document

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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
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Chaoyang District
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China
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