Freescale Semiconductor
Application Note

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MPC8548E PowerQUICC III Family Bring-Up Guide

This document provides recommendations for new designs based on the MPC8548E PowerQUICC™ III family of integrated host communications processors (collectively referred to throughout this document as MPC8548E):

- MPC8548E
- MPC8548
- MPC8547E
- MPC8545E
- MPC8545
- MPC8543E
- MPC8543

This document may also be useful in debugging newly designed systems by highlighting those aspects of a design that merit special attention during initial system startup.

For updates to this document, refer to the website listed on the back cover of this document.

Contents

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1 Introduction

This section outlines recommendations to simplify the first phase of design. Before designing a system with an MPC8548E device, it is recommended that the designer be familiar with the available documentation, software, models, and tools.

1.1 References

Some references listed here may be available only under a non-disclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

- Collateral
  - *MPC8548E PowerQUICC III™ Integrated Host Processor Family Reference Manual* (MPC8548ERM)
  - *Errata to MPC8548E PowerQUICC™ III Integrated Host Processor Family Reference Manual* (MPC8548ERMAD)
  - *Device Errata for the MPC8548E PowerQUICC™ III* (MPC8548ECE)
  - *MPC8548E PowerQUICC III™ Integrated Processor Hardware Specifications* (MPC8548EEC)
- Tools
  - Boot sequencer generator tool
  - UPM Programming tool
- Models
  - IBIS
  - BSDL

1.2 Device Errata

The device errata document describes the latest fixes and work arounds for the MPC8548E. The errata document should be thoroughly researched prior to starting a design with the respective MPC8548E device.

1.3 Boot Sequencer Tool

The MPC8548E features the boot sequencer to allow configuration of any memory-mapped register before the completion of power-on reset (POR). The register data to be changed is stored in an I^2C EEPROM. The MPC8548E requires a particular data format for register changes as outlined in the MPC8548ERM. The boot sequencer tool is a C-code file. When compiled and given a sample data file, it generates the appropriate raw data format as outlined in the MPC8548ERM (that is, an s-record file that can be used to program the EEPROM).

1.4 UPM Programming Tool

The UPM programming tool features a GUI for a user-friendly programming interface. It allows programming of all three of the MPC8548E's UPM machines. The GUI consists of a wave editor, a table editor, and a report generator. The user can edit the waveform directly or the RAM array directly. At the end of programming, the report generator prints out the UPM RAM array that can be used in a C-program.

1.5 Available Training

Our third-party partners are part of an extensive Design Alliance Program. The current training partners can be found on our website under Design Alliance Program.

Training material from past Smart Network Developer's Forums and Freescale Technology Forums are also available. These trainings modules are a valuable resource in understanding the MPC8548E. This material is also available at our website listed on the back cover of this document.

1.6 Product Revisions

Table 1 lists the processor version register (PVR) and system version register (SVR) values for the various MPC8548E derivatives of silicon.

Table 1. MPC8548E PowerQUICC III Product Revisions

Silicon Version	Device Number	Core Revision	Processor Version Register (PVR) Value	System Version Register (SVR) Value
Ver. 2.0	MPC8548	Rev. 2.0	0x8021_0020	0x8031_0020
	MPC8548E			0x8039_0020
	MPC8547E			0x8039_0120
	MPC8545			0x8031_0220
	MPC8545E			0x8039_0220
	MPC8543			0x8032_0020
	MPC8543E			0x803A_0020
Ver. 2.1	MPC8548	Rev. 2.2	0x8021_0022	0x8031_0021
	MPC8548E			0x8039_0021
	MPC8547E			0x8039_0121
	MPC8545			0x8031_0221
	MPC8545E			0x8039_0221
	MPC8543			0x8032_0021
	MPC8543E			0x803A_0021

2 Power

This section provides design considerations for the MPC8548E power supplies, as well as power sequencing. For information on AC and DC electrical specifications and thermal characteristics for the MPC8548E, refer to the MPC8548E Hardware Specification (MPC8548EEC).

2.1 Power Supplies

The MPC8548E has a core voltage V_{DD} and SerDes voltages SV_{DD} and XV_{DD}, which operate at a lower voltage than the I/O voltages BV_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, and TV_{DD}. It is recommended that the core voltage V_{DD} of MPC8548E be supplied through a variable switching supply or regulator to allow for future compatibility with possible core voltage changes on future silicon revisions. The core voltage, 1.1 V (±5%), is supplied across V_{DD} and GND.

The I/O blocks of the MPC8548E are supplied with the following:

- 2.5 V (±5%) or 3.3 V (±5%) across BV_{DD} and GND
- 1.8 V (±5%) or 2.5 V (±5%) across GV_{DD} and GND
- 2.5 V (±5%) or 3.3 V (±5%) across LV_{DD} and GND
- 3.3 V (±5%) across OV_{DD} and GND
- 1.1 V (±5%) across SV_{DD} and GND
- 2.5 V (±5%) or 3.3 V (±5%) across TV_{DD} and GND
- 1.1 V (±5%) across XV_{DD} and GND

Typically, these are supplied by simple linear regulators. This increases the complexity of the system because multiple voltage supplies and PCB power planes are required for the design.

Both LV_{DD} and TV_{DD} are used to supply the eTSEC interfaces on the device; LV_{DD} manages eTSEC1 and eTSEC2, and TV_{DD} manages eTSEC3 and eTSEC4. For the respective eTSEC, LV_{DD}/TV_{DD} must be the following:

- 3.3 V for GMII, MII, RMII, or TBI modes of operation
- 2.5 V for GMII, RGMII, RTBI, or FIFO modes of operation

NOTE

As a result, 3.3 V and 2.5 V modes cannot be paired on eTSECs powered by the same I/O supply on the MPC8548E.

2.2 Power Consumption

Operating-mode power dissipation numbers (TYPICAL) are provided in the MPC8548E Hardware Specification (MPC8548EEC). Two TYPICAL numbers are provided, one at 65 °C and one at 105 °C, to assist in the thermal design for the device. If the targeted junction temperature (T_J) of the MPC8548E in the system is not one of these two temperatures, a linear extrapolation of these two TYPICAL dissipation values can be used to estimate the power dissipation at the targeted junction temperature.

The MAXIMUM number, provided at 105 °C, is intended to assist in the power supply design selection.

A low-power SLEEP mode dissipation (at 65 °C) is also provided for applications concerned about minimizing power consumption when the MPC8548E is not active.

NOTE

The SLEEP, TYPICAL, and MAXIMUM power numbers are based on the power dissipation on the 1.1 V nominal V_{DD} supply only. Typical power dissipation estimates on the peripheral supplies (BV_{DD}, GV_{DD}, LV_{DD}, OV_{DD}, TV_{DD}, and XV_{DD}) are provided in the MPC8548EEC document.

2.3 I/O Power Dissipation

I/O usage varies from design to design. Table 2 provides power dissipation estimates for the I/O supplies.

Table 2. Estimated I/O Power Dissipation

Interface	Parameters	1.1 V (XV_{DD})	1.8 V (GV_{DD})	2.5 V ($B/G/LV_{DD}$)	3.3 V ($B/L/OV_{DD}$)	Comments
DDR	266 MHz data	—	0.31 W	0.59W	—	—
	333 MHz data	—	0.38 W	0.73W	—	
	400 MHz data		0.46 W			
	533 MHz data	—	0.60 W	—	—	
PCI Express	x8, 2.5 G-baud	0.71 W	—	—	—	—
Serial RapidIO	x4, 2.5 G-baud	0.49 W	—	—	—	—
PCI Express	64-bit, 133 MHz	—	—	—	0.25 W	—
PCI	64-bit, 66 MHz	—	—	—	0.14 W	Power per PCI port
	64-bit, 66 MHz	—	—	—	0.08 W	
	32-bit, 66 MHz	—	—	—	0.07 W	
	32-bit, 33 MHz	—	—	—	0.04 W	
Local bus	32-bit, 133 MHz	—	—	0.14 W	0.24 W	—
	32-bit, 66 MHz	—	—	0.07 W	0.13 W	
	32-bit, 33 MHz	—	—	0.04 W	0.07 W	
eTSEC (10/100/1000 Ethernet)	MII	—	—	—	0.01 W	Power per eTSEC used
	GMII	—	—	—	0.07 W	
	TBI	—	—	—	0.07 W	
	RGMII	—	—	0.04 W	—	
	RTBI	—	—	0.04 W	—	
eTSEC (packet FIFO)	8-bit, 200 MHz	—	—	0.11 W	—	Power per FIFO interface used
	8-bit, 155 MHz	—	—	0.08 W	—	

2.4 Power Sequencing

The device requires its power rails to be applied in a specific sequence to ensure proper device operation. These requirements per the MPC8548EEC document are as follows for power-up:

1. V_{DD}, AV_{DD}_n, BV_{DD}, LV_{DD}, OV_{DD}, SV_{DD}, TV_{DD}, XV_{DD}
2. GV_{DD}

All supplies must be at their stable values within 50 ms.

The purpose of the sequence is to guarantee the state of the DDR signals at reset. In order to guarantee MCKE low during power-up (as should be *attempted* per the JEDEC JESD79-2C specification), the above sequencing for GV_{DD} is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing of GV_{DD} is not required.

From a system standpoint, if any of the I/O power supplies ramp prior to the V_{DD} core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn by the device.

2.5 PLL Power Supply Filtering

Each of the PLLs on the MPC8548E is provided with power through independent power supply pins (AV_{DD}_PLAT, AV_{DD}_CORE, AV_{DD}_PCI, AV_{DD}_LBIU, and AV_{DD}_SRDS, respectively). Ideally, these voltages are derived directly from V_{DD} through a low-frequency filter scheme.

While there are a number of ways to reliably provide power to the PLLs, the recommended solution is to provide independent filter circuits per PLL power supply as illustrated in Figure 1, Figure 2, and Figure 3, one to each of the AV_{DD} pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLLs resonant frequency range from a 500-kHz to 10-MHz range. If the PCI is run in synchronous mode, no filter is required for AV_{DD}_PCI.

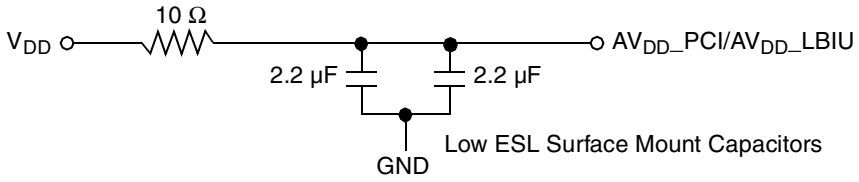


Figure 1. PLL Power Supply Filter Circuit with PCI/LBIU Pins

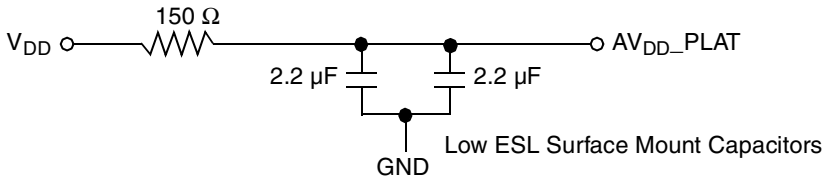


Figure 2. PLL Power Supply Filter Circuit with PLAT Pins

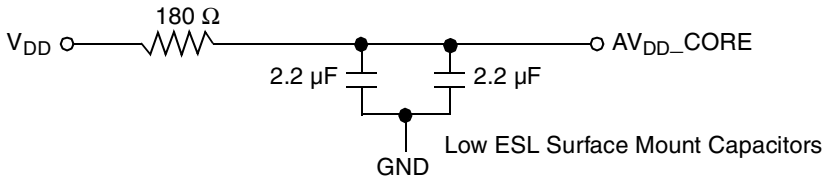
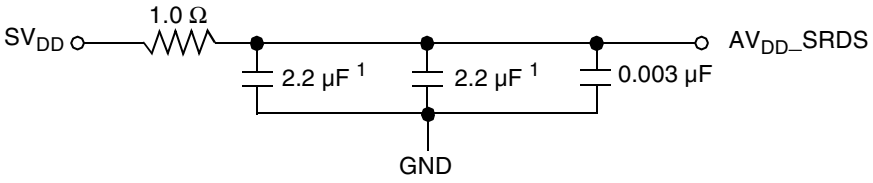


Figure 3. PLL Power Supply Filter Circuit with CORE Pins

The AV_{DD}_SRDS signal provides power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in Figure 4. If the SerDes is not used, a filter for AV_{DD}_SRDS is not required.



1. An 0805 sized capacitor is recommended for system initial bring-up.

Figure 4. SerDes PLL Power Supply Filter

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits.

These filters are a necessary extension of the PLL circuitry and are to what the device is specified. Any deviation from the recommended filters are done at the customer's risk (unless specified by Freescale).

2.6 Power Supply Decoupling

The MPC8548E requires a clean, tightly regulated source of power. The system designer should place at least one decoupling capacitor at each V_{DD} and B/G/L/O/TV_{DD} pin of the device. These decoupling capacitors should have a value of 0.1 µF and receive their power from separate V_{DD}, B/G/L/O/TV_{DD}, and GND power planes in the PCB, utilizing short traces to minimize inductance.

In addition, several bulk storage capacitors should be distributed around the PCB to feed the V_{DD} and B/G/L/O/TV_{DD} planes to enable quick recharging of the smaller chip capacitors.

The capacitors should be placed as close as possible to the MPC8548E processor. The capacitors need to be selected to work well with the power supply so they can handle the dynamic load requirements of the MPC8548E. For good, clean power supplied to the MPC8548E, the customer should work closely with their power-supply vendor to choose the correct value and type of capacitors.

If the SerDes is used, it requires a clean, tightly regulated source of power (SV_{DD} and XV_{DD}) to ensure low jitter on transmit and reliable recovery of data in the receiver:

- The board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device.
- There should be a 1-µF ceramic chip capacitor from each SerDes supply (SV_{DD} and XV_{DD}) to the board ground plane on each side of the device.

- Between the device and any SerDes voltage regulator should be a 10-µF, low ESR SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

2.7 Power Supplies Checklist

Table 3 provides a summary MPC8548E power supply checklist for the designer.

Table 3. Power Supplies Checklist

Item	Description	Completed
1	All power supplies have a voltage tolerance no greater than 5% from the nominal value.	
2	eTSEC supplies are chosen according to the mode of operation used.	
3	Power supply selected is based on MAXIMUM power dissipation.	
4	Thermal design is based on TYPICAL power dissipation.	
5	Power-up sequence is less than 50 ms.	
6	Power sequencing is understood and based on whether or not latch-up or garbage data written to DDR is a concern	
7	Recommended PLL filter circuit is applied to AV_{DD}_PLAT, AV_{DD}_CORE, and AV_{DD}_LBIU.	
8	If PCI is used in asynchronous mode, then the recommended PLL filter circuit is applied to AV_{DD}_PCI.	
9	If SerDes is used, then the recommended PLL filter circuit is applied to AV_{DD}_SRDS.	
10	PLL filter circuits are placed as close to the respective AV_{DD} pin as possible.	
11	Decoupling capacitors of 0.1 µF are placed at each V_{DD}, B/G/L/O/TV_{DD} pin.	
12	Bulk capacitors are placed on each V_{DD}, B/G/L/O/TV_{DD} plane.	
13	If SerDes is used, the recommended decoupling for S/XV_{DD} is used.	

3 Power-On Reset and Reset Configurations

This section provides information about reset configurations.

3.1 Configuration and Timing

Various device functions are initialized by sampling certain signals during the assertion of $\overline{\text{HRESET}}$. These power-on reset (POR) inputs are either pulled high or low during this period. While these pins are generally output pins during normal operation, they are treated as inputs while $\overline{\text{HRESET}}$ is asserted. $\overline{\text{HRESET}}$ must be asserted for a minimum on 100 µs. When $\overline{\text{HRESET}}$ de-asserts, the configuration pins are sampled and latched into registers, and the pins then take on their normal output circuit characteristics.

Most of the configuration pins have an internally gated 20-kΩ pull-up resistor, enabled only during $\overline{\text{HRESET}}$. For those configurations in which the default state is desired, no external pull-up is required. Otherwise, a 4.7-kΩ pull-down resistor is recommended to pull the configuration pin to a valid logic low level. In the case where a configuration pin has no default, 4.7-kΩ pull-up or pull-down resistors are recommended for appropriate configuration of the pin.

An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device which drives the configuration signals to the MPC8548E when HRESET is asserted. The PLD must begin to drive these signals at least 4 SYSCLK cycles prior to the de-assertion of HRESET (PLL configuration inputs must meet a 100-µs set-up time to HRESET), hold their values for at least 2 SYSCLK cycles after the de-assertion of HRESET, and then release the pins to high impedance afterward for normal device operation.

3.2 Configuration Settings

Table 4 summarizes the customer-configurable device settings for the MPC8548E. Refer to the MPC8548ERM for a more detailed description of each configuration option.

Table 4. User Configuration Options

Configuration Type	Functional Pins	Comments
MPC8548E Derivative	DMA_DACK[0:1]	There is no default value for this family device selection; these signals must be pulled to the desired value. **Note:** A family derivative with features not supported is not guaranteed to function if reconfigured as a fully featured derivative. For more information, see Table 5.
CCB Clock PLL Ratio	LA[28:31]	There is no default value for this PLL ratio; these signals must be pulled to the desired value
e500 Core PLL Ratio	LBCTL, LALE, LGPL2	There is no default value for this PLL ratio; these signals must be pulled to the desired value
Boot ROM Location	TSEC1_TXD[6:4]	Default: Local Bus GPCM (32-bit ROM)
Host/Agent	LWE[1:3]	Default: MPC8548E acts as the host processor/root complex
I/O Port Selection	TSEC1_TXD[3:1]	Default: PCI Express x8 (2.5 Gbps); 100-MHz reference clock
CPU Boot	LA27	Default: e500 core is allowed to boot without waiting for configuration by an external master.
Boot Sequencer	LGPL3, LGPL5	Default: Boot sequencer is disabled.
DDR DRAM Type	TSEC2_TXD1, TSEC2_TX_ER	Default: DDR controller is configured for DDR2
eTSEC1/2 Width	EC_MDC	Default: eTSEC1 and eTSEC2 Ethernet interfaces operate in their standard width TBI, GMII, MII. Or, if eTSEC1 is in FIFO mode, it operates as a 16-bit FIFO. eTSEC2 FIFO width is 8 bits regardless of this configuration setting.
eTSEC3/4 Width	TSEC3_TXD2	Default: eTSEC3 Ethernet interface operates in standard TBI, GMII, MII, or 8-bit FIFO mode. eTSEC 4 is unavailable.
eTSEC1 Protocol	TSEC1_TXD0, TSEC1_TXD7	Default: The eTSEC1 controller operates using the TBI protocol (or RTBI if configured in reduced mode).
eTSEC2 Protocol	TSEC2_TXD0, TSEC2_TXD7	Default: The eTSEC2 controller operates using the TBI protocol (or RTBI if configured in reduced mode).
eTSEC3 Protocol	TSEC3_TXD0, TSEC3_TXD1	Default: The eTSEC3 controller operates using the TBI protocol (or RTBI if configured in reduced mode).

Table 4. User Configuration Options (continued)

Configuration Type	Functional Pins	Comments
eTSEC4 Protocol	TSEC4_TXD0, TSEC4_TXD1	Default: The eTSEC4 controller operates using the RTBI protocol.
RapidIO® Device ID	TSEC2_TXD[2:4]	Default: Device ID[5:7] default to 1s.
RapidIO System Size	LGPL0	Default: Small system size (up to 256 devices).
PCI1 Clock Select	$\overline{\text{PCI2\_GNT3}}$	Default: Synchronous mode. SYSCLK is used as the clock for the PCI1/PCI Express interface.
PCI2 Clock Select	$\overline{\text{PCI2\_GNT4}}$	Default: Synchronous mode. SYSCLK is used as the clock for the PCI2 interface.
PCI1 Speed Configuration	LWE0	Default: PCI frequency above 33 MHz or PCI Express frequency above 66 MHz.
PCI2 Speed Configuration	LGPL1	Default: PCI frequency above 33 MHz.
PCI Bus Width	$\overline{\text{PCI1\_REQ64}}$	Default: The PCI1/PCI Express interface operates as a 32-bit interface.
PCI1 I/O Impedance	$\overline{\text{PCI1\_GNT1}}$	Default: 42-Ω I/O drivers are used on the PCI1/PCI Express interface.
PCI2 I/O Impedance	$\overline{\text{PCI2\_GNT1}}$	Default: 42-Ω I/O drivers are used on the PCI2 interface.
PCI1/PCI Express Arbiter	$\overline{\text{PCI1\_GNT2}}$	Default: The on-chip PCI1/PCI Express arbiter is enabled.
PCI2 Arbiter	$\overline{\text{PCI2\_GNT2}}$	Default: The on-chip PCI2 arbiter is enabled.
PCI Debug Configuration	$\overline{\text{PCI1\_GNT3}}$	Default: PCI operates in normal mode.
PCI Express Configuration	$\overline{\text{PCI1\_GNT4}}$	Default: Interface operates in PCI mode.
Memory Debug	MSRCID0	Default: Debug information from the DDR SDRAM controller is driven on the MSRCID and MDVAL signals.
DDR Debug	MSRCID1	Default: Debug information is not driven on ECC pins. ECC pins function in their normal mode.
SerDes Enable	TSEC4_TXD2	Default: SerDes interface is enabled.
General Purpose POR Configuration	LAD[0:31]	There is no default value for this general purpose POR.

Table 5 shows the derivatives of the MPC8548E.

Table 5. MPC8548E Derivatives

Part Number	SVR	DMA_DACK_B[0:1]	Test_Sel
MPC8548E with Security	803_9_00_20	‘b11	1
MPC8548 without Security	803_1_00_20	‘b11	1
MPC8547 (always with Security)	803_9_01_20	‘b01	1
MP8545E with Security	803_9_02_20	‘b10	1
MPC8545 without Security	803_1_02_20	‘b10	1

Table 5. MPC8548E Derivatives (continued)

Part Number	SVR	DMA_DACK_B[0:1]	Test_Sel
MPC8543E with Security	803_A_00_20	‘b11	0
MPC8543 without Security	803_2_00_20	‘b11	0

3.3 Internal Test Modes

Several pins double as test mode enables. These test modes are for internal use only. If enabled during reset, they may result in the MPC8548E not coming out of reset. Table 6 lists these pins and how they should be addressed during the reset sequence.

Table 6. Internal Test Mode Pins

Pin Group	Pins	Guideline for Reset
Debug	TRIG_OUT/READY	Since these pins have an internal pull-up enabled only at reset, they may be left floating if unconnected. Otherwise, they may need to be driven high (that is, by a PLD), if the device to which they are connected does not release these pins to high impedance during reset.
	MSRCID2	
	MSRCID3	
	MSRCID4	
Design For Test	LSSD_MODE	These pins must be pulled to OV_{DD} via a 100 Ω–1 kΩ resistor.
	L1_TSTCLK	—
	L2_TSTCLK	
	TEST_SEL	These pins must be pulled up or down at time of reset according to Table 5.
eTSEC	TSEC2_TXD5	Since these pins have an internal pull-up enabled only at reset, they may be left floating if unconnected. Otherwise, they may need to be driven high (that is, by a PLD), if the device to which they are connected does not release these pins to high impedance during reset.
	TSEC2_TXD6	
	TSEC3_TXD3	
	TSEC3_TXD7/ TSEC4_TXD3	
Power Management	ASLEEP	
System Control	$\overline{\text{HRESET\_REQ}}$	

3.4 Reset Checklist

Table 7 provides a summary MPC8548E POR and reset checklist for the designer.

Table 7. Checklist for POR and Reset Configurations

Item	Description	Completed
1	$\overline{\text{HRESET}}$ is asserted for a minimum of 100 μs.	
2	$\overline{\text{DMA\_DACK}}$[0:1] are configured to select the appropriate MPC8548E family derivative.	

Table 7. Checklist for POR and Reset Configurations (continued)

Item	Description	Completed
3	Configuration pins are either appropriately tied-off with a 4.7-kΩ resistor, or driven by an external device (meeting their required setup and hold times).	
4	PLL configurations are defined and meet the required set-up and hold times.	
5	Internal test mode pins are guaranteed not to be low during reset.	

4 Device Pins

This section provides the recommended test points and a device pin map.

4.1 Recommended Test Points

For easier debug, it is recommended that the test points on the board include the following pins:

- CLK_OUT (helps verify the CCB clock)
- TRIG_OUT (helps verify the end of the reset sequence)
- ASLEEP (helps verify the end of the reset sequence)
- SENSEVDD (helps verify power plane VDD)
- SENSEVSS (helps verify ground plane VSS)
- HRESET_REQ (helps verify proper boot sequencer functions and reset requests)

4.2 Pin Map

Figure 5 provides a bottom view of the pin map of the device.

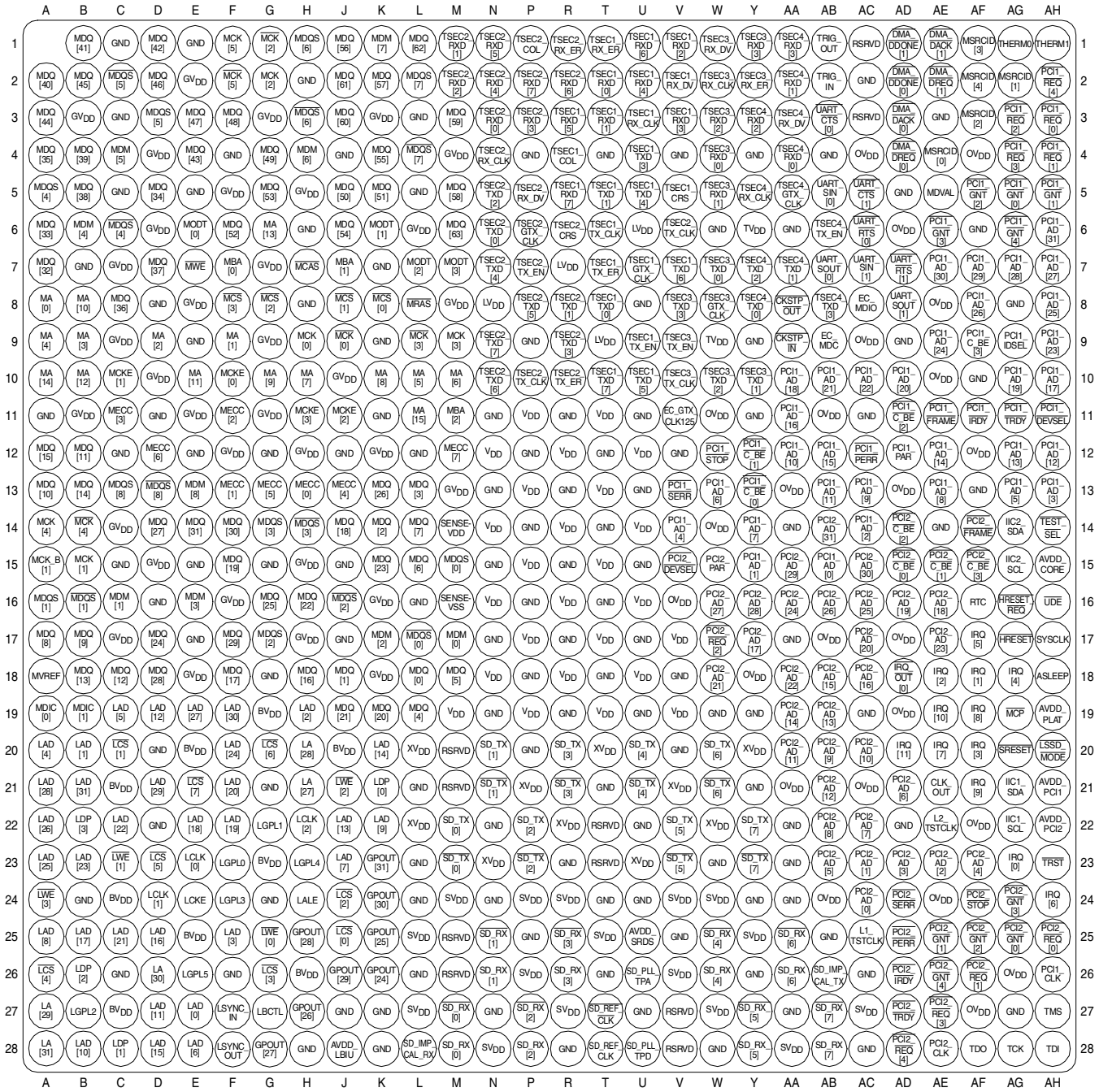


Figure 5. MPC8548E Ball Map

5 Clocks

The clock inputs for the MPC8548E are the EC_GTX_CLK125, PCI1_CLK, PCI2_CLK, RTC, SD_REF_CLK, and SYSCLK. The EC_GTX_CLK125 input is used by the eTSEC controller as a reference clock for gigabit Ethernet modes. The PCI1_CLK and PCI2_CLK inputs are PCI clock inputs if the PCI controllers are configured in asynchronous mode. SD_REF_CLK is the reference clock for PCI Express and/or SRIO operating modes. SYSCLK is the primary clock input to the device. Table 8 shows how the clock pins should be connected.

Table 8. Clock Pin Recommendations

Pin	Pin Used	Pin Not Used
EC_GTX_CLK125	If any of the eTSECs are used in gigabit mode, connect to a 125-MHz clock.	Pull high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively.
PCI1_CLK	If PCI1 is configured for PCI and asychronous mode, connect to a 16–66 MHz clock. If PCI1 is configured for PCI Express and asychronous mode, connect to a 66–133 MHz clock.	Pull high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
PCI2_CLK	If PCI2 is configured for asychronous mode, connect to a 16–66 MHz clock.	Pull high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
RTC	If used, connect to a clock that runs no greater than 1/4 the platform CCB_clk.	Pull high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
SD_REF_CLK / $\overline{\text{SD\_REF\_CLK}}$	If the SerDes is enabled at POR, connect to a clock at the frequency specified per the POR I/O Port Selection.	These pins must be connected to GND.
SYSCLK	This must always be connected to an input clock of 16–133 MHz.	

6 DDR Interface

This section discusses the termination of DDR pins on the device.

NOTE

Disable the clocks that are not used via the DDRCLKDR register. By default, all clocks are operational, but not all clock signals are used in a given application. Therefore, by disabling the unused clocks, it first lowers the power consumption and then lowers the unused switching activity in the part. DDRCLKDR is not a part of the memory controller register set; it is located in the global utility register section.

Table 9 shows how the DDR pins should be connected.

Table 9. DDR Pin Recommendations

Pin	Pin Used	Pin Not Used
MA[0:15]	Auto-precharge for DDR signaled on A10 when DDR_SDRAM_CFG[PCHB8] = 0. Auto-precharge for DDR signaled on A8 when DDR_SDRAM_CFG[PCHB8] = 1.	These pins may be left unconnected.
MBA[0:2]	—	
$\overline{\text{MCAS}}$	—	
MCK/$\overline{\text{MCK}}$[0:5]	—	
MCKE[0:3]	These pin may not be driven low at assertion of $\overline{\text{HRESET}}$. See MCP8548ECE DDR 20 for more information.	
$\overline{\text{MCS}}$[0:3]	—	
MDIC[0:1]	MDIC0 is grounded through an 18.2-Ω precision 1% resistor and MDIC1 is connected to GV_{DD} through an 18.2-Ω precision 1% resistor. These pins are used for automatic calibration of the DDR I/Os.	
MDM[0:8]	—	These pins may be left unconnected.
MDQ[0:63]	—	
MDQS[0:8] / $\overline{\text{MDQS}}$[0:8]	—	
MECC[0:7]	—	These pins should be pulled high or low via a 2–10 kΩ resistor.
MODT[0:3]	—	These pins may be left unconnected.
$\overline{\text{MRAS}}$	—	
$\overline{\text{MWE}}$	—	

7 Debug and Test Interface

This section discusses the termination of Debug and Test pins on the device. Table 10 shows how the debug and test pins should be connected.

Table 10. Debug and Test Pin Recommendations

Pin	Pin Used	Pin Not Used
ASLEEP	This pin must NOT be pulled down during power-on reset.	This pin may be left unconnected.
CLK_OUT	**Note:** This output is actively driven during reset rather than being released to high impedance during reset.	This pin may be left unconnected.
MDVAL	—	This pin must be left unconnected.

Table 10. Debug and Test Pin Recommendations (continued)

Pin	Pin Used	Pin Not Used
L1_TSTCLK	These signals must be pulled up via a 100–1000 Ω resistor to OV_{DD} for normal machine operation.	
L2_TSTCLK		
LSSD_MODE		
MSRCID[0:1]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	This pin must be left unconnected.
MSRCID[2:4]	These pins must NOT be pulled down during power-on reset.	This pin must be left unconnected.
SD_IMP_CAL_RX	This pin must be pulled down through a 200-Ω resistor.	
SD_IMP_CAL_TX	This pin must be pulled down through a 100-Ω resistor.	
SD_PLL_TPA	Do not connect.	
TEST_SEL	This signal must be pulled up via a 100–1000 Ω resistor to OV_{DD} for normal machine operation.	
THERM[0:1]	—	These pins may be left unconnected.
TRIG_IN	—	Tie low through a 2–10 kΩ resistor to GND.
TRIG_OUT / READY	This pin must NOT be pulled down during power-on reset.	This pin must be left unconnected.

8 DMA Interface

This section discusses the termination of DMA pins on the device. Table 11 shows how the DMA pins should be connected.

Table 11. DMA Pin Recommendations

Pin	Pin Used	Pin Not Used
$\overline{\text{DMA\_DACK}}$[0:1]	This pin is a reset configuration pin that sets the device derivative. These pins require 4.7-kΩ pull-up or pull-down resistors.	
$\overline{\text{DMA\_DACK2}}$ / $\overline{\text{LCS6}}$	—	If the Local Bus function of this pin is not used, this output pin may be left floating.
$\overline{\text{DMA\_DACK3}}$ / IRQ10	—	Pull high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
$\overline{\text{DMA\_DREQ}}$[0:1]	—	Pull high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{DMA\_DREQ2}}$ / $\overline{\text{LCS5}}$	—	If the Local Bus function of this pin is not used, this output pin may be left floating.
$\overline{\text{DMA\_DREQ3}}$ / IRQ9	—	Pull high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.
$\overline{\text{DMA\_DDONE}}$[0:1]	—	These output pins may be left floating.

Table 11. DMA Pin Recommendations (continued)

Pin	Pin Used	Pin Not Used
$\overline{\text{DMA\_DDONE2}}$ / $\overline{\text{LCS7}}$	—	If the Local Bus function of this pin is not used, this output pin may be left floating.
$\overline{\text{DMA\_DDONE3}}$ / IRQ11	—	Pull high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.

9 DUART Interface

This section discusses the termination of DUART pins on the device. Table 12 shows how the DUART pins should be connected.

Table 12. DUART Pin Recommendations

Pin	Pin Used	Pin Not Used
$\overline{\text{UART\_CTS}}$[0:1]	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{UART\_RTS}}$[0:1]	—	These output pins may be left floating.
UART_SIN[0:1]	—	Tie low through a 2–10 kΩ resistor to GND.
UART_SOUT[0:1]	—	These output pins may be left floating.

10 Ethernet Management Interface

This section discusses the termination of the Ethernet management pins on the device. Table 13 shows how the Ethernet management pins should be connected.

Table 13. Ethernet Management Pin Recommendations

Pin	Pin Used	Pin Not Used
EC_MDC	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
EC_MDIO	—	Tie high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively.

11 eTSEC Interface

This section discusses the termination of the Ethernet pins on the device. Table 14 shows how the Ethernet pins should be connected.

Table 14. Ethernet Pin Recommendations

Pin	Pin Used	Pin Not Used
TSEC1_COL	—	Tie low through a 2–10 kΩ resistor to GND.
TSEC2_COL	—	
TSEC1_CRS	—	
TSEC2_CRS	—	
TSEC1_GTX_CLK	—	These output pins may be left floating.
TSEC2_GTX_CLK	—	
TSEC3_GTX_CLK	—	
TSEC4_GTX_CLK	—	
TSEC1_RX_CLK	—	Tie high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively
TSEC2_RX_CLK	—	
TSEC3_RX_CLK	—	Tie high or low through a 2–10 kΩ resistor to TV_{DD} or GND, respectively.
TSEC4_RX_CLK / TSEC3_COL	—	
TSEC1_RX_DV	—	Tie low through a 2–10 kΩ resistor to GND.
TSEC2_RX_DV	—	
TSEC3_RX_DV	—	
TSEC4_RX_DV / TSEC3_CRS	—	
TSEC1_RX_ER	—	
TSEC2_RX_ER	—	
TSEC3_RX_ER	—	
TSEC1_RXD[7:0]	—	Tie high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively.
TSEC2_RXD[7:0]	—	
TSEC3_RXD[3:0]	—	Tie high or low through a 2–10 kΩ resistor to TV_{DD} or GND, respectively.
TSEC4_RXD[3:0] / TSEC3_RXD[7:4]	—	
TSEC1_TX_CLK	—	Tie high or low through a 2–10 kΩ resistor to LV_{DD} or GND, respectively
TSEC2_TX_CLK	—	
TSEC3_TX_CLK	—	Tie high or low through a 2–10 kΩ resistor to TV_{DD} or GND, respectively.

Table 14. Ethernet Pin Recommendations (continued)

Pin	Pin Used	Pin Not Used
TSEC1_TX_EN	These pins require an external 4.7 kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively driven (during reset).	These output pins may be left floating.
TSEC2_TX_EN		
TSEC3_TX_EN		
TSEC4_TX_EN / TSEC3_TX_ER		
TSEC2_TX_ER	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
TSEC1_TX_ER	—	This output pin may be left floating.
TSEC1_TXD[7:0]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	These output pins may be left floating.
TSEC2_TXD[7:0]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. TSEC2_TXD1 must be valid at Power-Up.	These output pins may be left floating (with the exception of TSEC2_TXD1).
TSEC3_TXD[3:0]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. The following pins must NOT be pulled down during power-on reset: TSEC3_TXD[3] and TSEC4_TXD3/TSEC3_TXD7.	These output pins may be left floating.
TSEC4_TXD[3:0] / TSEC3_TXD[7:4]		

12 I²C Interface

This section discusses the termination of I^2C pins on the device. Table 15 shows how the I^2C pins should be connected.

Table 15. I^2C Pin Recommendations

Pin	Pin Used	Pin Not Used
IIC1_SCL	Tie these open-drain signals high through a 1-kΩ resistor to OV_{DD}.	Tie high through a 2–10 kΩ resistor to OV_{DD}.
IIC2_SCL		
IIC1_SDA		
IIC2_SDA		

13 JTAG Interface

Correct operation of the JTAG interface requires configuration of a group of system control pins as demonstrated in Figure 7. Care must be taken to ensure that these pins are maintained at a valid deasserted state under normal operating conditions as most have asynchronous behavior and spurious assertion may give unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1™ specification, but it is provided on all processors built on Power Architecture technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 7 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 6, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header; so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 6 is common to all known emulators.

13.1 Termination of Unused Signals

If the JTAG interface and COP header is not used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 7. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.
- No pull-up/pull-down is required for TDI, TMS, TDO, or TCK.

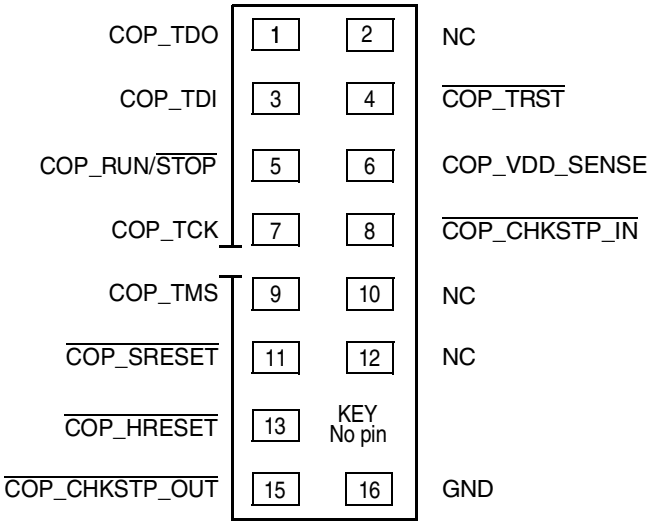
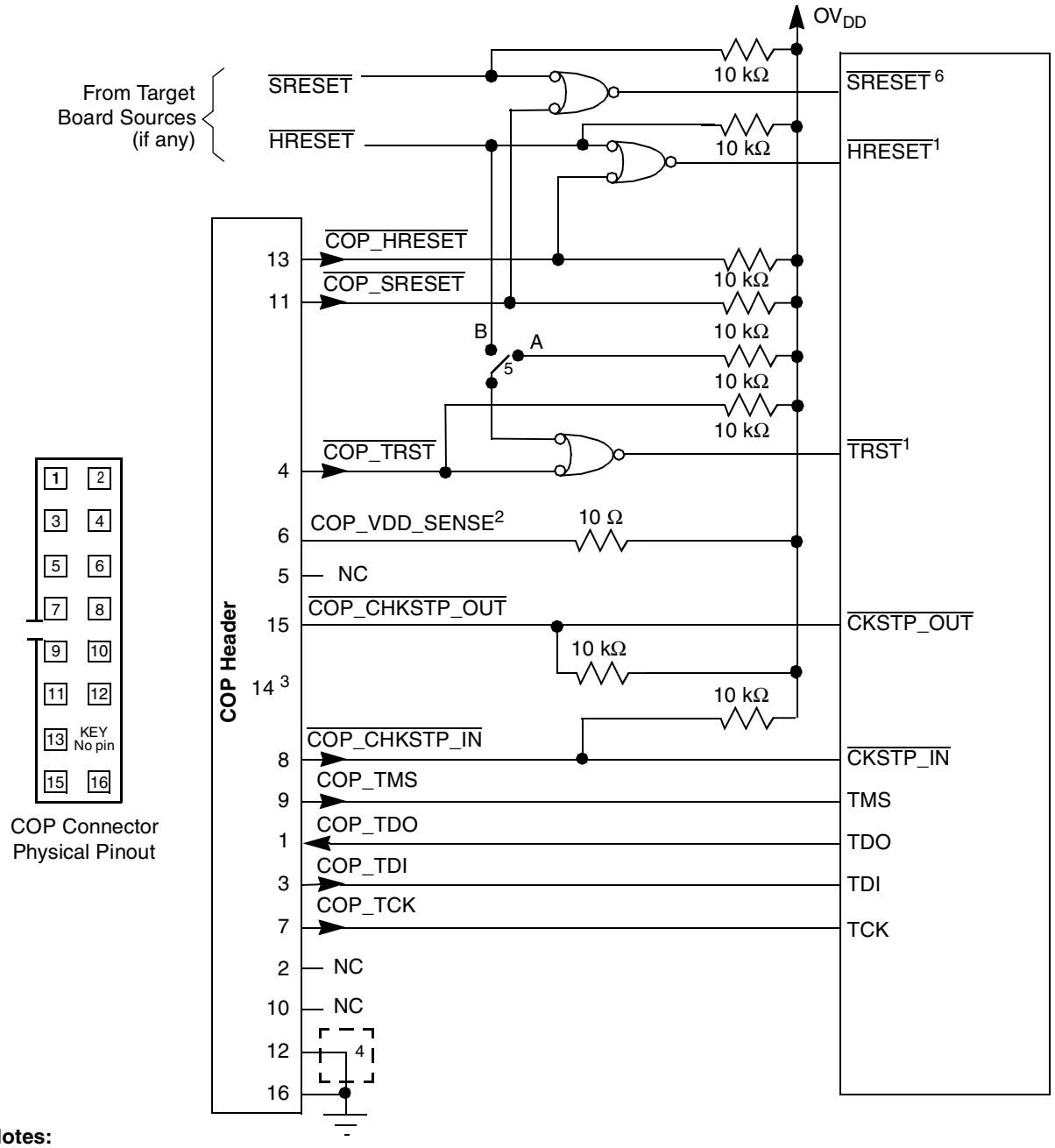


Figure 6. COP Connector Physical Pinout



Notes:

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10-Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No-Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

Figure 7. JTAG Interface Connection

13.2 JTAG Pins

Table 16 shows how the JTAG pins should be connected.

Table 16. JTAG Pin Recommendations

Pin	Pin Used	Pin Not Used
TCK	Connect to Pin7 of the COP connector	Tie high through a 2–10 kΩ resistor to OV_{DD}.
TDI	This pin has a weak internal pull-up P-FET that are always enabled. Connect to Pin3 of the COP connector	Tie high or low through a 2–10 kΩ resistor to OV_{DD} or GND.
TDO	Connect to Pin1 of the COP connector	This pin may be left unconnected.
TMS	This pin has a weak internal pull-up P-FET that are always enabled. Connect to Pin9 of the COP connector	Tie high or low through a 2–10 kΩ resistor to OV_{DD} or GND.
TRST	This pin has a weak internal pull-up P-FET that are always enabled. Connect to Pin4 of the COP connector and $\overline{\text{HRESET}}$ from the board	$\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0-Ω resistor.

13.3 JTAG Checklist

Table 17 provides a summary MPC8548E POR and reset checklist for the designer.

Table 17. Checklist for JTAG

Item	Description	Completed
1	Connect the JTAG pins to the COP header as shown in Figure 7.	

14 Local Bus Interface

This section discusses the termination of Local Bus pins on the device. Table 18 shows how the Local Bus pins should be connected.

Table 18. Local Bus Pin Recommendations

Pin	Pin Used	Pin Not Used
LA27	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LA[28:31]	This pin is a reset configuration pin that sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors.	
LAD[0:31]	Note that the LSB for the address = LAD[24:31]; however, the MSB for the data is on LAD[0:7].	Tie high or low through a 2–10 kΩ resistor to BV_{DD} or GND, respectively, if the general purpose POR configuration is not used.
LALE	This pin is a reset configuration pin that sets the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors.	
LBCTL		

Table 18. Local Bus Pin Recommendations (continued)

Pin	Pin Used	Pin Not Used
LCLK[0:2]	—	These output pins may be left floating.
LCKE	—	
$\overline{\text{LCS}}$[0:4]	—	
$\overline{\text{LCS5}}$ / $\overline{\text{DMA\_DREQ2}}$	—	If the DMA functions of these pins are not used, these output pins may be left floating.
$\overline{\text{LCS6}}$ / $\overline{\text{DMA\_DACK2}}$	—	
$\overline{\text{LCS7}}$ / $\overline{\text{DMA\_DDONE2}}$	—	
LGPL0 / LSDA10	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR defaults are acceptable, these output pins may be left floating.
LGPL1 / $\overline{\text{LSDWE}}$		
LGPL2 / $\overline{\text{LOE}}$ / $\overline{\text{LSDRAS}}$	This pin is a reset configuration pin that sets the e500 core clock to CCB Clock PLL ratio. These pins require 4.7-kΩ pull-up or pull-down resistors.	
LGPL3 / $\overline{\text{LSDCAS}}$	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LGPL4 / $\overline{\text{LGTA}}$ / LUPWAIT / LPBSE	—	This pin either needs to be pulled-up via a 2–10 kΩ resistor to BV_{DD} or needs to be reconfigured as LPBSE prior to boot-up.
LGPL5	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR default is acceptable, this output pin may be left floating.
LSYNC_IN	LSYNC_IN needs to be connected via a trace to LSYNC_OUT of length equal to the longest LCK*n* signal used.	LSYNC_IN needs to be directly connected to LSYNC_OUT.
LSYNC_OUT		
$\overline{\text{LWE0}}$ / $\overline{\text{LBS0}}$ / $\overline{\text{LSDDQM0}}$	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state.	If the POR defaults are acceptable, these output pins may be left floating.
$\overline{\text{LWE1}}$ / $\overline{\text{LBS1}}$ / $\overline{\text{LSDDQM1}}$		
$\overline{\text{LWE2}}$/ $\overline{\text{LBS2}}$ / $\overline{\text{LSDDQM2}}$		
$\overline{\text{LWE3}}$ / $\overline{\text{LBS3}}$ / $\overline{\text{LSDDQM3}}$		

15 PCI Interface

This section discusses the termination of PCI pins on the device.

15.1 Unrealized $\overline{\text{RST}}$ Pin

The MPC8548E does not implement for the PCI interface a specific RST pin separate from the rest of the device pins. Instead, the PCI $\overline{\text{RST}}$ is realized with the $\overline{\text{HRESET}}$ input.

15.2 PCI Pins

Table 19 shows how the PCI pins should be connected. Unless otherwise noted, unused inputs need be tied to their inactive state through a 2–10 kΩ resistor, and unused I/Os need be tied high or low through a 2–10 kΩ resistor to OV_{DD} and GND, respectively.

Table 19. PCI Pin Recommendations

Pin	Pin Used	Pin Not Used
PCI1_ACK64 / PCI2_DEVSEL	A weak pull-up resistor (2–10 kΩ) need be placed on this pin to OV_{DD}.	
PCI1_AD[31:0]	—	PCI specifications recommend that a weak pull-up resistor (2–10 kΩ) be placed on the higher order pins to OV_{DD} when using 64-bit buffer mode (pins PCI_AD[63:32] and PCI1_C_$\overline{\text{BE}}$[7:4]).
PCI1_AD[63:32] / PCI2_AD[31:0]	—	
PCI1_C_$\overline{\text{BE}}$[3:0]	—	
PCI1_C_$\overline{\text{BE}}$[7:4] / PCI2_C_$\overline{\text{BE}}$[3:0]	—	
PCI1_CLK	If PCI1 is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI1_CLK, otherwise the processor will not boot up.	Tie high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively,
PCI1_DEVSEL	A weak pull-up resistor (2–10 kΩ) be placed on this pin to OV_{DD}.	
PCI1_FRAME		
PCI1_GNT0	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.
$\overline{\text{PCI1\_GNT}}$[4:1]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI*n*_AD pins as “No Connect” or terminated through 2–10 kΩ pull-up resistors with the default of internal arbiter if the PCIn_AD pins are not connected to any other PCI device. The PCI block drives the PCIn_AD pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.	If the POR defaults are acceptable, these output pins may be left floating.

Table 19. PCI Pin Recommendations (continued)

Pin	Pin Used	Pin Not Used
PCI1_IDSEL	—	Tie low through a 2–10 kΩ resistor to GND.
PCI1_IRDY	A weak pull-up resistor (2–10 kΩ) need be placed on this pin to OV_{DD}.	
PCI1_PAR	—	Tie low through a 2–10 kΩ resistor to GND.
PCI1_PAR64 / PCI2_PAR	—	
PCI1_PERR	A weak pull-up resistor (2–10 kΩ) need be placed on this pin to OV_{DD}.	
PCI1_REQ0	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.
PCI1_REQ[4:1]	—	
PCI1_REQ64 / PCI2_FRAME	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. A weak pull-up resistor (2–10 kΩ) need be placed on this pin to OV_{DD}. In the event that this POR pin need be pulled low at reset, extra logic needs to be added to do just that, as in normal operation this pin needs to be pulled-up.	
PCI1_SERR	A weak pull-up resistor (2–10 kΩ) need be placed on this pin to OV_{DD}.	
PCI1_STOP		
PCI1_TRDY		
PCI2_CLK	If PCI2 is configured as PCI asynchronous mode, a valid clock must be provided on pin PCI2_CLK, otherwise the processor will not boot up.	Tie high or low through a 2–10 kΩ resistor to OV_{DD} or GND, respectively,
PCI2_GNT0	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.
PCI2_GNT[4:1]	This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. When a PCI block is disabled, either the POR config pin that selects between internal and external arbiter must be pulled down to select external arbiter if there is any other PCI device connected on the PCI bus, or leave the PCI*n*_AD pins as “No Connect” or terminated through 2–10 kΩ pull-up resistors with the default of internal arbiter if the PCIn_AD pins are not connected to any other PCI device. The PCI block drives the PCIn_AD pins if it is configured to be the PCI arbiter—through POR config pins—irrespective of whether it is disabled via the DEVDISR register or not. It may cause contention if there is any other PCI device connected on the bus.	If the POR defaults are acceptable, these output pins may be left floating.
PCI2_IRDY	A weak pull-up resistor (2–10 kΩ) need be placed on this pin to OV_{DD}.	
PCI2_PERR		

Table 19. PCI Pin Recommendations (continued)

Pin	Pin Used	Pin Not Used
PCI2_REQ0	—	Tie high through a 2–10 kΩ resistor to OV_{DD}.
PCI2_REQ[4:1]	—	
PCI2_SERR	A weak pull-up resistor (2–10 kΩ) need be placed on this pin to OV_{DD}.	
PCI2_STOP		
PCI2_TRDY		

16 PIC Interface

This section discusses the termination of PIC pins on the device. Table 20 shows how the PIC pins should be connected.

Table 20. PIC Pin Recommendations

Pin	Pin Used	Pin Not Used
IRQ[0:8]	A weak pull-up or pull-down may be needed to the inactive state.	Tie high or low to the inactive state through a 2–10 kΩ resistor to OV_{DD} or GND, respectively,
IRQ9 / $\overline{\text{DMA\_DREQ3}}$		
IRQ10 / $\overline{\text{DMA\_DACK3}}$		
IRQ11 / $\overline{\text{DMA\_DDONE3}}$		
IRQ_OUT	Pull high through a 2–10 kΩ resistor to OV_{DD}.	
MCP		
UDE		

17 SerDes Interface

This section discusses the termination of SerDes pins on the device. Table 21 shows how the SerDes pins should be connected.

Table 21. SerDes Pin Recommendations

Pin	Pin Used	Pin Not Used
SD_PLL_TPD	Do not connect.	
SD_RX[0:7]	—	These pins must be connected to GND.
$\overline{\text{SD\_RX}}$[0:7]	—	
SD_TX[0:7]	If these pins are used for PCI Express, AC coupling capacitors need to be placed at the outputs.	These pins must be left unconnected.
$\overline{\text{SD\_TX}}$[0:7]		

18 System Control

This section discusses the termination of System Control pins on the device. Table 22 shows how the System Control pins should be connected.

Table 22. System Control Pin Recommendations

Pin	Pin Used	Pin Not Used
CKSTP_IN	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin7 of the COP connector (refer to Figure 7).	Pull high through a 2–10 kΩ resistor to OV_{DD}.
CKSTP_OUT	Pull this open-drain signal high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin15 of the COP connector (refer to Figure 7).	This pin may be left unconnected.
HRESET	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin13 of the COP connector (refer to Figure 7).	
HRESET_REQ	Pull high through a 2–10 kΩ resistor to OV_{DD}. This pin must NOT be pulled down during power-on reset.	This pin must NOT be pulled down during power-on reset.
SRESET	Pull high through a 2–10 kΩ resistor to OV_{DD}. Connect to Pin11 of the COP connector (refer to Figure 7).	Pull high through a 2–10 kΩ resistor to OV_{DD}.

19 Reserved Pins

Several pins on the MPC8548E are marked RESERVED. Table 23 shows how the SerDes pins should be connected.

Table 23. RESERVED Pin Recommendations

Pin Number	Comment
AC1	Pull high through a 2–10 kΩ resistor to OV_{DD}.
AC3	
M20	These pins must be left unconnected.
M21	
M25	This pin should be pulled to ground through a 300-Ω (±10%) resistor.
M26	This pin should be connected to XV_{DD}.
T22	These pins must be left unconnected.
T23	
V27	This pin should be pulled to ground through a 300-Ω (±10%) resistor.
V28	This pin should be connected to XV_{DD}.

20 Power and Ground Signals

The MPC8548E has several power supplies. Table 24 shows how the SerDes pins should be connected.

Table 24. Power and Ground Pin Recommendations

Pin	Comment
AV_{DD}_CORE	Power supply for e500 PLL (1.1 V through a filter).
AV_{DD}_LBIU	Power supply for Local Bus PLL (1.1 V through a filter).
AV_{DD}_PCI1	Power supply for PCI1 PLL (1.1 V through a filter).
AV_{DD}_PCI2	Power supply for PCI2 PLL (1.1 V through a filter).
AV_{DD}_PLAT	Power supply for core complex bus PLL. (1.1 V through a filter)
AV_{DD}_SRDS	Power supply for SerDes PLL (1.1 V through a filter).
BV_{DD}	Power supply for the Local Bus I/Os (2.5 V / 3.3 V).
GND	Power supply for the DDR I/Os (1.8 V / 2.5 V).
GV_{DD}	Power supply for the DDR I/Os (1.8 V / 2.5 V).
LV_{DD}	Power supply for the TSEC1 and TSEC2 I/Os (2.5 V / 3.3 V).
MVREF	DDR input reference voltage equal to approximately half of GV_{DD}
OV_{DD}	Power supply for PCI and other standards' I/Os (3.3 V).
SENSEVDD	This pin is connected to the V_{DD} plane internally and may be used by the core power supply to improve tracking and regulation.
SENSEVSS	This pin is connected to the GND plane internally and may be used by the core power supply to improve tracking and regulation.
SV_{DD}	Power supply for the SerDes transceivers (1.1 V).
TV_{DD}	Power supply for the TSEC3 and TSEC4 I/Os (2.5 V / 3.3 V).
XV_{DD}	Power supply for the SerDes I/Os (1.1 V).
V_{DD}	Power supply the core I/Os (1.1 V).

21 Revision History

Table 25 provides a revision history for this application note.

Table 25. Document Revision History

Revision	Date	Substantive Change(s)
3	07/2010	• In Section 2.1, "Power Supplies," for the list above the note, changed the second item from "2.5 V for RGMII, RTBI, or FIFO modes of operation" to "2.5 V for GMII, RGMII, RTBI, or FIFO modes of operation." • Added note in Section 6, "DDR Interface," to disable unused clocks.
2	07/2009	• Added IO power guideline on Section 2.3, "I/O Power Dissipation." • Removed ref to use 0.01uF or 0.1uF in Section 2.6, "Power Supply Decoupling."

Table 25. Document Revision History (continued)

Revision	Date	Substantive Change(s)
1	10/2008	• Updated Section 4.2, “Pin Map,” to change “top view of the pin map” to “bottom view of the pin map.” • In Section 16, “PIC Interface,” changed PCI to PIC in first sentence. • Updated part number column in Table 5, “MPC8548E Derivatives.”
0	06/2008	Initial release.

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