**Freescale Semiconductor**
Application Note

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# MPC8572E PowerQUICC™ III Bring-Up Guide

This document provides recommendations for new designs based on the MPC8572E PowerQUICC™ III family of integrated host communications processors (collectively referred to throughout this document as MPC8572E):

- MPC8572E
- MPC8572

This document may also be useful in debugging newly designed systems by highlighting those aspects of a design that merit special attention during initial system startup.

**Contents**





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# 1 Introduction

This section outlines recommendations to simplify the first phase of design. Before designing a system with an MPC8572E device, it is recommended that the designer be familiar with the available documentation, software, models, and tools.

## 1.1 MPC8572E Overview

This section provides a high-level overview of MPC8572E features. Figure 1 shows the major functional units within the device.

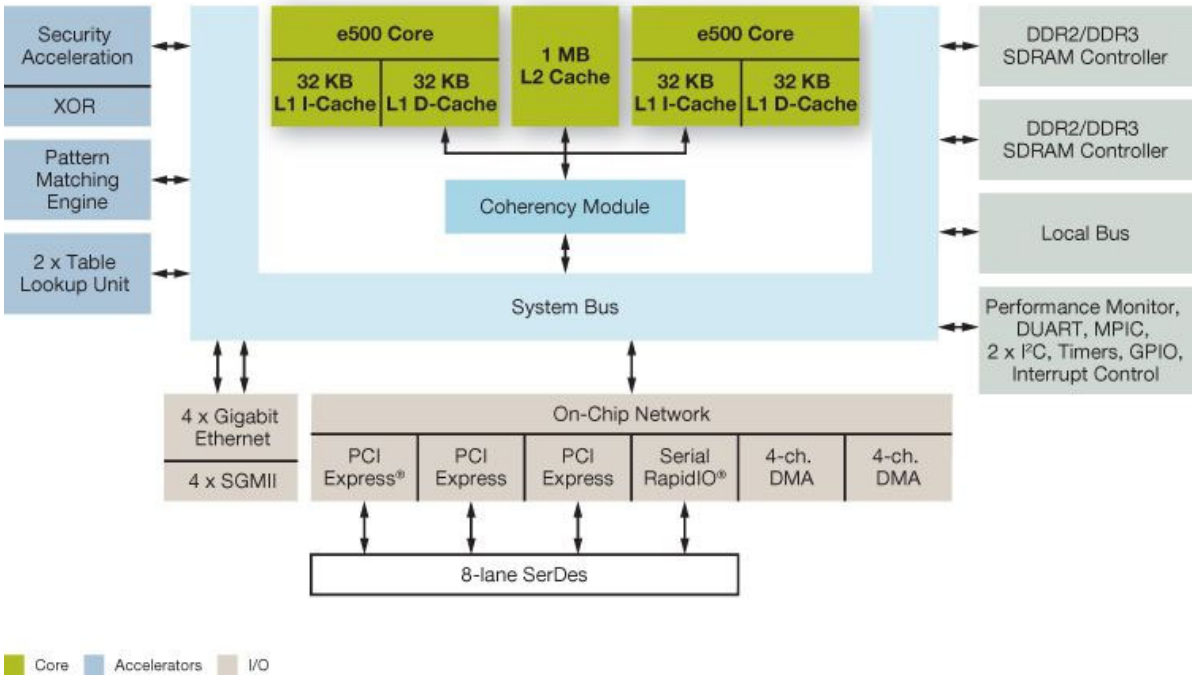



**Figure 1. MPC8572E Block Diagram**

## 1.2 References

Some references listed here may be available only under a non-disclosure agreement (NDA). Contact your local field applications engineer or sales representative to obtain a copy.

- Collateral
  - — *MPC8572 PowerQUICC™ III Fact Sheet* (MPC8572FS)
  - — *MPC8572E PowerQUICC III™ Integrated Host Processor Family Reference Manual* (MPC8572ERM)
  - — *Errata to MPC8572E PowerQUICC™ III Integrated Host Processor Family Reference Manual* (MPC8572ERMAD)

  - *Device Errata for the MPC8572E PowerQUICC™ III* (MPC8572ECE)
  - *MPC8572E PowerQUICC III™ Integrated Processor Hardware Specifications* (MPC8572EEC)
  - *PowerQUICC™ DDR2 SDRAM Controller Register Setting Considerations* (AN3369)
  - *Hardware and Layout Design Considerations for DDR2 SDRAM Memory Interfaces* (AN2910)
  - *MPC8572 Development System User's Guide* (MPC8572DSUG)
  - *MPC8572DS (Whitefin) Development System Errata* (MPC8572DSBE)
  - *MPC8572DS Development System Configuration Guide* (MPC8572ECFG)
- Tools
  - Software
    - Boot sequencer generator tool (I2CBOOTSEQ)
    - UPM Programming tool (LBCUPMIBCG)
  - Hardware
    - Development System (MPC8572DS) including schematics, bill of materials, board errata list, User's Guide, and configuration guide
- Models
  - IBIS
  - BSDL
  - Flowtherm

## 1.3 Device Errata

The MPC8572ECE document describes the device errata, fixes, and workarounds for the MPC8572E. This errata document should be researched thoroughly prior to starting a design with the MPC8572E device.

**NOTE**

This document is available under NDA. Contact your local Freescale office to obtain a copy.

## 1.4 Boot Sequencer Tool

The MPC8572E features the boot sequencer to allow configuration of any memory-mapped register before the completion of power-on reset (POR). The register data to be changed is stored in an $I^2C$ EEPROM. The MPC8572E requires a particular data format for register changes as outlined in the MPC8572ERM. The boot sequencer tool (I2CBOOTSEQ) is a C-code file. When compiled and given a sample data file, it will generate the appropriate raw data format as outlined in the MPC8572ERM. The file that is generated is an s-record file that can be used to program the EEPROM.

## 1.5 UPM Programming Tool

The UPM programming tool (LBCUPMIBCG) features a GUI for a user-friendly programming interface. It allows programming of all three of the MPC8572E's UPM machines. The GUI consists of a wave editor, a table editor, and a report generator. The user can edit the waveform directly or the RAM array directly. At the end of programming, the report generator prints out the UPM RAM array that can be used in a C-program.

## 1.6 Available Training

Our third-party partners are part of an extensive Design Alliance Program. The current training partners can be found on our website under Design Alliance Program at www.freescale.com/alliances.

Training material from past Smart Network Developer's Forums and Freescale Technology Forums are also available. These trainings modules are a valuable resource in understanding the *MPC8572E*. This material is also available at our website listed on the back cover of this document.

## 1.7 Product Revisions

Table 1 lists the processor version register (PVR) and system version register (SVR) values for the various MPC8572E derivatives of silicon.

**Table 1. Revision Level to Part Marking Cross-Reference**

| MPC8572E Revision | e500 V2 Core Revision | Processor Version Register | Device Marking | System Version Register |
|---|---|---|---|---|
| 1.0 | 3.0 | 0x8021_0030 | 00M44J | With Security Engine 0x80E8_0010 |
| | | | 60M44J | Without Security Engine 0x80E0_0010 |
| 1.1 | 3.0 | 0x8021_0030 | 01M44J | With Security Engine 0x80E8_0011 |
| | | | 61M44J | Without Security Engine 0x80E0_0011 |
| 1.1.1 | 3.0 | 0x8021_0030 | 02M44J | With Security Engine 0x80E8_0011 |
| | | | 62M44J | Without Security Engine 0x80E0_0011 |
| 2.0 [1] | 3.0 | 0x8021_0030 | 00M20X | With Security Engine 0x80E8_0020 |
| | | | 60M20X | Without Security Engine 0x80E0_0020 |
| 2.1 | 3.0 | 0x8021_0030 | 01M20X | With Security Engine 0x80E8_0021 |
| | | | 61M20X | Without Security Engine 0x80E0_0021 |

[1] Silicon version 2.0 is available for prototype purposes only. This version will not be available as a qualified device.

# 2 Power

This section provides design considerations for the MPC8572E power supplies and power sequencing. For information about AC and DC electrical specifications and thermal characteristics for the MPC8572E, refer to the MPC8572EEC Hardware Specifications document.

## 2.1 Power Supplies

The MPC8572E has a core voltage $V_{DD}$, PLL supply voltage $AV_{DD}$, and SerDes voltages $SV_{DD}$ and $XV_{DD}$ that operate at a lower voltage than the I/O voltages $BV_{DD}$, $GV_{DD}$, $LV_{DD}$, $OV_{DD}$, and $TV_{DD}$. The core voltage, 1.1 V (±5%), is supplied across $V_{DD}$ and GND.

The I/O blocks of the MPC8572E are supplied with the following:

- 1.8 V (±5%), 2.5 V (±5%), or 3.3 V (±5%) across $BV_{DD}$ and GND
- 1.5 V (±5%) or 1.8 V (±5%) across $GV_{DD}$ and GND
- 2.5 V (±5%) or 3.3 V (±5%) across $LV_{DD}$ and GND
- 3.3 V (±5%) across $OV_{DD}$ and GND
- 1.1 V (±5%) across $SV_{DD}$ and GND
- 2.5 V (±5%) or 3.3 V (±5%) across $TV_{DD}$ and GND
- 1.1 V (±5%) across $XV_{DD}$ and GND

Both $LV_{DD}$ and $TV_{DD}$ are used to supply the eTSEC interfaces on the device: $LV_{DD}$ powers eTSEC1 and eTSEC2, and $TV_{DD}$ powers eTSEC3, eTSEC4, and FEC. The supported voltage levels for $LV_{DD}/TV_{DD}$ are as follows:

- 3.3 V or 2.5 V for GMII, MII, RMII, and TBI modes of operation
- 2.5 V for RGMII, RTBI, and FIFO modes of operation.

**NOTE**

Each eTSEC port can be independently configured to operate in SGMII mode. Details are provided in the *MPC8572E PowerQUICC III™ Integrated Host Processor Family Reference Manual* (MPC8572ERM).

## 2.2 Power Consumption

Operating-mode power dissipation numbers (typical) are provided in the MPC8572E Hardware Specification (MPC8572EEC). Two typical numbers are provided, one at 65 °C and one at 105 °C, to assist in the thermal design for the device. If the targeted junction temperature ($T_J$) of the MPC8572E in the system is not one of these two temperatures, a linear extrapolation of these two typical dissipation values can be used to estimate the power dissipation at the targeted junction temperature.

The maximum, provided at 105 °C, is intended to assist in the power supply design selection.

Low-power mode estimates are provided in Table 2 for applications concerned about minimizing power consumption when the MPC8572 core is not active.

**Table 2. Power Dissipation Estimates for Low-Power Modes**

| Low Power Mode | Typical-70 [1] | Typical-110 [2] | Unit |
|---|---|---|---|
| SLEEP | 5.4 | 9.3 | W |
| NAP | 6.3 | 9.8 | W |
| DOZE | 6.7 | 11.1 | W |

**Notes:**

1. Typ-70 is based on $V_{DD}$ = 1.1 V and $T_j$ = 70 °C.
2. Typ-110 is based on $V_{DD}$ = 1.1 V and $T_j$ = 110 °C.

## 2.3 Power Sequencing

The device requires its power rails to be applied in a specific sequence in order to ensure proper device operation. These requirements, per the MPC8572EEC document, are as follows for power-up:

1. VDD, AVDD_*n*, BVDD, LVDD, OVDD, SVDD_SRDS1 and SVDD_SRDS2, TVDD, XVDD_SRDS1, and XVDD_SRDS2
2. $GV_{DD}$

All supplies must be at their stable values within 50 ms.

Items on the same line have no ordering requirement with respect to one another. Items on separate lines must be ordered sequentially such that voltage rails on a previous step must reach 90% of their value before the voltage rails on the current step reach 10% of theirs.

The purpose of the sequence is to guarantee the state of the DDR signals at reset. In order to guarantee MCKE low during power-up (as should be *attempted* per the JEDEC JESD79-2C specification), the above sequencing for $GV_{DD}$ is required. If there is no concern about any of the DDR signals being in an indeterminate state during power-up, then the sequencing of $GV_{DD}$ is not required.

From a system standpoint, if any of the I/O power supplies ramp prior to the $V_{DD}$ core supply, the I/Os associated with that I/O supply may drive a logic one or zero during power-up, and extra current may be drawn on the I/O power rails. This is due to the fact that there is no way for the logic to control the I/O buffers until the $V_{DD}$ core supply has been ramped. To avoid this additional current draw, the $V_{DD}$ core supply must be ramped prior to the I/O supplies.

## 2.4 PLL Power Supply Filtering

Each of the PLLs on the MPC8572EEC is provided with power through independent power supply pins (AVDD_PLAT, AVDD_CORE0, AVDD_CORE1, AVDD_DDR, AVDD_LBIU, AVDD_SRDS1, and AVDD_SRDS2). Preferably these voltages will be derived directly from $V_{DD}$ through a low frequency filter scheme.

While there are a number of ways to reliably provide power to the PLLs, the recommended solution is to provide independent filter circuits per the PLL power supply as illustrated in Figure 2, one to each of the $AV_{DD}$ pins. By providing independent filters to each PLL, the opportunity to cause noise injection from one PLL to the other is reduced. This circuit is intended to filter noise in the PLLs resonant frequency range from a 500-kHz to 10-MHz range.

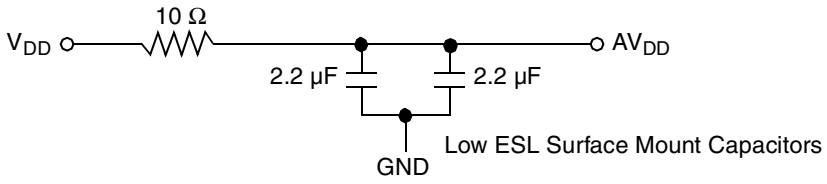
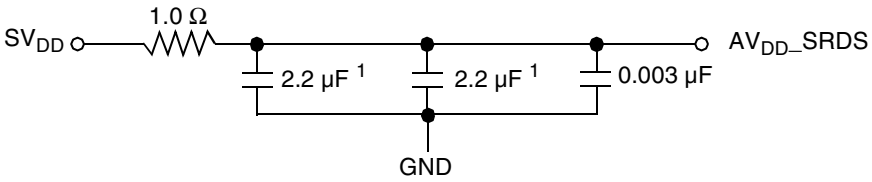



**Figure 2. PLL Power Supply Filter Circuit**

The $AV_{DD}$_SRDSn signals provide power for the analog portions of the SerDes PLL. To ensure stability of the internal clock, the power supplied to the PLL is filtered using a circuit similar to the one shown in Figure 3. For maximum effectiveness, the filter circuit is placed as closely as possible to the $AV_{DD}$_SRDSn balls to ensure it filters out as much noise as possible. The ground connection should be near the $AV_{DD}$_SRDSn balls. The 0.003-µF capacitor is closest to the balls, followed by the 1-µF capacitor, and finally the 1-Ω resistor to the board supply plane. The capacitors are connected from $AV_{DD}$_SRDSn to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. If the SerDes is not used, a filter for $AV_{DD}$_SRDS is not required.




1. An 0805 sized capacitor is recommended for system initial bring-up.
2. AVDD_SRDS should be a filtered version of SVDD.
3. Signals on the SerDes interface are fed from the XVDD power plane.

**Figure 3. SerDes PLL Power Supply Filter**

Each circuit should be placed as close as possible to the specific $AV_{DD}$ pin being supplied to minimize noise coupled from nearby circuits.

These filters are a necessary extension of the PLL circuitry and are compliant with the device specifications. Any deviation from the recommended filters is done at the customer's risk.

## 2.5 Power Supply Decoupling

The MPC8572E requires a clean, tightly regulated source of power. The system designer should place at least one decoupling capacitor at each $V_{DD}$ and B/G/L/O/$TV_{DD}$ pin of the device. These decoupling capacitors should have a value of 0.01 or 0.1 µF and receive their power from separate $V_{DD}$, B/G/L/O/$TV_{DD}$ and GND power planes in the PCB, utilizing short traces to minimize inductance.

In addition, several bulk storage capacitors should be distributed around the PCB to feed the $V_{DD}$ and B/G/L/O/$TV_{DD}$ planes, to enable quick recharging of the smaller chip capacitors.

The capacitors should be placed as close as possible to the MPC8572E processor. The capacitors need to be selected to work well with the power-supply so as to be able to handle the dynamic load requirements of the MPC8572E. For good, clean power supplied to the MPC8572E, the customer should work closely with their power-supply vendor to choose the correct value and type of capacitors.

If the SerDes is used, it requires a clean, tightly regulated source of power ($SV_{DD}$ and $XV_{DD}$) to ensure low jitter on transmit and reliable recovery of data in the receiver:

- The board should have at least 10 x 10-nF SMT ceramic chip capacitors as close as possible to the supply balls of the device.
- There should be a 1-µF ceramic chip capacitor from each SerDes supply ($SV_{DD}$ and $XV_{DD}$) to the board ground plane on each side of the device.
- Between the device and any SerDes voltage regulator there should be a 10-µF, low ESR SMT tantalum chip capacitor and a 100-µF, low ESR SMT tantalum chip capacitor. This should be done for all SerDes supplies.

## 2.6 Power Supplies Checklist

Table 3 provides a summary MPC8572E power supply checklist for the designer.

**Table 3. Power Supplies Checklist**

| Item | Description | Completed |
|---|---|---|
| 1 | All power supplies have a voltage tolerance no greater than 5% from the nominal value. | |
| 2 | eTSEC supplies are chosen according to the mode of operation used. | |
| 3 | Power supply selected is based on MAXIMUM power dissipation. | |
| 4 | Thermal design is based on TYPICAL power dissipation. | |
| 5 | Power-up sequence is less than 50 ms. | |
| 6 | Power sequencing is understood and based on whether or not latch-up or garbage data written to DDR is a concern. | |
| 7 | Recommended PLL filter circuit is applied to $AV_{DD}$_PLAT, $AV_{DD}$_CORE0, $AV_{DD}$_CORE1, $AV_{DD}$_DDR and $AV_{DD}$_LBIU. | |
| 8 | If SerDes1 or SerDes2 is enabled, then the recommended PLL filter circuit is applied to $AV_{DD}$_SRDS1 or $AV_{DD}$_SRDS1, respectively. Otherwise, a filter is not required. | |
| 9 | PLL filter circuits are placed as close to the respective $AV_{DD}$ pin as possible. | |
| 10 | Decoupling capacitors of 0.01 or 0.1 µF are placed at each $V_{DD}$, B/G/L/O/$TV_{DD}$ pin. | |
| 11 | Bulk capacitors are placed on each $V_{DD}$, B/G/L/O/$TV_{DD}$ plane. | |
| 12 | If SerDes is enabled, the recommended decoupling for S/$XV_{DD}$ is used. | |

# 3 Power-On Reset and Reset Configurations

This section discusses power-on reset and reset configurations. A summary MPC8572E POR and reset checklist is provided for the designer at the end of the section.

## 3.1 Configuration and Timing

Various device functions are initialized by sampling certain signals during the assertion of HRESET. These power-on reset (POR) inputs are either pulled high or low during this period. While these pins may be output pins during normal operation, they are treated as inputs while HRESET is asserted. HRESET must be asserted for a minimum on 100 µs. When HRESET de-asserts, the configuration pins are sampled and latched into registers and the pins then take on their normal input/output circuit characteristics.

All of the configuration pins have an internally gated 20 kΩ pull-up resistor, enabled only during HRESET. For those configurations in which the default state is desired, no external pull-up is required. Otherwise, a 4.7 kΩ pull-down resistor is recommended to pull the configuration pin to a valid logic low level. If the default setting is not a valid setting, 4.7 kΩ pull-up or pull-down resistors are required for proper configuration.

An alternative to using pull-up and pull-down resistors to configure the POR pins is to use a PLD or similar device which drives the configuration signals to the MPC8572E when HRESET is asserted. The PLD must begin to drive these signals at least four SYSCLK cycles prior to the de-assertion of HRESET (PLL configuration inputs must meet a 100 µs set-up time to HRESET), hold their values for at least 2 SYSCLK cycles after the de-assertion of HRESET, and then release the pins to high impedance afterward for normal device operation.

## 3.2 Configuration Settings

The following table summarizes the customer configurable device settings for the MPC8572E. Refer to the MPC8572ERM for a more detailed description of each configuration option.

**Table 4. User Configuration Options**

| Configuration Type | Functional Pins | Comments |
|---|---|---|
| System PLL Ratio | LA[29:31] | There is no default value for this PLL ratio; these signals must be pulled to the desired value. See Section 6, “DDR Interface.” |
| DDR PLL Ratio | TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2 | Default: Synchronous mode |
| e500 Core 0 PLL Ratio | LBCTL, LALE, LGPL2/LOE/LFRE | Default: Core0:CCB Clock Ratio = 3.5:1. |
| e500 Core 1 PLL Ratio | LWE[0]/LBS[0]/LFWE, UART_SOUT[1], READY_P1 | Default: Core1:CCB Clock Ratio = 3.5:1. |
| Boot ROM Location | TSEC1_TXD[6:4], TSEC1_TX_ER | Default: Local Bus GPCM (32-bit ROM) |
| Host/Agent | LWE[1:3]/LBS[1:3] | Default: MPC8572E acts as the host processor/root complex on all interfaces |

**Table 4. User Configuration Options (continued)**

| Configuration Type | Functional Pins | Comments |
|---|---|---|
| I/O Port Selection | TSEC1_TXD[3:1], TSEC2_TX_ER | Default: PCI Express® 1 port active (x8) (2.5 Gbps) |
| CPU Boot | LA[27], EC3_MDC | Default: Both e500 cores are allowed to boot without waiting for configuration by an external master |
| Boot Sequencer | LGPL3/$\overline{\text{LFWP}}$, LGPL5 | Default: Boot sequencer is disabled. No $I^2C$ ROM is accessed |
| DDR SDRAM Type | TSEC2_TXD[1] | Default: DDR controller is configured for DDR3 |
| FEC Configuration | $\overline{\text{DMA1\_DDONE[1]}}$ | Default: FEC is disabled and eTSEC3 and eTSEC4 are able to use their respective parallel interface pins |
| eTSEC1 SGMII | LA[28] | Default: eTSEC1 Ethernet interface operates in standard parallel interface mode according to POR config inputs of eTSEC1 width and eTSEC1 protocol. |
| eTSEC2 SGMII | LGPL1/LFALE | Default: eTSEC2 Ethernet interface operates in standard parallel interface mode according to POR config inputs of eTSEC2 width and eTSEC2 protocol. |
| eTSEC3 SGMII | TSEC3_TXD[3] | Default: eTSEC3 Ethernet interface operates in standard parallel interface mode according to POR config inputs of eTSEC3 width and eTSEC3 protocol, provided the FEC is not enabled. If the FEC is enabled, eTSEC3 is powered down. |
| eTSEC4 SGMII | UART_SOUT[0] | Default: eTSEC4 Ethernet interface operates in standard parallel interface mode according to POR config inputs of eTSEC4 width and eTSEC4 protocol, provided the FEC is not enabled. If the FEC is enabled, eTSEC4 is powered down. |
| eTSEC1 and eTSEC2 Width | EC1_MDC | Default: eTSEC1 and eTSEC2 Ethernet interfaces operate in their standard width TBI, GMII, MII mode if not configured to operate in SGMII mode. Or if eTSEC1 is in FIFO mode and not SGMII mode, it operates as a 16-bit FIFO. eTSEC2 FIFO width is 8 bits, if available (eTSEC1 must not be configured as a 16-bit FIFO), regardless of this configuration setting. |
| eTSEC3 and eTSEC4 Width | TSEC3_TXD[2] | Default: eTSEC3 Ethernet interface operates in standard width TBI, GMII, MII, or 8-bit FIFO mode if not configured to operate in SGMII mode and the FEC is disabled. eTSEC 4 is unavailable unless configured to operate in SGMII mode. |
| eTSEC1 Protocol | TSEC1_TXD[0], TSEC1_TXD[7] | Default: The eTSEC1 controller operates using the TBI protocol if not configured to operate in SGMII mode (or RTBI if configured in reduced mode). |
| eTSEC2 Protocol | TSEC2_TXD[0], TSEC2_TXD[7] | Default: The eTSEC2 controller operates using the TBI protocol if not configured to operate in SGMII mode (or RTBI if configured in reduced mode). |
| eTSEC3 Protocol | TSEC3_TXD[0], TSEC3_TXD[1] | Default: The eTSEC3 controller operates using the TBI protocol if not configured to operate in SGMII mode and FEC is disabled (or RTBI if configured in reduced mode). |
| eTSEC4 Protocol | TSEC4_TXD[0], TSEC4_TXD[1] | Default: The eTSEC4 controller operates using the RTBI protocol if not configured to operate in SGMII mode and FEC is disabled. |

**Table 4. User Configuration Options (continued)**

| Configuration Type | Functional Pins | Comments |
|---|---|---|
| SGMII SerDes Reference Clock Configuration | TSEC_1588_TRIG_OUT | Default: SGMII SerDes expects a 100 MHz reference clock frequency |
| RapidIO™ Device ID | TSEC2_TXD[2:4] | Default: The three lower-order bits of the RapidIO device ID are set to all 1s. |
| RapidIO System Size | LGPL0 | Default: Small system size (up to 256 devices). |
| Memory Debug | $\overline{\text{DMA2\_DACK}}$[0], $\overline{\text{DMA1\_DDONE}}$[0] | Default: Debug information from the DDR SDRAM controller 2 is driven on the MSRCID and MDVAL signals |
| DDR Debug | $\overline{\text{DMA2\_DDONE}}$[0] | Default: Debug information is not driven on ECC pins. ECC pins function in their normal mode. |
| General Purpose POR | LAD[0:31] | There is no default value for this general purpose POR. |
| eLBC FCM ECC Configuration | MSRCID[0] | Default: BRn[DECC] = 01. Data error checking is enabled, but ECC generation is disabled for FCM on full-page transfers. |
| SerDes1 Enable | TSEC2_TXD[5] | Default: SerDes1 interface is enabled. |
| SGMII SerDes Enable | $\overline{\text{UART\_RTS}}$[1] | Default: SGMII SerDes interface is enabled. |

## 3.3 Internal Test Modes

Several pins double as test mode enables. These test modes are for internal use only; if enabled during reset, they may result in the MPC8572E not coming out of reset. Table 5 lists these pins and how they should be addressed during the reset sequence.

**Table 5. Internal Test Mode Pins**

| Pin Group | Pins | Guideline for Reset |
|---|---|---|
| Debug | TRIG_OUT/READY_P0/$\overline{\text{QUIESCE}}$ | Because these pins have an internal pull-up enabled only at reset, they may be left floating if unconnected. Otherwise, they may need to be driven high (that is, by a PLD) if the device to which they are connected does not release these pins to high impedance during reset. |
| | MDVAL | |
| | MSRCID[0] | |
| | MSRCID[1] | |
| | MSRCID[2] | |
| | MSRCID[3] | |
| | MSRCID[4 | |
| Design For Test | $\overline{\text{LSSD\_MODE}}$ | These pins must be pulled to $OV_{DD}$ via a 100 Ω–1 kΩ resistor. |
| | L1_TSTCLK | |
| | L2_TSTCLK | |
| | $\overline{\text{TEST\_SEL}}$ | |

**Table 5. Internal Test Mode Pins (continued)**

| Pin Group | Pins | Guideline for Reset |
|---|---|---|
| Power Management | ASLEEP | Since these pins have an internal pull-up enabled only at reset, they may be left floating if unconnected. Otherwise, they may need to be driven high (that is, by a PLD) if the device to which they are connected does not release these pins to high impedance during reset. |
| System Control | HRESET_REQ | |

## 3.4 Reset Checklist

Table 6 provides a summary MPC8572E POR and reset checklist for the designer.

**Table 6. Checklist for POR and Reset Configurations**

| Item | Description | Completed |
|---|---|---|
| 1 | HRESET is asserted for a minimum of 100 µs. | |
| 2 | The following signals must NOT be pulled low during POR sequence: EC5_MDC, HRESET_REQ, TRIG_OUT/READY_P0/QUIESCE, MSRCID[1:4], MDVAL, ASLEEP, DMA_DACK[0:1]. | |
| 3 | Configuration pins are either appropriately tied-off with a 4.7 kΩ resistor, or driven by an external device (meeting their required setup and hold times). Otherwise, default configurations will be used. | |
| 4 | PLL configurations are defined and meet the required set-up and hold times. | |
| 5 | SD1_REF_CLK is present if SerDes1 enabled. SD2_REF_CLK is present if SerDes2 enabled. | |
| 6 | Internal test mode pins are guaranteed not to be low during reset. | |
| 7 | Valid SD1_REF_CLK provided if SerDes1 is enabled. Valid SD2_REF_CLK provided if SerDes2 is enabled. | |

# 4 Device Pins

This section discusses recommended test points and provides various views of the device pin map.

## 4.1 Recommended Test Points

For easier debug, it is recommended that the test points on the board include the following pins:

- CLK_OUT (This helps to verify the CCB clock.)
- TRIG_OUT (This helps to verify the end of the reset sequence.)
- ASLEEP (This helps to verify the end of the reset sequence.)
- SENSEVDD (This helps to verify power plane VDD.)
- SENSEVSS (This helps to verify ground plane VSS.)
- HRESET_REQ (This helps to verify proper boot sequencer functions and reset requests.)

## 4.2 Pin Map

Figure 4 provides a bottom view of the pin map of the device. Figure 5 through Figure 8 provide detailed views.

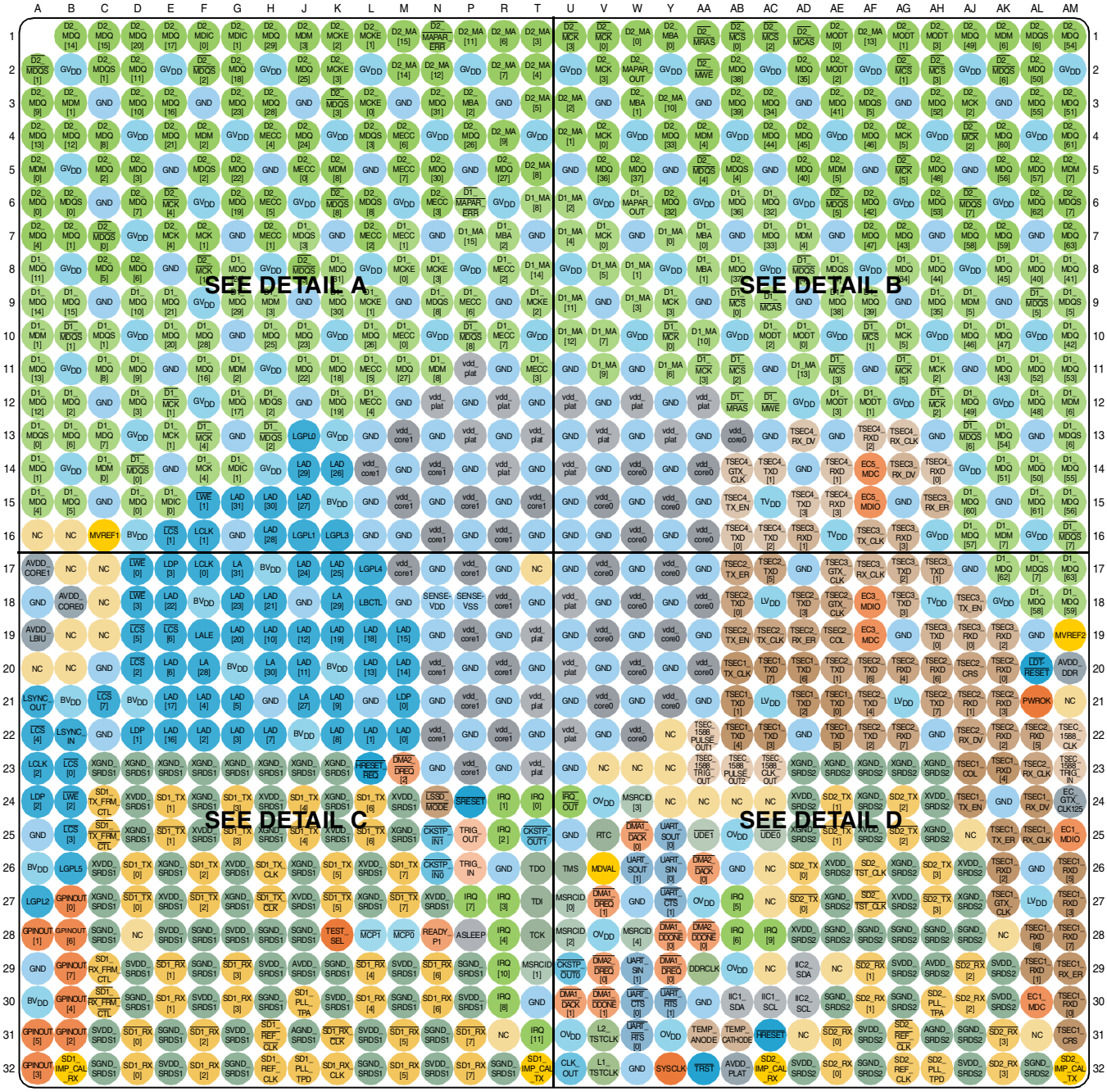
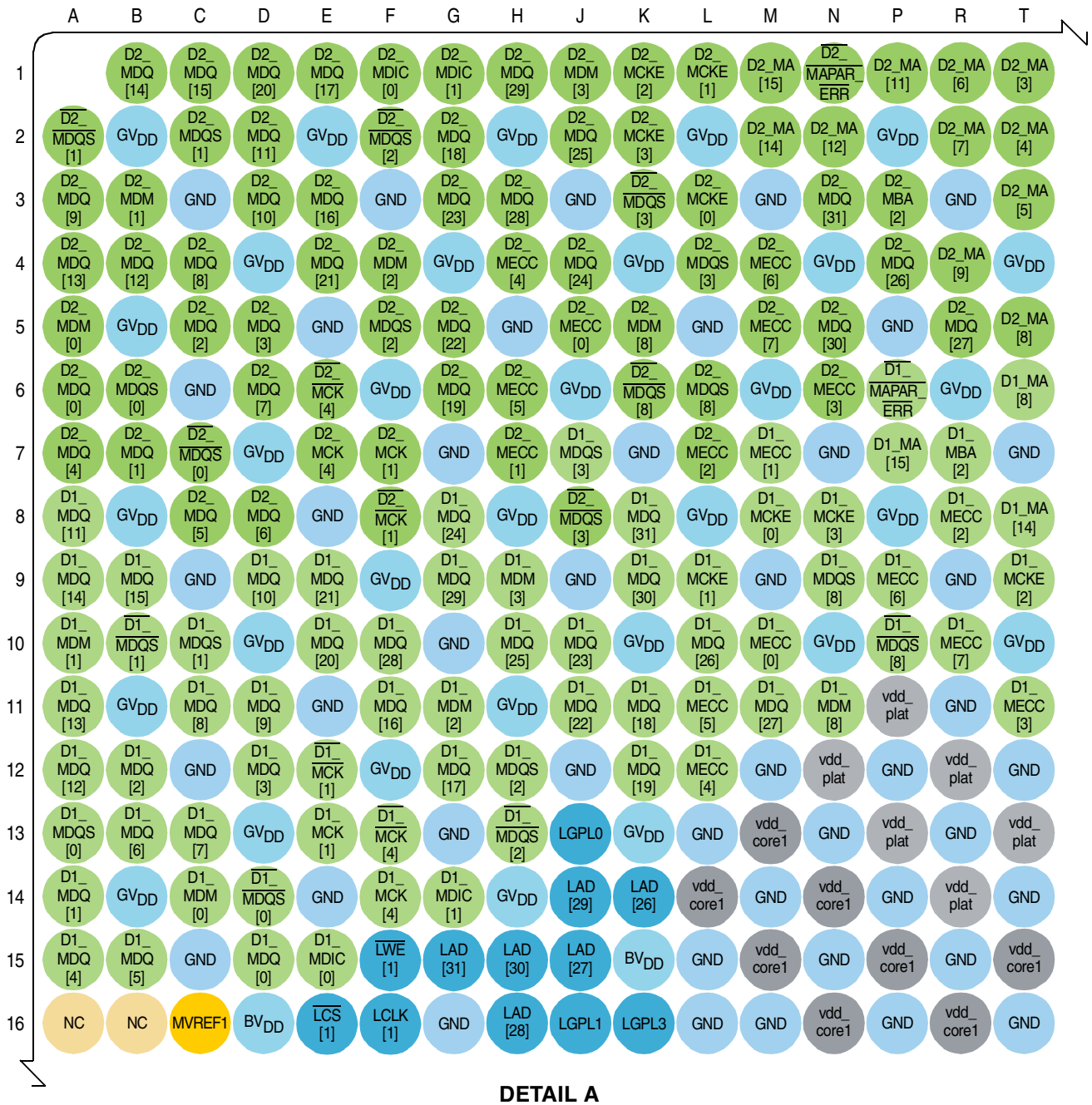
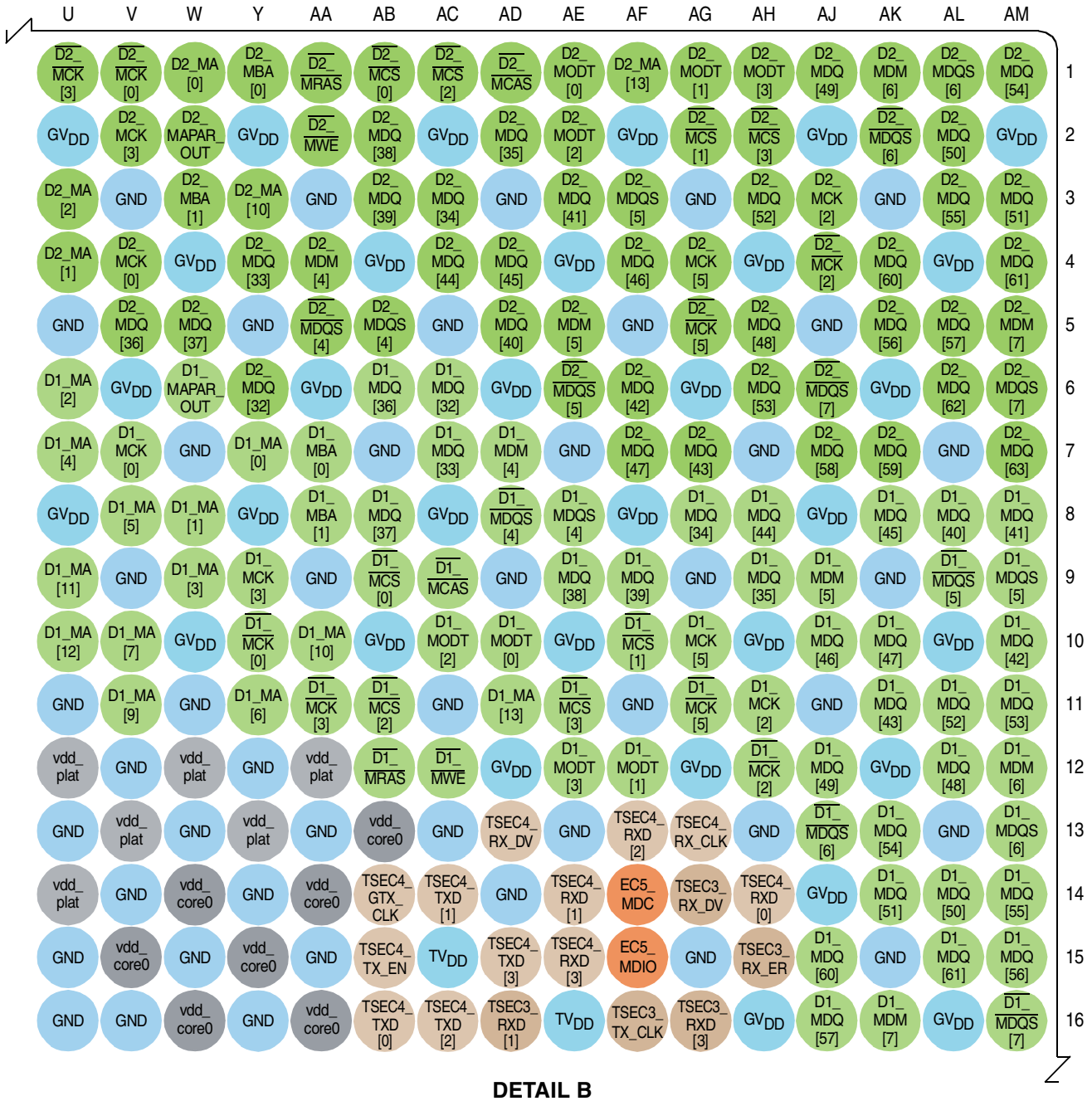



**Figure 4. MPC8572E Pin Map Bottom View**




**DETAIL A**

**Figure 5. MPC8572E Pin Map Detail A**




**DETAIL B**

**Figure 6. MPC8572E Pin Map Detail B**

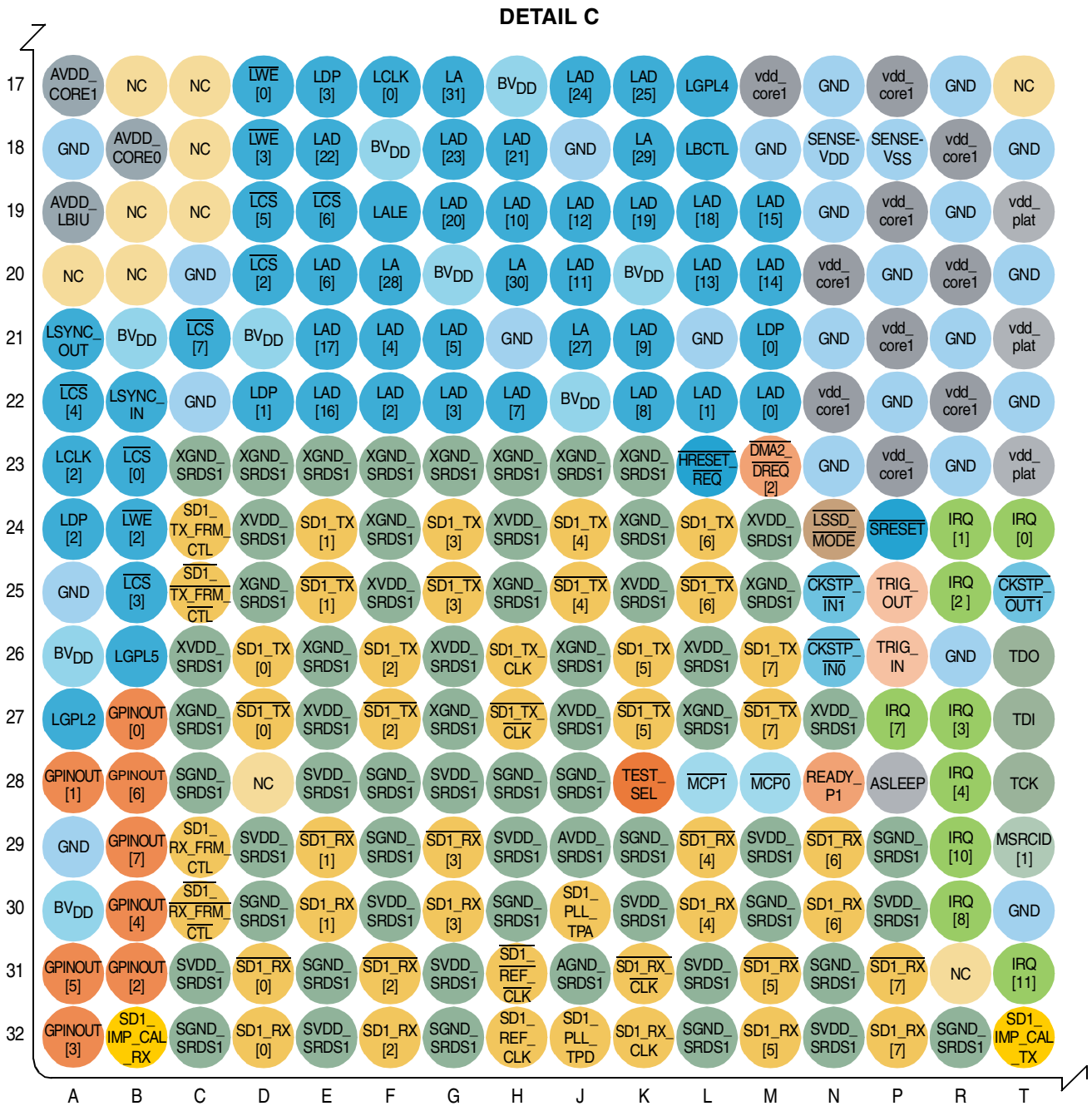



**Figure 7. MPC8572E Pin Map Detail C**

**DETAIL D**

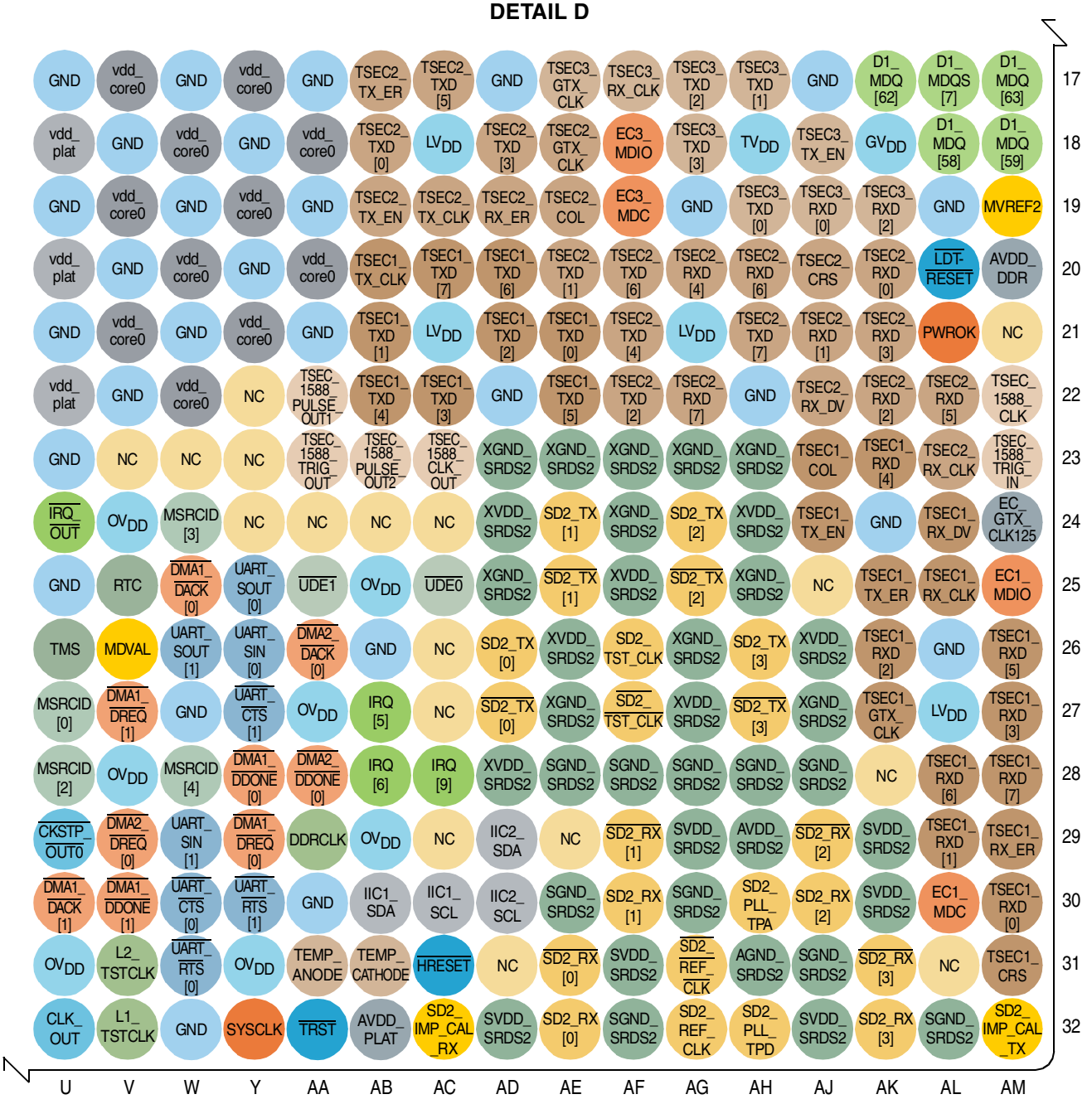



**Figure 8. MPC8572E Pin Map Detail D**

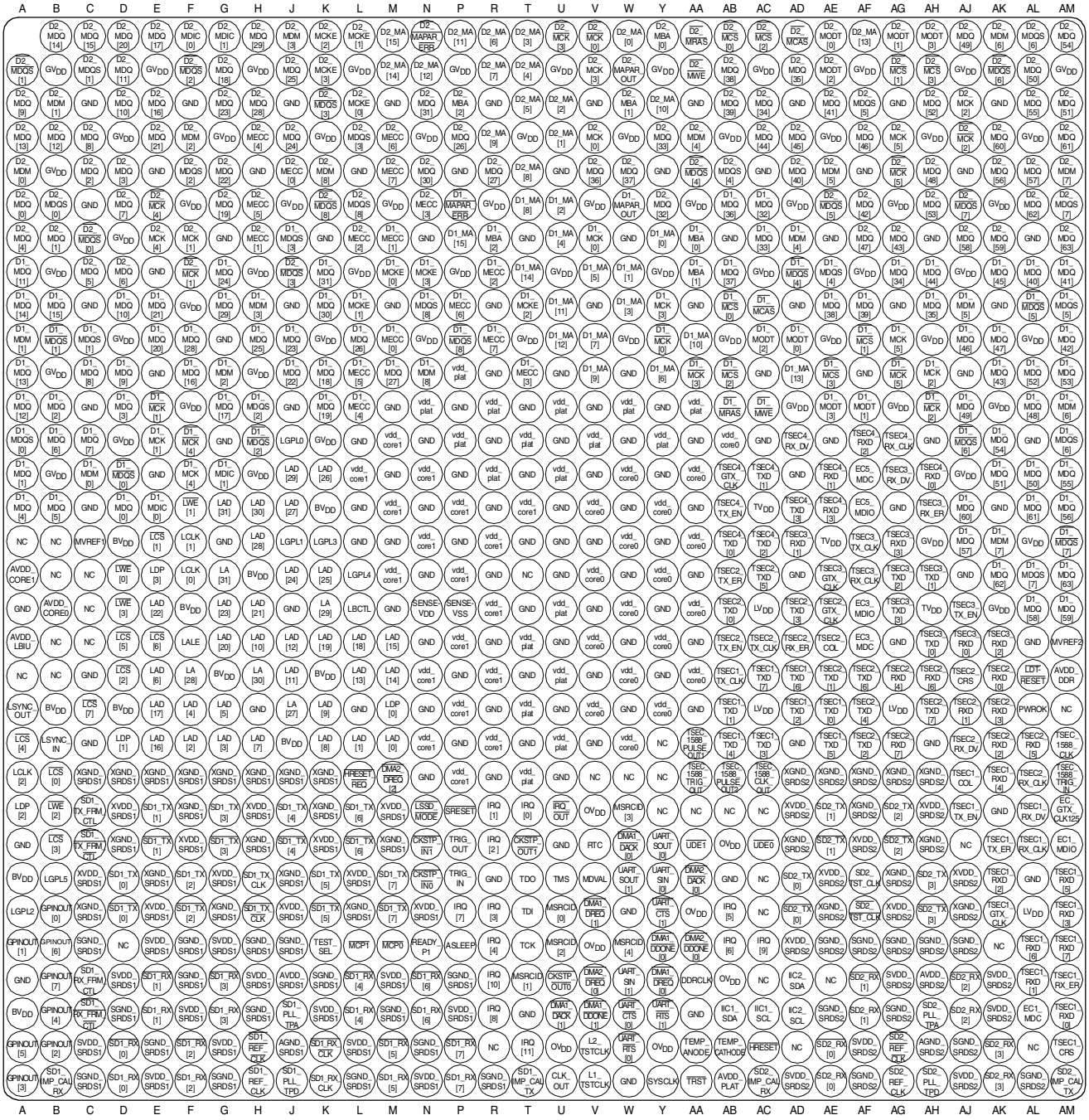


**Figure 9. MPC8572E Ball Map**

# 5 Clocks

Figure 10 shows the internal distribution of clocks within the MPC8572E.

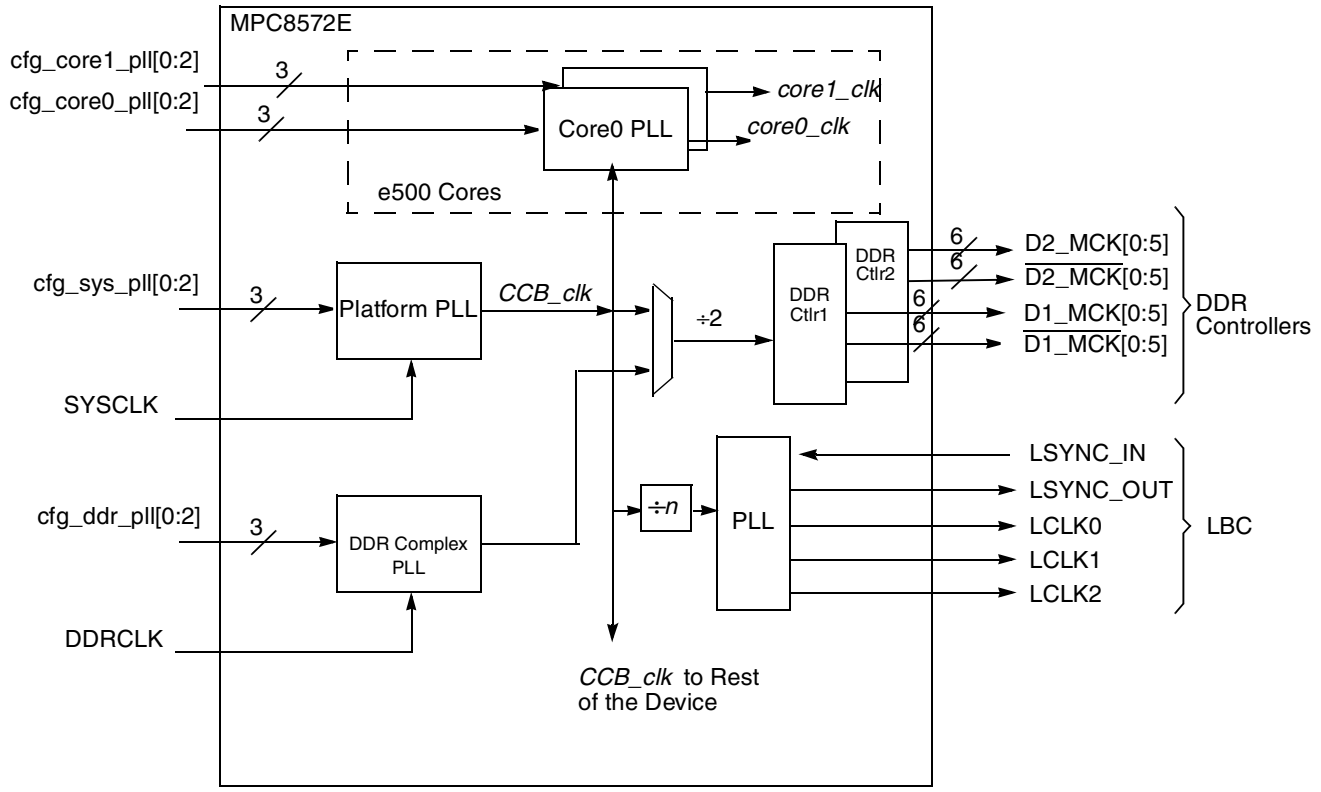



**Figure 10. Clock Subsystem Block Diagram**

The clock inputs for the MPC8572E are the SYSCLK, DDRCLK, EC_GTX_CLK125, RTC, SD1_REF_CLK/SD1_REF_CLK, and SD2_REF_CLK/SD2_REF_CLK. SYSCLK is the primary clock input to the device. DDRCLK is the reference clock used for the DDR interface when it is configured in asynchronous mode. The EC_GTX_CLK125 input is used by the eTSEC controller as a reference clock for gigabit Ethernet modes. SD1_REF_CLK/SD1_REF_CLK is the reference clock for the PCI Express® and RapidIO interfaces, and SD2_REF_CLK/SD2_REF_CLK is the reference clock for the SGMII interfaces. Table 10 shows how the clock pins should be connected.

**Table 10. Clock Pin Recommendations**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| DDRCLK | If DDR is configured in asynchronous mode, connect to an input clock as described in the MPC8572EEC Hardware Specifications document. | Connect to GND through a 2–10 kΩ resistor. |
| TSEC_1588_CLK | Connect to an input clock as described in the MPC8572EEC Hardware Specifications document. | Connect to GND through a 2–10 kΩ resistor. |

**Table 10. Clock Pin Recommendations (continued)**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| TSECn_RX_CLK | — | Tie high or low through a 2–10 kΩ resistor to $L/TV_{DD}$ or GND, respectively. |
| FEC_RX_CLK | — | Tie high or low through a 2–10 kΩ resistor to $L/TV_{DD}$ or GND, respectively. |
| EC_GTX_CLK125 | If any of the eTSECs are used in gigabit mode, connect to a 125 MHz clock. | Connect to GND through a 2–10 kΩ resistor. |
| RTC | If used, connect to a clock that runs no greater than 1/4 the platform CCB_clk. | Pull high or low through a 2–10 kΩ resistor to $OV_{DD}$ or GND, respectively. |
| SD1_REF_CLK/ $\overline{\text{SD1\_REF\_CLK}}$ | If SerDes1 is enabled via POR config pins, connect to a clock at the frequency specified per the POR I/O Port Selection. [1] | These pins must be connected to XGND_SRDS1. |
| SD2_REF_CLK/ $\overline{\text{SD2\_REF\_CLK}}$ | If SGMII SerDes is enabled via POR config pins, connect to a clock at the frequency specified per the POR I/O Port Selection.[1] | These pins must be connected to XGND_SRDS2. |
| SYSCLK | This must always be connected to an input clock of 33–133 MHz. | |

**Note:**

1 If SerDes is enabled, corresponding SerDes Reference Clock must be provided to successfully complete POR.

## 5.1 System PLL Ratio

The system PLL inputs, shown in Table 11 establish the clock ratio between the SYSCLK input and the platform clock used by the MPC8572E.

**Table 11. CCB Clock PLL Ratio**

| Functional Signals | Reset Configuration Name | Value (Binary) | CCB Clock : SYSCLK Ratio |
|---|---|---|---|
| LA[29:31] | cfg_sys_pll[0:2] | 000 | 4 : 1 |
| | | 001 | 5 : 1 |
| No Default | | 010 | 6 : 1 |
| | | 011 | 8 : 1 |
| | | 100 | 10 : 1 |
| | | 101 | 12 : 1 |
| | | 110 | Reserved |
| | | 111 | Reserved |

## 5.2 e500 Core PLL Ratios

The Core0 and Core1 PLL Ratios, shown in Table 12 and Table 13 respectively, establish the ratio between the e500 core clocks and the e500 core complex bus (CCB) clock.

**Table 12. e500 Core0 Clock PLL Ratios**

| Functional Signals | Reset Configuration Name | Value (Binary) | e500 Core0: CCB ClockRatio |
|---|---|---|---|
| LBCTL, LALE, LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$ | cfg_core0_pll[0:2] | 000 | Reserved |
| | | 001 | Reserved |
| Default (111) | | 010 | Reserved |
| | | 011 | 3 : 2 (1.5 : 1) |
| | | 100 | 2 : 1 |
| | | 101 | 5 : 2 (2.5:1) |
| | | 110 | 3 : 1 |
| | | 111 | 7 : 2 (3.5 : 1) |

**Table 13. e500 Core1 Clock PLL Ratios**

| Functional Signals | Reset Configuration Name | Value (Binary) | e500 Core1 : CCB ClockRatio |
|---|---|---|---|
| $\overline{\text{LWE}}$[0]/$\overline{\text{LBS}}$[0]/$\overline{\text{LFWE}}$, UART_SOUT[1], READY_P1 | cfg_core1_pll[0:2] | 000 | Reserved |
| | | 001 | Reserved |
| Default (111) | | 010 | Reserved |
| | | 011 | 3 : 2 (1.5 : 1) |
| | | 100 | 2 : 1 |
| | | 101 | 5 : 2 (2.5:1) |
| | | 110 | 3 : 1 |
| | | 111 | 7 : 2 (3.5 : 1) |

## 5.3 DDR PLL Ratio

The DDR PLL Ratio, shown in Table 14, establishes the ratio between the DDRCLK input and the DDR Complex Clock. The DDR Complex Clock is divided by two before being provided to the DDR interface. Since DDR data is transferred on both the rising and falling edges, the DDR data rate (in MT/s) is equal to the DDR Complex Clock frequency (in MHz).

**Table 14. DDR Complex Clock PLL Ratio**

| Functional Signals | Reset Configuration Name | Value (Binary) | DDR Complex Clock:DDRCLK Ratio |
|---|---|---|---|
| TSEC_1588_CLK_OUT, TSEC_1588_PULSE_OUT1, TSEC_1588_PULSE_OUT2<br><br>Default (111) | cfg_ddr_pll[0:2] | 000 | 3 : 1 |
| | | 001 | 4 : 1 |
| | | 010 | 6 : 1 |
| | | 011 | 8 : 1 |
| | | 100 | 10 : 1 |
| | | 101 | 12 : 1 |
| | | 110 | 14 : 1 |
| | | 111 | Synchronous mode |

# 6 DDR Interface

This section discusses the termination of DDR pins on the device. Table 15 shows how the DDR pins should be connected.

**Table 15. DDR Pin Recommendations**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| MA[0:15] | Auto-precharge for DDR signaled on A10 when DDR_SDRAM_CFG[PCHB8] = 0. Auto-precharge for DDR signaled on A8 when DDR_SDRAM_CFG[PCHB8] = 1. | These pins may be left unconnected. |
| MBA[0:2] | — | |
| $\overline{\text{MCAS}}$ | — | |
| MCK/$\overline{\text{MCK}}$[0:5] | — | |
| MCKE[0:3] | These pins are actively driven instead of being tri-stated during reset. | |
| $\overline{\text{MCS}}$[0:3] | — | |
| MDIC[0:1] | When operating in DDR2 mode, connect Dn_MDIC[0] to ground through an 18.2-W (full-strength mode) or 36.4-W (half-strength mode) precision 1% resistor, and connect Dn_MDIC[1] to GVDD through an 18.2-W (full-strength mode) or 36.4-W (half-strength mode) precision 1% resistor. When operating in DDR3 mode, connect Dn_MDIC[0] to ground through an 20-W (full-strength mode) or 40-W (half-strength mode) precision 1% resistor, and connect Dn_MDIC[1] to GVDD through an 20-W (full-strength mode) or 40-W (half-strength mode) precision 1% resistor. These pins are used for automatic calibration of the DDR IOs. | |

**Table 15. DDR Pin Recommendations (continued)**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| $\overline{\text{MAPAR\_ERR}}$ | — | This pin should be connected to GVDD via a 2-10 kΩ resistor. |
| MAPAR_OUT | | These pins may be left unconnected. |
| MDM[0:8] | — | These pins may be left unconnected. |
| MDQ[0:63] | — | These pins should be pulled low via a 2-10 kΩ resistor. |
| MDQS[0:8] | — | These pins should be pulled low via a 2-10 kΩ resistor. |
| $\overline{\text{MDQS}}$[0:8] | — | These pins should be pulled to GVDD via a 2-10 kΩ resistor. |
| MECC[0:7] | — | These pins should be pulled low via a 2-10 kΩ resistor. |
| MODT[0:3] | — | These pins may be left unconnected. |
| $\overline{\text{MRAS}}$ | — | |
| $\overline{\text{MWE}}$ | — | |

# 7 Debug and Test Interface

This section discusses the termination of debug and test pins on the device. Table 16 shows how the debug and test pins should be connected.

**Table 16. Debug and Test Pin Recommendations**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| ASLEEP | This pin must NOT be pulled down during power-on reset. | This pin may be left unconnected. |
| CLK_OUT | NOTE: This output is actively driven during reset rather than being tri-stated during reset. | This pin may be left unconnected. |
| MDVAL | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | This pin may be left unconnected. |
| L1_TSTCLK | These signals must be pulled up via a 100–1000 Ω resistor to $OV_{DD}$ for normal machine operation. | |
| L2_TSTCLK | | |
| $\overline{\text{LSSD\_MODE}}$ | | |
| $\overline{\text{TEST\_SEL}}$ | | |
| MSRCID[0:1] | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | This pin may be left unconnected. |
| MSRCID[2:4] | This pin must NOT be pulled down during power-on reset. | This pin must be left unconnected. |
| SD1_IMP_CAL_RX | This pin must be pulled down through a 200 Ω (±1%) resistor. | |
| SD1_IMP_CAL_TX | This pin must be pulled down through a 100 Ω (±1%) resistor. | |

**Table 16. Debug and Test Pin Recommendations (continued)**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| SD1_PLL_TPA | Do not connect. | |
| SD2_IMP_CAL_RX | This pin must be pulled down through a 200 Ω (±1%) resistor. | |
| SD2_IMP_CAL_TX | This pin must be pulled down through a 100 Ω (±1%) resistor. | |
| SD2_PLL_TPA | Do not connect. | |
| $\overline{\text{TEST\_SEL}}$ | This signal must be pulled up via a 100-1000 Ω resistor to $OV_{DD}$ for normal machine operation. | |
| TEMP_ANODE, TEMP_CATHODE | TEMP_ANODE, TEMP_CATHODE are temperature diode pins on the microprocessor that can be used in conjunction with other system temperature monitoring devices (such as Analog Devices, ADT7461™ | These pins may be left unconnected. |
| TRIG_IN | — | Tie low through a 2–10 kΩ resistor to GND. |
| TRIG_OUT/READY_P0/ $\overline{\text{QUIESCE}}$ | This pin must NOT be pulled down during power-on reset. | This pin must be left unconnected. |

# 8 DMA Interface

This section discusses the termination of DMA pins on the device. Table 17 shows how the DMA pins should be connected.

**Table 17. DMA Pin Recommendations**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| $\overline{\text{DMA1\_DREQ}}$[0:1] | — | Pull high through a 2–10 kΩ resistor to $OV_{DD}$. |
| $\overline{\text{DMA1\_DACK}}$[0:1] | This pin must NOT be pulled down during power-on reset. | These output pins may be left floating. |
| $\overline{\text{DMA1\_DDONE}}$[0:1] | These pins are reset configuration pins and may require 4.7 kΩ pull-up or pull-down resistors. | |
| $\overline{\text{DMA2\_DREQ}}$[0] | — | Pull high through a 2–10 kΩ resistor to $OV_{DD}$. |
| $\overline{\text{LCS}}$[5]/$\overline{\text{DMA2\_DREQ}}$[1] | — | Pull high through a 2–10 kΩ resistor to $OV_{DD}$. |
| $\overline{\text{DMA2\_DREQ}}$[2] | — | Pull high through a 2–10 kΩ resistor to $OV_{DD}$. |
| $\overline{\text{DMA2\_DACK}}$[0] | This pin is a reset configuration pin and may require a 4.7 kΩ pull-up or pull-down resistor. | |
| $\overline{\text{LCS}}$[6]/$\overline{\text{DMA2\_DACK}}$[1] | — | If the Local Bus function of this pin is not used, this output pin may be left floating. |
| $\overline{\text{DMA2\_DDONE}}$[0] | This pin is a reset configuration pin and may require a 4.7 kΩ pull-up or pull-down resistor. | |
| $\overline{\text{LCS}}$[7]/$\overline{\text{DMA2\_DDONE}}$[1] | — | If the Local Bus function of this pin is not used, this output pin may be left floating. |

# 9 DUART Interface

This section discusses the termination of DUART pins on the device. Table 18 shows how the DUART pins should be connected.

**Table 18. DUART Pin Recommendations**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| $\overline{\text{UART\_CTS}}$[0:1] | — | Tie high through a 2–10 kΩ resistor to $OV_{DD}$. |
| $\overline{\text{UART\_RTS}}$[0] | — | This output pin may be left floating. |
| $\overline{\text{UART\_RTS}}$[1] | — | These pins are reset configuration pins and may require 4.7 kΩ pull-up or pull-down resistors. |
| UART_SIN[0:1] | — | Tie low through a 2–10 kΩ resistor to GND. |
| UART_SOUT[0:1] | These pins are reset configuration pins and may require 4.7 kΩ pull-up or pull-down resistors. | |

# 10 Ethernet Management Interface

This section discusses the termination of the Ethernet management pins on the device. Table 19 shows how the Ethernet management pins should be connected.

**Table 19. Ethernet Management Pin Recommendations**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| EC1_MDC | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | If the POR default is acceptable, this output pin may be left floating. |
| EC1_MDIO | — | Tie high or low through a 2–10 kΩ resistor to $OV_{DD}$ or GND, respectively. |
| EC3_MDC | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | If the POR default is acceptable, this output pin may be left floating. |
| EC3_MDIO | — | Tie high or low through a 2–10 kΩ resistor to $OV_{DD}$ or GND, respectively. |
| EC5_MDC | This pin must NOT be pulled down during power-on reset. | This output pin may be left floating. |
| EC5_MDIO | — | Tie high or low through a 2–10 kΩ resistor to $OV_{DD}$ or GND, respectively. |

# 11 eTSEC Interface

This section discusses the termination of the Ethernet pins on the device. Table 20 shows how the Ethernet pins should be connected.

**Table 20. Ethernet Pin Recommendations**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| TSEC_1588_CLK | — | Tie low through a 2–10 kΩ resistor to GND. |
| TSEC_1588_TRIG_IN | — | Tie low through a 2–10 kΩ resistor to GND. |
| TSEC_1588_TRIG_OUT | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | If the POR default is acceptable, this output pin may be left floating. |
| TSEC_1588_CLK_OUT | | |
| TSEC_1588_PULSE_OUT1 | | |
| TSEC_1588_PULSE_OUT2 | | |
| TSEC1_COL/FIFO1_TX_FC | — | Tie low through a 2–10 kΩ resistor to GND. |
| TSEC2_COL/FIFO2_TX_FC | — | Tie low through a 2–10 kΩ resistor to GND. |
| TSEC4_RX_CLK/TSEC3_COL/ FEC_COL/FIFO3_TX_FC | — | Tie high or low through a 2–10 kΩ resistor to $TV_{DD}$ or GND, respectively. |
| TSEC1_RXD[7:0]/FIFO1_RXD[7:0] | — | Tie high or low through a 2–10 kΩ resistor to $LV_{DD}$ or GND, respectively. |
| TSEC1_TXD[7]/FIFO1_TXD[7] | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | If the POR default is acceptable, this output pin may be left floating. |
| TSEC1_TXD[6:4]/FIFO1_TXD[6:4] | | |
| TSEC1_TXD[3:1]/FIFO1_TXD[3:1] | | |
| TSEC1_TXD[0]/FIFO1_TXD[0] | | |
| TSEC1_CRS/FIFO1_RX_FC | — | Tie low through a 2–10 kΩ resistor to GND. |
| TSEC1_GTX_CLK | — | These output pins may be left floating. |
| TSEC1_RX_CLK/FIFO1_RX_CLK | — | Tie high or low through a 2–10 kΩ resistor to $LV_{DD}$ or GND, respectively. |
| TSEC1_RX_DV/FIFO1_RX_DV/FIF O1_RXC[0] | — | Tie low through a 2–10 kΩ resistor to GND. |
| TSEC1_RX_ER/FIFO1_RX_ER/FIF O1_RXC[1] | — | |
| TSEC1_TX_CLK/FIFO1_TX_CLK | — | Tie high or low through a 2–10 kΩ resistor to $LV_{DD}$ or GND, respectively. |
| TSEC1_TX_EN/FIFO1_TX_EN/FIF O1_TXC[0] | These pins require an external 4.7 kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively (during reset). | These output pins may be left floating. |
| TSEC1_TX_ER/FIFO1_TX_ERR/FI FO1_TXC[1] | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | If the POR default is acceptable, this output pin may be left floating. |

**Table 20. Ethernet Pin Recommendations (continued)**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| TSEC2_RXD[7:0]/FIFO2_RXD[7:0]/ FIFO1_RXD[15:8] | — | Tie high or low through a 2–10 kΩ resistor to $LV_{DD}$ or GND, respectively. |
| TSEC2_TXD[7]/FIFO2_TXD[7]/FIF O1_TXD[15] | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | If the POR default is acceptable, this output pin may be left floating. |
| TSEC2_TXD[6]/FIFO2_TXD[6]/FIF O1_TXD[14] | | |
| TSEC2_TXD[5]/FIFO2_TXD[5]/FIF O1_TXD[13] | | |
| TSEC2_TXD[4:2]/FIFO2_TXD[4:2]/ FIFO1_TXD[12:10] | | |
| TSEC2_TXD[1]/FIFO2_TXD[1]/FIF O1_TXD[9] | | |
| TSEC2_TXD[0]/FIFO2_TXD[0]/FIF O1_TXD[8] | | |
| TSEC2_CRS/FIFO2_RX_FC | — | Tie low through a 2–10 kΩ resistor to GND. |
| TSEC2_GTX_CLK | — | These output pins may be left floating. |
| TSEC2_RX_CLK/FIFO2_RX_CLK | — | Tie high or low through a 2–10 kΩ resistor to $LV_{DD}$ or GND, respectively. |
| TSEC2_RX_DV/FIFO2_RX_DV/FIF O1_RXC[2] | — | Tie low through a 2–10 kΩ resistor to GND. |
| TSEC2_RX_ER/FIFO2_RX_ER | — | |
| TSEC2_TX_CLK/FIFO2_TX_CLK | — | Tie high or low through a 2–10 kΩ resistor to $LV_{DD}$ or GND, respectively. |
| TSEC2_TX_EN/FIFO2_TX_EN/FIF O1_TXC[2] | These pins require an external 4.7 kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively (during reset). | These output pins may be left floating. |
| TSEC2_TX_ER/FIFO2_TX_ERR | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | If the POR default is acceptable, this output pin may be left floating. |
| TSEC3_TXD[3]/FEC_TXD[3]/FIFO3 _TXD[3] | | |
| TSEC3_TXD[2]/FEC_TXD[2]/FIFO3 _TXD[2] | | |
| TSEC3_TXD[1:0]/FEC_TXD[1:0]/FI FO3_TXD[1:0] | | |
| TSEC3_RXD[3:0]/FEC_RXD[3:0]/FI FO3_RXD[3:0] | — | Tie high or low through a 2–10 kΩ resistor to $TV_{DD}$ or GND, respectively. |
| TSEC3_GTX_CLK | — | These output pins may be left floating. |
| TSEC3_RX_CLK/FEC_RX_CLK/FI FO3_RX_CLK | — | Tie high or low through a 2–10 kΩ resistor to $TV_{DD}$ or GND, respectively. |

**Table 20. Ethernet Pin Recommendations (continued)**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| TSEC3_RX_DV/FEC_RX_DV/FIFO 3_RX_DV | — | Tie low through a 2–10 kΩ resistor to GND. |
| TSEC3_RX_ER/FEC_RX_ER/FIFO 3_RX_ER | — | Tie low through a 2–10 kΩ resistor to GND. |
| TSEC3_TX_CLK/FEC_TX_CLK/FIFO3_TX_CLK | — | Tie high or low through a 2–10 kΩ resistor to $TV_{DD}$ or GND, respectively. |
| TSEC3_TX_EN/FEC_TX_EN/FIFO 3_TX_EN | These pins require an external 4.7 kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively (during reset). | These output pins may be left floating. |
| TSEC4_TXD[3:2]/TSEC3_TXD[7:6] /FIFO3_TXD[7:6] | — | These output pins may be left floating. |
| TSEC4_TXD[1:0]/TSEC3_TXD[5:4] /FIFO3_TXD[5:4] | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | If the POR default is acceptable, this output pin may be left floating. |
| TSEC4_RXD[3:0]/TSEC3_RXD[7:4] /FIFO3_RXD[7:4] | — | Tie high or low through a 2–10 kΩ resistor to $TV_{DD}$ or GND, respectively. |
| TSEC4_GTX_CLK | — | These output pins may be left floating. |
| TSEC4_RX_DV/TSEC3_CRS/FEC _CRS/FIFO3_RX_FC | — | Tie low through a 2–10 kΩ resistor to GND. |
| TSEC4_TX_EN/TSEC3_TX_ER/FEC_TX_ER/FIFO3_TX_ER | These pins require an external 4.7 kΩ pull-down resistor to prevent PHY from seeing a valid Transmit Enable before it is actively (during reset). | These output pins may be left floating. |

# 12 $I^2C$ Interface

This section discusses the termination of $I^2C$ pins on the device. Table 21 shows how the $I^2C$ pins should be connected.

**Table 21. $I^2C$ Pin Recommendations**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| IIC1_SCL | Tie these open-drain signals high through a 1 kΩ resistor to $OV_{DD}$. | Tie high through a 2–10 kΩ resistor to $OV_{DD}$. |
| IIC2_SCL | | |
| IIC1_SDA | | |
| IIC2_SDA | | |

# 13 JTAG Interface

Correct operation of the JTAG interface requires the configuration of a group of system control pins as demonstrated in Figure 12. Care must be taken to ensure that these pins are maintained at a valid de-asserted state under normal operating conditions as most have asynchronous behavior and spurious assertion gives unpredictable results.

Boundary-scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE Std 1149.1™ specification, but it is provided on all processors built on Power Architecture™ technology. The device requires $\overline{\text{TRST}}$ to be asserted during power-on reset flow to ensure that the JTAG boundary logic does not interfere with normal chip operation. While the TAP controller can be forced to the reset state using only the TCK and TMS signals, generally systems assert $\overline{\text{TRST}}$ during the power-on reset flow. Simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical because the JTAG interface is also used for accessing the common on-chip processor (COP), which implements the debug interface to the chip.

The COP function of these processors allow a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources—such as voltage monitors, watchdog timers, power supply failures, or push-button switches—the COP reset signals must be merged into these signals with logic.

The arrangement shown in Figure 12 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ while ensuring that the target can drive $\overline{\text{HRESET}}$ as well.

The COP interface has a standard header, shown in Figure 11, for connection to the target system, and is based on the 0.025" square-post, 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

The COP header adds many benefits such as breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features. An inexpensive option can be to leave the COP header unpopulated until needed.

There is no standardized way to number the COP header, so emulator vendors have issued many different pin numbering schemes. Some COP headers are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom. Still others number the pins counter-clockwise from pin 1 (as with an IC). Regardless of the numbering scheme, the signal placement recommended in Figure 11 is common to all known emulators.

## 13.1 Termination of Unused Signals

If the JTAG interface and COP header will not be used, Freescale recommends the following connections:

- $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 kΩ isolation resistor so that it is asserted when the system reset signal ($\overline{\text{HRESET}}$) is asserted, ensuring that the JTAG scan chain is initialized during the power-on reset flow. Freescale recommends that the COP header be designed into the system as shown in Figure 12. If this is not possible, the isolation resistor allows future access to $\overline{\text{TRST}}$ in case a JTAG interface may need to be wired onto the system in future debug situations.

- No pull-up/pull-down is required for TDI, TMS, or TDO.

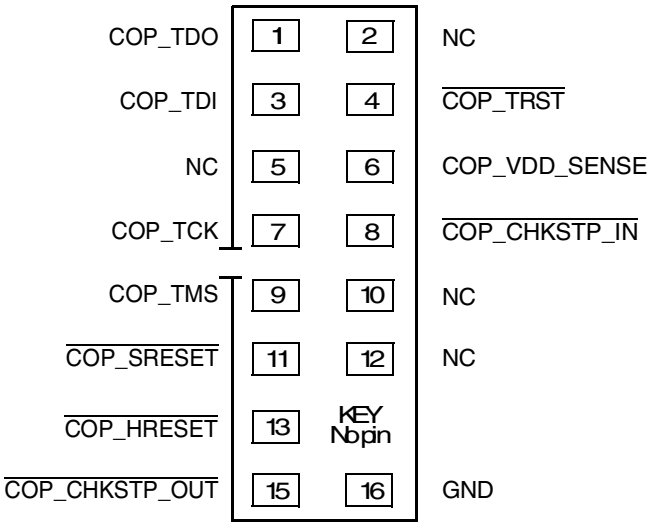
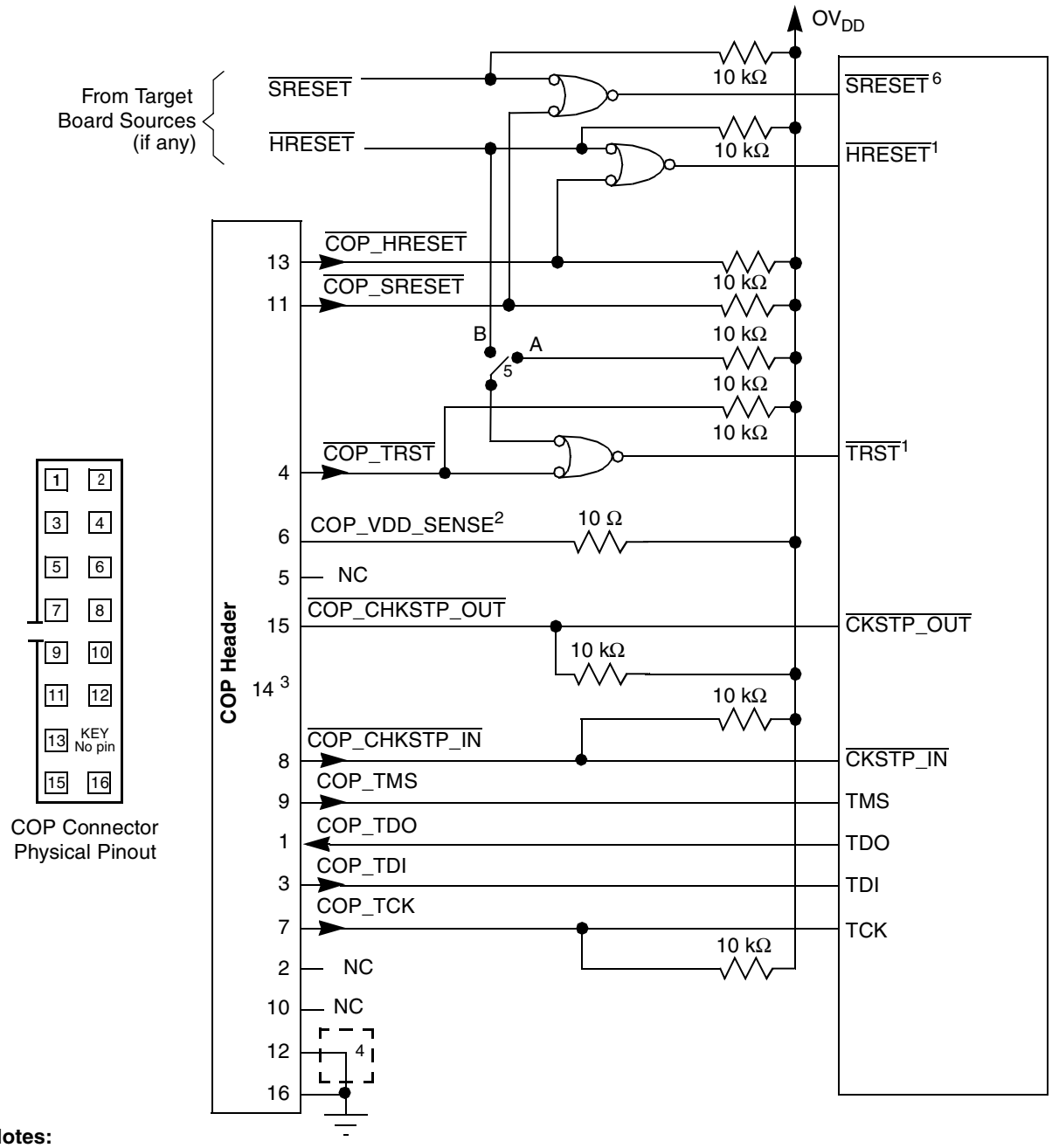



**Figure 11. COP Connector Physical Pinout**




**Notes:**

1. The COP port and target board should be able to independently assert $\overline{\text{HRESET}}$ and $\overline{\text{TRST}}$ to the processor in order to fully control the processor as shown here.
2. Populate this with a 10-Ω resistor for short-circuit/current-limiting protection.
3. The KEY location (pin 14) is not physically present on the COP header.
4. Although pin 12 is defined as a No Connect, some debug tools may use pin 12 as an additional GND pin for improved signal integrity.
5. This switch is included as a precaution for BSDL testing. The switch should be closed to position A during BSDL testing to avoid accidentally asserting the $\overline{\text{TRST}}$ line. If BSDL testing is not being performed, this switch should be closed to position B.
6. Asserting $\overline{\text{SRESET}}$ causes a machine check interrupt to the e500 core.

**Figure 12. JTAG Interface Connection**

## 13.2 JTAG Pins

Table 22 shows how the JTAG pins should be connected.

**Table 22. JTAG Pin Recommendations**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| TCK | If COP is used then connect as needed plus strap to OVDD via 10 K pullup. | If COP is unused; Tie TCK to OVDD through a 10 kΩ resistor. This will prevent TCK from changing state and reading incorrect data into the device. |
| TDI | This pin has a weak internal pull-up P-FET that are always enabled. Connect to Pin3 of the COP connector | This pin may be left unconnected. |
| TDO | Connect to Pin1 of the COP connector | This pin may be left unconnected. |
| TMS | This pin has a weak internal pull-up P-FET that are always enabled. Connect to Pin9 of the COP connector | This pin may be left unconnected. |
| $\overline{\text{TRST}}$ | This pin has a weak internal pull-up P-FET that are always enabled. Connect to Pin4 of the COP connector and $\overline{\text{HRESET}}$ from the board | $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0 Ω resistor. |

## 13.3 JTAG Checklist

Table 23 provides a summary POR and reset checklist for the designer.

**Table 23. Checklist for JTAG**

| Item | Description | Completed |
|---|---|---|
| 1. | Connect the JTAG pins to the COP header as shown in Figure 12. | |

# 14 Enhanced Local Bus Interface

This section discusses the termination of local bus pins on the device. Table 24 shows how the local bus pins should be connected.

**Table 24. Local Bus Pin Recommendations**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| LA[27] | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | If the POR default is acceptable, this output pin may be left floating. |
| LA[28] | | |
| LA[29:31] | This pin is a reset configuration pin that sets the CCB clock to SYSCLK PLL ratio. These pins require 4.7 kΩ pull-up or pull-down resistors. | |
| LAD[0:31] | Note that the LSB for the address = LAD[24:31]; however, the MSB for the data is on LAD[0:7]. | Tie high or low through a 2–10 kΩ resistor to $BV_{DD}$ or GND, respectively, if the general purpose POR configuration is not used. |
| LALE | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | If the POR default is acceptable, this output pin may be left floating. |
| LBCTL | | |

**Table 24. Local Bus Pin Recommendations (continued)**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| LCLK[0:2] | — | These output pins may be left floating. |
| $\overline{\text{LCS}}$[0:4] | | |
| LDP[0:3] | — | Tie high or low to the inactive state through a 4.7 kΩ resistor to $BV_{DD}$ or GND, respectively. |
| $\overline{\text{LCS}}$[5]/$\overline{\text{DMA2\_DREQ}}$[1] | — | If the DMA functions of these pins are not used, these output pins may be left floating. |
| $\overline{\text{LCS}}$[6]/$\overline{\text{DMA2\_DACK}}$[1] | — | |
| $\overline{\text{LCS}}$[7] /$\overline{\text{DMA2\_DDONE}}$[1] | — | |
| LGPL0/LFCLE | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | If the POR defaults are acceptable, these output pins may be left floating. |
| LGPL1/$\overline{\text{LFALE}}$ | | |
| LGPL2/$\overline{\text{LOE}}$/$\overline{\text{LFRE}}$ | | |
| LGPL3/$\overline{\text{LFWP}}$ | | |
| LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/ LPBSE/LFRB | — | This pin either needs to be pulled-up via a 2–10 kΩ resistor to $BV_{DD}$ or needs to be reconfigured as LPBSE prior to boot-up. |
| LGPL5 | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | If the POR default is acceptable, this output pin may be left floating. |
| LSYNC_IN | LSYNC_IN needs to be connected via a trace to LSYNC_OUT of length equal to the longest LCK*n* signal used. | LSYNC_IN needs to be directly connected to LSYNC_OUT. |
| LSYNC_OUT | | |
| $\overline{\text{LWE0}}$/$\overline{\text{LBS0}}$/$\overline{\text{LFWE}}$ | This pin is a reset configuration pin. It has a weak internal pull-up P-FET which is enabled only when the processor is in the reset state. | If the POR defaults are acceptable, these output pins may be left floating. |
| $\overline{\text{LWE}}$[1:3]/$\overline{\text{LBS}}$[1:3] | | |

# 15 PIC Interface

This section discusses the termination of programmable interrupt controller (PIC) pins on the device. Table 25 shows how the PIC pins should be connected.

**Table 25. PIC Pin Recommendations**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| IRQ[0:11] | A weak pull-up or pull-down may be needed to the inactive state. | Tie high or low to the inactive state through a 2–10 kΩ resistor to $OV_{DD}$ or GND, respectively, |

**Table 25. PIC Pin Recommendations (continued)**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| $\overline{\text{IRQ\_OUT}}$ | Pull high through a 2–10 kΩ resistor to $OV_{DD}$. | |
| $\overline{\text{MCP\_0}}$ | | |
| $\overline{\text{MCP\_1}}$ | | |
| $\overline{\text{UDE0}}$ | | |
| $\overline{\text{UDE1}}$ | | |

# 16 SerDes Interface

This section discusses the termination of SerDes pins on the device. Table 26 and Table 27 show how the SerDes pins should be connected. Note that the SerDes must always have power applied to its supply pins. Also note that a valid clock input is required on SD1_REF_CLK if SerDes1 is enabled, and a valid clock input is required on SD2_REF_CLK if SGMII SerDes is enabled. Failure to provide a reference clock for an enabled SerDes block prevents the device from completing POR sequence.

**Table 26. SerDes1 Pin Recommendations**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| SD1_PLL_TPD | Do not connect. | |
| SD1_PLL_TPA | | |
| SD1_RX[0:7] | — | These pins must be connected to GND. |
| $\overline{\text{SD1\_RX}}$[0:7] | | |
| SD1_TX[0:7] | — | These pins must be left unconnected. |
| $\overline{\text{SD1\_TX}}$[0:7] | | |
| SD1_IMP_CAL_RX | This pin must be pulled down through a 200 Ω (±1%) resistor. | |
| SD1_IMP_CAL_TX | This pin must be pulled down through a 100 Ω (±1%) resistor. | |
| SD1_REF_CLK | If SerDes1 is enabled via POR config pins, connect to a clock at the frequency specified per the POR I/O Port Selection. [1] | These pins must be connected to XGND_SRDS1. |
| $\overline{\text{SD1\_REF\_CLK}}$ | If SerDes1 is enabled via POR config pins, connect to a clock at the frequency specified per the POR I/O Port Selection.[1] | These pins must be connected to XGND_SRDS1. |

**Note:**

1 If SerDes is enabled, corresponding SerDes Reference Clock must be provided to successfully complete POR.

**Table 27. SerDes2 Pin Recommendations**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| SD2_PLL_TPD | Do not connect. | |
| SD2_PLL_TPA | | |
| SD2_RX[0:3] | — | These pins must be connected to GND. |
| $\overline{\text{SD2\_RX}}$[0:3] | | |
| SD2_TX[0:3] | — | These pins must be left unconnected. |
| $\overline{\text{SD2\_TX}}$[0:3] | | |
| SD2_IMP_CAL_RX | This pin must be pulled down through a 200 Ω (±1%) resistor. | |
| SD2_IMP_CAL_TX | This pin must be pulled down through a 100 Ω (±1%) resistor. | |
| SD2_REF_CLK | If SGMII SerDes is enabled via POR config pins, connect to a clock at the frequency specified per the POR I/O Port Selection. [1] | These pins must be connected to XGND_SRDS2. |
| $\overline{\text{SD2\_REF\_CLK}}$ | If SGMII SerDes is enabled via POR config pins, connect to a clock at the frequency specified per the POR I/O Port Selection.[1] | These pins must be connected to XGND_SRDS2. |

1 If SerDes is enabled, corresponding SerDes Reference Clock must be provided to successfully complete POR.

# 17 System Control

This section discusses the termination of system control pins on the device. Table 28 shows how the system control pins should be connected.

**Table 28. System Control Pin Recommendations**

| Pin Name | Pin Used | Pin Not Used |
|---|---|---|
| $\overline{\text{CKSTP\_IN0}}$ | Pull high through a 2–10 kΩ resistor to $OV_{DD}$. Connect to Pin7 of the COP connector (refer to Figure 12). | Pull high through a 2–10 kΩ resistor to $OV_{DD}$. |
| $\overline{\text{CKSTP\_IN1}}$ | | |
| $\overline{\text{CKSTP\_OUT0}}$ | Pull this open-drain signal high through a 2–10 kΩ resistor to $OV_{DD}$. Connect to Pin15 of the COP connector (refer to Figure 12). | This pin may be left unconnected. |
| $\overline{\text{CKSTP\_OUT1}}$ | | |
| $\overline{\text{HRESET}}$ | Pull high through a 2–10 kΩ resistor to $OV_{DD}$. Connect to Pin13 of the COP connector (refer to Figure 12). | |
| $\overline{\text{HRESET\_REQ}}$ | Pull high through a 2–10 kΩ resistor to $OV_{DD}$. This pin must NOT be pulled down during power-on reset. | This pin must NOT be pulled down during power-on reset. |
| $\overline{\text{SRESET}}$ | Pull high through a 2–10 kΩ resistor to $OV_{DD}$. Connect to Pin11 of the COP connector (refer to Figure 12). | Pull high through a 2–10 kΩ resistor to $OV_{DD}$. |

# 18 Power and Ground Signals

The MPC8572 has several power supplies. Table 29 describes each of the power supplies.

**Table 29. Power and Ground Pin Recommendations**

| Pin | Comment |
|---|---|
| $AV_{DD}$_CORE0 | Power supply for Core0 PLL (1.1 V through a filter) |
| $AV_{DD}$_CORE1 | Power supply for Core1 PLL (1.1 V through a filter) |
| $AV_{DD}$_DDR | Power supply for DDR (1.1 V through a filter) |
| $AV_{DD}$_LBIU | Power supply for Local Bus PLL (1.1 V through a filter) |
| $AV_{DD}$_PLAT | Power supply for core complex bus PLL (1.1 V through a filter) |
| $AV_{DD}$_SRDS1 | Power supply for SerDes 1 PLL (1.1 V through a filter) |
| $AV_{DD}$_SRDS2 | Power supply for SerDes 2 PLL (1.1 V through a filter) |
| $BV_{DD}$ | Power supply for the Local Bus I/Os and GPIO (1.8 V/2.5 V/3.3 V) |
| GND | Ground |
| $GV_{DD}$ | Power supply for the DDR I/Os (1.8 V/2.5 V) |
| $LV_{DD}$ | Power supply for TSEC1&2 I/Os (2.5 V/3.3 V) |
| MVREF | DDR input reference voltage equal to approximately half of $GV_{DD}$ |
| $OV_{DD}$ | General I/O Supply (3.3 V) |
| SENSEVDD | This pin is connected to the $V_{DD}$ plane internally and may be used by the core power supply to improve tracking and regulation. |
| SENSEVSS | This pin is connected to the GND plane internally and may be used by the core power supply to improve tracking and regulation. |
| $SV_{DD}$_SRDS1 | Power for SerDes 1 Logic (1.1 V) |
| $SV_{DD}$_SRDS2 | Power for SerDes 2 Logic(1.1 V) |
| $XV_{DD}$_SRDS1 | Pad Power for SerDes 1 transceivers (1.1 V) |
| $XV_{DD}$_SRDS2 | Pad Power for SerDes 2 transceivers (1.1 V) |
| XGND_SRDS1 | SerDes 1 Transceiver Pad GND |
| XGND_SRDS2 | SerDes 2 Transceiver Pad GND |
| SGND_SRDS1 | SerDes 1 Logic GND |
| SGND_SRDS2 | SerDes 2 Logic GND |
| AGND_SRDS1 | SerDes 1 PLL GND |
| AGND_SRDS2 | SerDes 2 PLL GND |
| $TV_{DD}$ | Power supply for the TSEC3&4 I/Os (2.5 V/3.3 V) |
| $V_{DD}$ | Power supply the core logic (1.1 V) |

# 19 Documentation History

Table 30 provides a revision history for this application note.

**Table 30. Document Revision History**

| Revision | Date | Substantive Change(s) |
|---|---|---|
| 2 | 06/2009 | • Added row for silicon version 2.1 in Table 1, “Revision Level to Part Marking Cross-Reference.”<br>• In Section 11, “eTSEC Interface,” updated recommendation for TSEC_1588_CLK and TSEC_1588_TRIG_IN.<br>• In Section 6, “DDR Interface,” added recommendation for MAPAR_OUT.<br>• In Section 15, “PIC Interface,” added recommendation for $\overline{\text{UDE0}}$ and $\overline{\text{UDE1}}$.<br>• In Section 14, “Enhanced Local Bus Interface,” updated recommendation for LDP[0:3]. |
| 1 | 04/2009 | • Changed title of Figure 4 from “MPC8572E Pin Map Top View” to “MPC8572E Pin Map Bottom View.” |
| 0 | 03/2009 | • Initial release. |

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