Freescale Semiconductor
Application Note

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MPC551x Clock Generation and Usage

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1 Introduction

The MPC551x is the newest family in Freescale Semiconductor’s MPC5500 Power Architecture family of 32-bit microcontrollers, leaders in the automotive market. The MPC551x is the latest generation of low-power, high-performance microcontrollers targeted primarily at the market for automotive body control and gateway devices.

With a focus on performance and low power in this new family, many features have been optimized. These features therefore differ from the parent family of the MPC55xx, which has traditionally been focused on automotive powertrain applications. For example, the clock generation for the MPC551x now offers four separate clock sources that allow the programmer more flexibility in customizing the application to the lowest system power. These four clock sources are:

- 32k OSC (32–40 kHz external oscillator)
- 32k IRC (32 kHz internal oscillator)

Contents

- XOSC (4–40 MHz external oscillator or external clock input)
- 16 MHz IRC (16 MHz internal oscillator)

There is also the standard PLL normally used for clock multiplication, which could also be used for clock generation in the event of external oscillator failure of the XOSC. There are several clock switching muxes and dividers used throughout the chip. Figure 1 shows the main clock generation and switching. Figure 2 shows the clock generation and switching for the RTC/API (Real Time Clock, Autonomous Periodic Interrupt) and wakeup from low-power mode logic.

This application note focuses on the clock sources for this new family and is intended to describe the various clock sources and their inter-relationships in a relatively simple and logical manner. For in-depth descriptions of the specific sources and their intended use, please consult the *MPC5510 Microcontroller Family Reference Manual* available at www.freescale.com.

2 Generation of System Clock

The MPC551x family always uses the 16 MHz IRC at power-on reset and any other resets. Exiting from lower power modes is really an internal reset, so at every exit from one of the low power modes (sleep or stop) the 16 MHz IRC provides the system clock. This 16 MHz IRC is used not only for the internal logic sequencing out of reset, but also for the system clock after exiting reset. The user can subsequently switch to another clock source as necessary.

At power-on reset the XOSC (4–40 MHz external oscillator) is powered and routed to the PLL, but again, it is not used unless selected by the customer’s code. Under user control by software, the XOSC can be on or off while the part is in a low-power mode, and will stay in the same state as the part exits the low-power mode. Basically, if the XOSC was turned off as the low-power mode was entered, then it will not be powered on at the exit of the low-power mode unless some specific code turns it back on (unless the exit was a power-on or external reset).

Note that all modules that can use the XOSC clock directly (FlexRay, FlexCan, RTC) should only be set up to run off the XOSC after the user knows that the oscillator is running and stable.

If the customer wants to increase the system clock (faster than the 16 MHz IRC) the normal way would be to use the XOSC and the PLL. The XOSC input can either be an external crystal or an external clock driven into EXTAL. While the customer could use only the XOSC and not use the PLL, care must be taken because there is no clock-quality checker on the XOSC. Therefore, switching to the XOSC without a stable oscillation could cause unexpected results (runaway code, etc.). The easiest way of verifying that the XOSC oscillation is stable would be to use the PLL lock detection, since it requires about 150 reference clocks (after the PLL is accurately tracking the input reference) for the PLL to be locked. You can use the loss of lock and/or loss of clock signals even without using the PLL for the system clock. You could also do a simple time delay, set to a period slightly longer than the longest expected stabilization time (calculated from system characterization).

To use the PLL you need to have XOSC on and an external 4–40 MHz oscillator circuit attached (or be driving an external clock into EXTAL). This oscillator is an amplitude-controlled circuit (Pierce mode configuration) so the use of fundamental frequency oscillators is recommended. See the *MPC5510 Microcontroller Family Reference Manual* for further details.

3 XOSC Frequency Selection

There are a few things to consider when selecting the XOSC frequency. While there is the capability to run the FlexRay module from the system clock, it is recommended that you use a 40 MHz oscillator (and drive the module from the crystal input) due to the limited temperature operation (for 80 MHz system clock) and tight timing requirements of the FlexRay communication. If you are planning on using a high speed CAN communication, you may also want to use the oscillator to drive the CAN module (again, for reduced jitter). The last considerations are things like crystal startup time, EMC radiation, XOSC power requirements, standard customer parts, etc.

To set up the PLL for the system clock you have to consider a few things:

- The reference frequency needs to be between 4 MHz and 10 MHz (the options are to divide the XOSC by 1, 2, 3, 4, 5, 6, 8, 10).
- The output frequency of the PLL needs to be between 192 MHz and 500 MHz (the options are to multiply the reference from 48 to 148).
- The PLL output frequency has to be divided by an even number in the range 4–64 to achieve the desired system clock frequency (the options are divide by 1 to 64, but you can only use divide by 4 to 64 or you exceed the maximum bus frequency).

For example, if you want to use a 40 MHz fundamental frequency oscillator (using XOSC for FlexRay) and you want to achieve a 66 MHz final system clock speed, then you can calculate the PLL register settings in this way:

1. Working backwards from the desired system clock speed of 66 MHz, you can determine that the only allowable PLL output dividers (ERFD) are four or six. Dividing by two would mean the PLL output was too slow (66 × 2 = 132 — minimum PLL clock is 192 MHz) and divide by eight would mean the PLL output clock was too fast (66 × 8 = 528 — maximum PLL clock is 500 MHz). So you need a PLL output clock of either 264 MHz (4 × 66) or 396 MHz (6 × 66).
2. Determine the potential PLL reference frequencies that you can get with the XOSC. With a 40 MHz fundamental frequency oscillator, you can divide by 4, 5, 6, 8, or 10 (dividing by three would give you a PLL reference frequency that would be too fast, because 10 MHz is the maximum), giving you possible PLL reference frequencies of 10, 8, 6.66, 5, or 4 MHz.
3. The only reference frequencies that are even factors of our desired output frequencies of 264 MHz or 396 MHz are 8 MHz or 4 MHz. So use either a 4 MHz reference with 396 MHz PLL clock (or 264 MHz) or use an 8 MHz reference with 264 MHz PLL clock. There are several things that determine which frequency to use, but generally speaking, the higher the PLL clock the less jitter you will have on your system clock (at the sacrifice of slightly higher I_{DD} currents). For our example we choose the 4 MHz PLL reference and 396 MHz PLL output clock. Depending on your desired system clock speed and desired XOSC frequency, you may not be able to exactly achieve both, and may have to change one of them to fit within the total system requirements.
4. To calculate the reference divider you must first determine what PLL reference frequency you will use. (This was done in steps 2 and 3 above.) In this example we want a 4 MHz reference, so we need a divide value of 10. (We have a 40 MHz input, therefore 40/4 = 10.) Subtract one from that number to calculate the value you load for the reference divider. So in this example 10 – 1 = 9, or 0b1001, to be loaded into the EPREDIV bits.

5. Calculate the EMFD (PLL multiplier) to generate your calculated PLL output frequency from step 3 (in this case it is 396 MHz).

   To do this, just take your desired PLL output frequency / PLL reference frequency – 16 (decimal). So 396/4=99, 99–16=83, or in other words 0b0101_0011 needs to be loaded into the EMFD bits.
6. Finally, calculate the ERFD to divide the PLL output clock down to the desired frequency (66 MHz in our case). So 396/6 = 66 MHz. Subtract one from that number to calculate the value you load for the post divider. So in this example 6 – 1 = 5; therefore load 0b0101 into the ERFD bits.

PLL usage summary: Using XOSC = 40 MHz, EPREDIV = 9, EMFD = 83, ERFD = 5 gives the following:

- XOSC = 40 MHz
- PLL reference = 4 MHz
- PLL speed = 396 MHz
- PLL post divider clock = 66 MHz

NOTE

> While not as critical as with other PowerPC parts, (because you normally are running off the 16 MHz IRC when setting up the PLL on the MPC551x), it is still recommended that when setting up the PLL to first set the post divider to a larger divider than your final divider. If the PLL overshoots the frequency (as it acquires lock) the output frequency will not exceed the part specification. After the PLL setup is complete and it is locked, rewrite the post divider to your desired frequency. Also enable the loss of clock, so if the XOSC fails the part can switch to another clock source (best practice is to reset into the 16 MHz IRC).

There is another divider in the system clock path after the PLL post divider (ERFD) called SYSCLKDIV (in the SIU module), but this divider is only needed for low-power operation. Basically it can divide the system clock down by 1, 2, 4, or 8, and is set to divide by 1 by default (reset). See Figure 1.

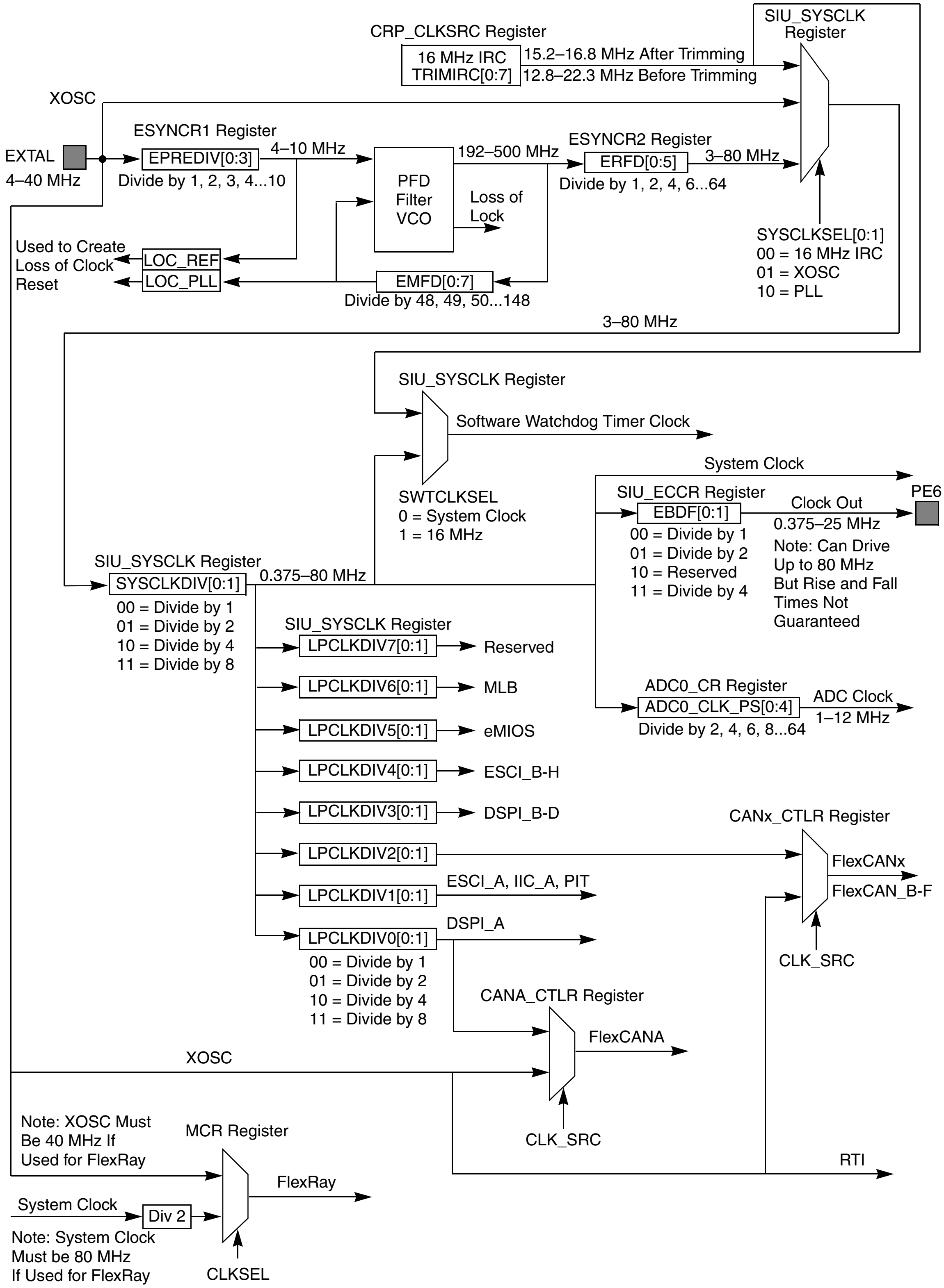

Figure 1. Main Clock Generation and Switching for the MPC551x Family

The software watchdog timer clock is, by default (reset), set to the system clock (at reset the 16 MHz IRC runs the bus) but can be switched to run off just the 16 MHz IRC even if the bus clock source is changed. Note that if you are switching the clock source for the software watchdog timer, you must turn it off before the change. The switchover is not synchronized and could cause unexpected operation if the clock is left running.

4 Clock Generation for RTC/API

This section discusses generation of the clock for real time counter/autonomous periodic interrupt and the clock source for wakeup logic and edge detection.

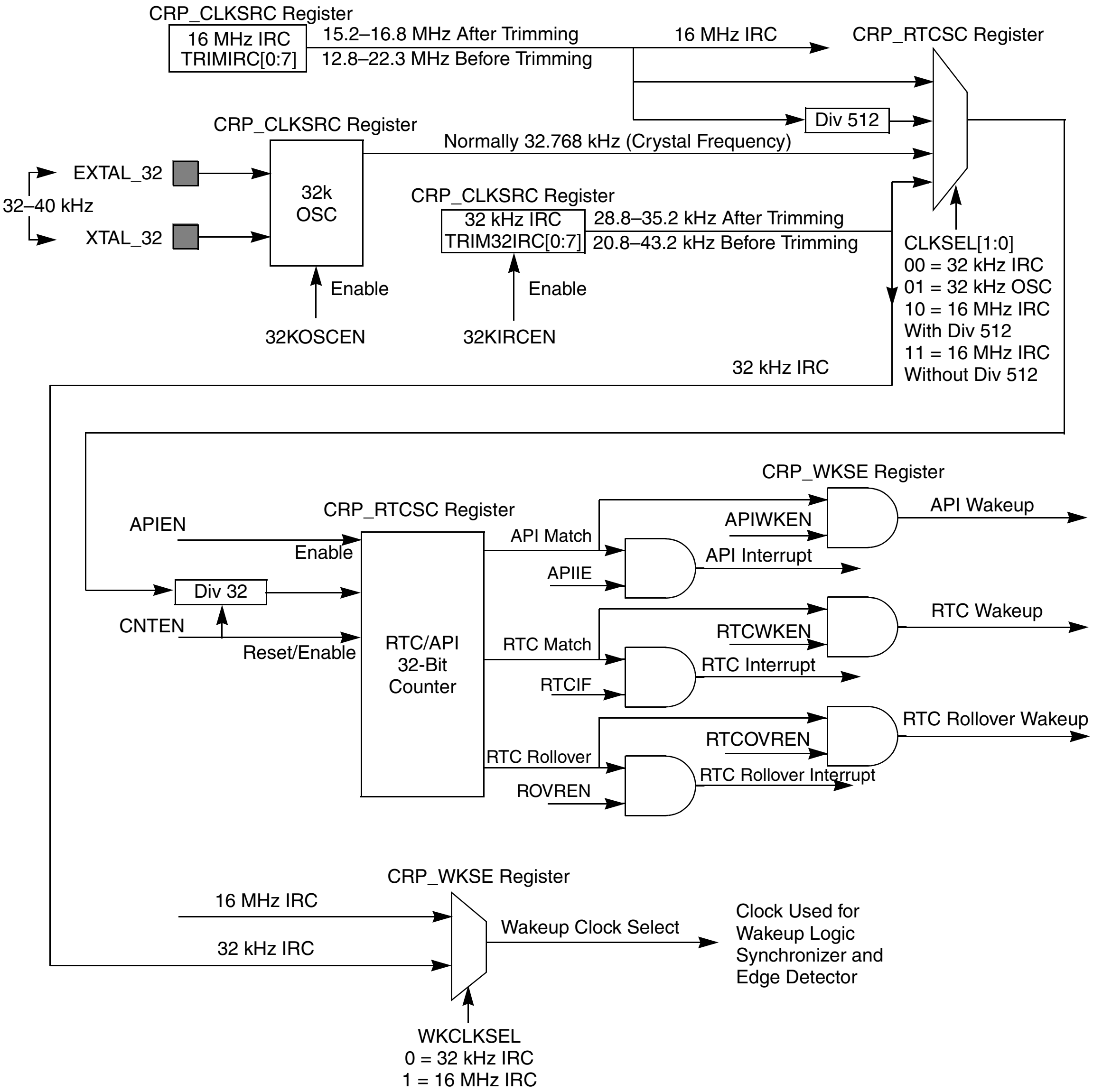

Figure 2. RTC/API and Wakeup from Low Power Modes Clock Generation and Switching for the MPC551x Family

The RTC can have two different clock periods. The most common usage period is a 1 ms interval (lsb count value). The API uses the first ten bits (0 to 9) of the counter giving it a 1 ms to 1 s range. The RTC uses the next twelve bits (10 to 21) giving it a range from 1 s to 4096 s (over 1 hour). See Figure 2.

The other optional usage period is a 2 µs interval (lsb count value). Again, the API uses the first ten bits (0–9) of the counter giving it a 2 µs to 2 ms range. The RTCVAL uses the next twelve bits (10 to 21) giving it a 2 ms to more than 8 s range.

The 1 ms period can be generated from three different sources. The first source is the internal 32 kHz IRC, the second source is the 32 kHz OSC, and the third source is the internal 16 MHz IRC divided down by 512.

The main advantages to each different source are:

- If you are trying to do real-time clock, then you will want to use an external 32.768 crystal, since that can be designed to a low ppm accuracy.
- If you want the lowest power but do not require the low ppm level accuracy of the 32 kHz OSC, then you can use the internal 32 kHz IRC. This oscillator will start up between 20.8 kHz to 43.2 kHz, and will be within 28.8 kHz to 35.2 kHz over temperature and V_{DD} levels after loading the factory-provided value into the 32 kHz trim register (CRP_CLKSRC register TRIM32IRC bits). Customers can also further improve the accuracy by using their own trim procedure (for example, changing the trim values over temperature and voltage levels).
- If you need the fastest external pin wakeup (at the expense of higher current) then you will want to use the 16 MHz IRC, since it takes two clocks minimum for a wakeup signal to get through the edge detection circuit. You also get a slightly more accurate time base than the 32 kHz IRC, since the 16 MHz IRC will be 12.8 MHz to 22.3 MHz (25 kHz to 43.6 kHz after divider) before trimming and then 15.2 MHz to 16.8 MHz (29.7 kHz to 32.8 kHz after divider) after loading the factory-provided trim values (over temperature and V_{DD}).

The other period that can be run to the RTC/API is a 2 µs resolution. This is done by feeding the 16 MHz IRC without the divide-by-512.

NOTE

The 32 kHz OSC is a very low-power amplitude-controlled oscillator. Extreme care should be used to avoid any stray loading on the circuit. Very small external loading (from a typical automotive system point of view), either resistive and/or capacitive, can prevent or, at minimum, greatly affect its operation.

5 Summary

The new features that have been added to the clock sources make the MPC551x an ideal part for automotive body applications where the end user wants to be able to switch between high performance and various low-power modes.

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