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Application Note

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MPC5566 to MPC5674F Migration Guide

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1 Introduction

This document provides a summary of the significant differences in the MPC5566 and MPC5674F devices, and may be used as a help for planning a migration to the MPC5674F. (The information provided in this application note also applies to any other device in the MPC567xF family.)

Note that the MPC5674F is available in both 416-pin and 516-pin packages and function of the device varies according to the package chosen. Where applicable, these differences are highlighted in the accompanying text.

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2 Overview

Table 1 provides a summary of the feature differences between the MPC5566 and MPC5674F devices.

Table 1. MPC5566/MPC5674F Feature Comparison

Feature	MPC5566	MPC5674F
Process	130 nm	90 nm
Core	e200z6	e200z7
SIMD	Yes	Yes
VLE	Yes	Yes
Cache	32 KB	32 KB (16 KB I/16 KB D)
Non-maskable interrupt (NMI)	No	NMI & Critical Interrupt[1]
MMU	32-entry	64-entry
Memory Protection Unit (MPU)	No	Yes
XBAR	4x5	6x5
Windowing software watchdog (SWT)	No	Yes
Core Nexus	3+	3+
SRAM	128 KB	256 KB
Flash	3 MB	4 MB
Flash fetch accelerator	2 × 256 bit	4 × 256 bit
External bus	32-bit	Yes[2]
Calibration bus	16-bit	16-bit non-multiplexed 32-bit multiplexed
DMA	64-channel	96-channel
DMA Nexus	Class 3	Class 3
Serial	Two	Three
eSCI_A	Yes	Yes
eSCI_B	Yes	Yes
eSCI_C	No	Yes
FlexCAN	Four	Four
CAN_A	64 buf	64 buf
CAN_B	64 buf	64 buf
CAN_C	64 buf	64 buf
CAN_D	64 buf	64 buf
SPI	Four	Four
DSPI_A	Yes	Yes
DSPI_B	Yes	Yes
DSPI_C	Yes	Yes

Table 1. MPC5566/MPC5674F Feature Comparison (continued)

Feature	MPC5566	MPC5674F
DSPI_D	Yes	Yes
Microsecond bus support	No	Yes
FlexRay	No	Yes
Ethernet	Yes	No
System timers	No	Eight PIT channels Four AutoSAR One Watchdog
eMIOS	24-channel	32-channel
eTPU	64-channel	64-channel
eTPU_A	Yes	Yes (eTPU2)[3]
eTPU_B	Yes	Yes (eTPU2)[3]
Code memory	20 KB	24 KB
Data memory	4 KB	6 KB
Interrupt controller	308-channel	448
eQADC	40-channel, two ADCs	64-channel, four ADCs
eQADC_A (2 ADCs)	Yes	Yes
eQADC_B (2 ADCs)	No	Yes
Temperature sensor	No	Yes
Variable gain amp.	No	Yes
Decimation filter	No	Yes (four)
Sensor diagnostics	No	Yes
PLL	FM	FM
VRC	Yes	Yes
Supplies	5 V, 3.3 V, 1.5 V	5 V, 3.3 V, 1.2 V
Low Power Modes	No	Stop Mode[1] Slow Mode[1]

1 Only available on revision 2 release of device.

2 External bus interface (EBI) is available on 496 and 516 PBGA.

3 eTPU2 only available on revision 2 release of device.

3 Memory

This section provides details of the differences in the memory, including information that is relevant for porting the application to the MPC5674F.

3.1 SRAM

The MPC5674F has 256 KB of SRAM, compared to the 128 KB of SRAM on the MPC5566. If the extra SRAM is to be used, the application initialization code must be modified so that it initializes all SRAM up to 256 KB. Additionally, any linker directive files must be updated to reflect the change in the memory map.

The MPC5674F ECC supports single-bit error reporting for SRAM memory.

3.2 Flash

- The MPC5674F has 4 MB of flash memory,[1] increased from the 3 MB of flash memory on the MPC5566.
- The MPC5674F requires a different flash-programming algorithm that will be provided by FSL as a software driver. Any proprietary flash-programming algorithms or drivers must be re-coded for the MPC5674F.
- The MPC5674F ECC supports single-bit error reporting for flash memory.
- There are now two sets of control registers, one for each flash array.
- Any PC tools used for programming flash will need to be updated.
- The flash block sizes have changed as shown in Table 2.

Table 2. MPC5566 vs. MPC5674F Flash Partitions

MPC5566		MPC5674F			
		Array A		Array B	
Block Size	Use	Block Size	Use	Block Size	Use
2 x 16 K 2 x 48 K 2 x 64 K	Low Address Space	8 x 16 K 2 x 64 K	Low Address Space		
		2 x 128 K	Mid Address Space		
				256 K	Low Address Space
				256 K	Mid Address Space
2 x 128 K	Mid Address Space	6 x 256 K	High Address Space	6 x 256 K	High Address Space
20 x 128 K	High Address Space				

1. The MPC5673F has 3 MB of flash memory.

4 Core

The MPC5674F employs the e200z7 core, instead of the e200z6 core used on the MPC5566. The e200z7 core is instruction-set equivalent with the e200z6 core, however some new instructions and features are added to the e200z7. The essential differences in the two cores are described in the following bullets.

- VLE — The MPC5674F provides several new VLE instructions that are designed to maximize performance when the core is saving and restoring context. Existing e200z6 VLE code will execute without modifications on the e200z7 core. Not all tool partners will support these new instructions initially.
- MMU Entries — The number of MMU entries has been increased from 32 to 64 on the MPC5674F. The MMU entries initialized by the BAM are unchanged, and existing code that relies on the BAM initialization will execute correctly.
- Cache — The cache size remains 32 KB, however the architecture has been changed from a unified 32K type cache to a Harvard type cache, with 16 KB for data and 16 KB for instruction storage. Three new registers associated with the instruction cache block are added; L1CFG1, L1CSR1, and LFINV1. Cache initialization code must be modified to include both blocks. The unified cache on existing e200z6 cores is initialized and locked using the data cache instructions, therefore code that puts the stack into the cache does not need to be modified.
- Non-Maskable Interrupts (NMI) — The MPC5674F provides a new NMI that can be used to generate a non-maskable interrupt to the core. No software changes are required unless this new feature is to be used.
- The Machine Check exception has been modified. Existing code for handling machine check must be modified to clear the machine check cause in the MCSR register. Refer to Freescale document e200z7RM, *e200z7 PowerPC™ Core Reference Manual*, for details.
- SIMD — The MPC5674F employs the new SPE2 instruction set that provides expanded signal processing capability. SPE2 is a superset of the existing SPE library. Any existing SPE code does not require modification.

5 Peripherals

5.1 Memory Protection Module (MPU)

The MPC5674F provides a new memory protection module (MPU). This module provides programmable access control for most of the memory map on a bus-master permission basis. By default, the MPU is not enabled and no changes to existing code are required.

5.2 XBAR

The XBAR on the MPC5674F supports six masters and five slaves, instead of the 4 × 5 configuration used on the MPC5566. Table 3 and Table 4 provide a list of the XBAR port assignments and associated masters. If existing software makes modifications to the default master priorities, the code may require changes to support the additional masters. Note also that some Master/Slave IDs have changed.

Table 3. MPC5566 XBAR Master/Slave Detail

Module	XBAR port	Master ID
e200z6 Instruction/data	Master 0	0
e200z6 Nexus		1
DMA	Master 1	2
EBI	Master 2	3
FEC	Master 3	4

Table 4. MPC5674F XBAR Master/Slave Detail

Module	XBAR port	Master ID
e200z7 Instruction	Master 0	0
e200z7 Data	Master 1	0
e200z7 Nexus		8
DMA_A	Master 4	4
DMA_B	Master 5	5
FlexRay	Master 6	6
EBI	Master 7	7

5.3 SIU

The SIU for MPC5674F has several changes that may impact the application.

- The SIU for the MPC5674F supports many additional pin functions, and the associated pad configuration registers may have changed for many pads due to a completely new ball map.
- The PCR[PA] bit definitions have changed. All existing PCR configurations should be verified for correct functioning.
- There is a new IMUX. Existing DSP and eQADC configurations have changed.
- Support has been added for a new NMI and critical interrupt.

5.4 Windowing Software Watchdog

The MPC5674F provides a new watchdog module. Also, a new bit is available in the Reset Config Halfword (RCHW) that will disable this watchdog if the BAM is executed. However, debuggers do not normally run the BAM so debuggers must also disable the software timer. If not disabled by the RCHW and if booting from flash, software must disable the software early in the initialization sequence.

Legacy watchdog operation from previous e200z6 core using the core TCR and TSR registers is still supported. If this core-provided watchdog is used, the code needs modification to adjust time out values due to the higher operating frequencies of the MPC5674F.

5.5 Nexus

The MPC5566 supports Nexus 3+ 2003 standard and the MPC5674F supports Nexus 3+ 2008 standard. Some messages and message formats may have changed. The MPC5566 may use either four or twelve MDO pins. The MPC5674F may use either twelve or sixteen MDO pins.

5.6 External Bus Interface (EBI)

The MPC5566 provides a 32-bit data, 26-bit address, non-multiplexed external bus interface. The 516 PBGA package provides a configurable external bus intended for calibration use. It supports either 32-bit muxed mode or 16-bit non-muxed mode.

5.7 Calibration Bus

The MPC5566 provides a 16-bit non-muxed calibration bus. The MPC5674F does not provide a calibration bus in the 416 PBGA package. The 516 PBGA package provides the EBI described in Section 5.6 that may be used for calibration, or the calibration bus is available in the 416 VertiCal package.

5.8 eDMA

The MPC5566 provides a 64-channel DMA engine. The MPC5674F provides 96 channels of DMA. The first 64 channels are identical to the MPC5566 and the additional 32 channels support the new Decimation Filters and the second ADC. No software modifications are required unless the new Decimation Filters or ADC are to be used. The MPC5674F supports misaligned accesses by the DMA.

5.9 eSCI

The MPC5566 provides two eSCI ports, eSCI A, and eSCI B. The MPC5674F provides an additional eSCI port, eSCI C. The programming model for the eSCI registers has changed slightly.
The ESCI_LCR[LDBG] bit has been removed and this function no longer exists. Existing eSCI code should be inspected to ensure correct operation.

5.10 FlexCAN

The MPC5566 and MPC5674F both provide four FlexCAN modules with 64 message buffers in each module. No software modification is required.

5.11 DSPI

Both the MPC5566 and the MPC5674F provide four DSPI modules. However, the MPC5674F also provides support for the Microsecond Bus downlink. Normal DSPI operation does not require modification to software.

5.12 FlexRay

The MPC5674F provides a FlexRay module with two FlexRay TX/RX units. Note that the FlexRay module requires the external oscillator or crystal frequency to be 40 MHz. See also Section 5.21.

5.13 FEC

The MPC5566 provides a Fast Ethernet Controller (FEC). The MPC5674F does not provide the FEC.

5.14 System Timers (STM)

The MPC5566 does not provide a system timer module (STM). This new module has been added to the MPC5674F to provide support for certain OS timing requirements. The STM is inactive from reset, and there is no software change required if the STM is not needed.

5.15 eMIOS

The MPC5566 has 24 orthogonal eMIOS channels. The MPC5674F provides an additional eight channels that are fully orthogonal. Existing configuration and channel servicing code will operate unmodified.

5.16 eTPU

- Both the MPC5566 and the MPC5674F devices provide two eTPUs with 64 channels total. The MPC5674F incorporates the eTPU2 module. The code memory size has been increased from 20 KB to 24 KB, and the parameter RAM increased from 4 KB to 6 KB on the MPC5674F.
- Error checking has been added to the parameter RAM on the MPC5674F so an error handler should be added.
- Existing eTPU microcode will execute on the eTPU2 used in the MPC5674F without modification.

5.17 Interrupt Controller

The MPC5566 interrupt controller has 308 interrupt request sources. The MPC5674F interrupt controller has 448 request sources to accommodate interrupt requests from new modules and features.
The pre-existing channel assignments for the MPC5566 are preserved in the MPC5674F for software compatibility.

5.18 eQADC

- The MPC5566 has one eQADC with two ADCs. An additional eQADC has been added to the MPC5674F providing a total of four on-chip ADCs.
- The total number of channels has been increased, from 40 to 64.
- Some channel assignments have changed to accommodate the extra eQADC module. Software management of the command and result queues may require modification.
- New channels have been added to access many internal voltages, including bandgap reference, 3.3 V rails, 1.2 V core voltage, LVIs.
- External muxes have been moved to digital pins allowing increased accuracy on muxed channels.

5.19 Temperature Sensor

A new temperature sensor feature has been added to the MPC5674F. The temperature sensor is read via a new channel in the eQADC.

5.20 Decimation Filter

Four decimation filters have been added to the MPC5674F. Additional interrupt request sources and DMA channels have been added to support the decimation filters — however, the filter is disabled at reset and no software changes are required.

5.21 FMPLL

The MPC5674F employs an enhanced FMPLL module that is not completely register-compatible with the FMPLL module used on the MPC5566. While the configuration operation is similar, the configuration control has now been placed in two registers instead of one. Software must be modified to address the new addresses of the configuration registers. Additionally, due to the change in recommended crystal frequency and bit definitions of the dividers in the configuration registers, the desired system frequency must be recalculated using a new algorithm, which has been provided.

5.22 VRC

The MPC5674F employs a VRC circuit similar to the VRC control used on the MPC5566. Some minor component changes may be required for the VRC decoupling scheme. The MPC5674F also provides a switch mode power supply (SMPS) that may provide a lower-current power supply/regulation solution. If the SMPS is to be used, an additional FET pass transistor, an inductor, and several resistors and capacitors are required. The layout may be designed so that either the normal VRC or the SMPS may be used depending on how the PCB is populated.

5.23 Power Supplies

Both the MPC5566 and the MPC5674 require +5 V and +3.3 V supplies — however, the MPC5566 requires a +1.5 V supply for internal logic, and the MPC5674F requires +1.2 V. An internal regulation controller is provided on the MPC5674F to create the 3.3 V and 1.2 V supplies.

The MPC5674F does not require power sequencing at reset, and any supply may be removed and restored without affecting other supplies. However, pin states may be different during power-up depending on the supply power-up sequence.

5.24 Low-Power Modes

Two new low-power modes are added for the MPC5674F; slow mode and stop mode. Both of these modes are disabled at reset. No software modification is required.

6 Package and Ball Map

The MPC5674F shares several packages with the MPC5566 — however, the ball maps are not pin-compatible. The PCB must be re-routed to support any MPC5674F package.

The MPC5674F rev. 1 device and the MPC5674F rev. 2 device have a minor difference in the ball map to support a new REFBYPC feature. The PCB layout should be implemented in a manner that allows support of both versions on the same PCB with a minor component population change. See Freescale document EB716, “MPC5674F Revision 1 to Revision 2 ADC (REFBYPC) PCB Modification Requirements,” for the details of this PCB design requirement.

The data sheets for each device should be used to compare the thermal data for any differences that would impact hardware design.

Power supply bypassing design/strategy may need to be modified for the MPC5674F.

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