Freescale Semiconductor
Application Note

Document Number: AN4036
Rev. 1, 03/2010

Migration within the MPC560xB/C/D Family

MPC5602D / MPC5601D to MPC5604B/C / MPC5603B/C / MPC5602B/C

by: Alistair Robertson, Freescale Semiconductor Ltd

The 32-bit MPC560xB/C/D automotive microcontrollers are a family of System-on-Chip (SoC) devices designed to be central to the development of the next generation of central vehicle body controller, smart junction box, front module, peripheral body, door control, and seat control applications.

The MPC560xB/C/D family is a series of automotive microcontrollers based on the Power Architecture™ Book E and designed specifically for embedded automotive applications.

The MPC560xB/C/D family is a highly scalable and compatible family of devices. However, designing an application that can be easily ported across different members requires knowledge of the features of the devices and any significant differences between them.

This document focuses specifically on migrating applications between two sets of products among the family:

- MPC5602D: For sales type MPC5602D and MPC5601D

Contents

- MPC5604B: For sales type MPC5604B/C, MPC5603B/C and MPC5062B/C

The set naming refers to the most common sales type in each set.

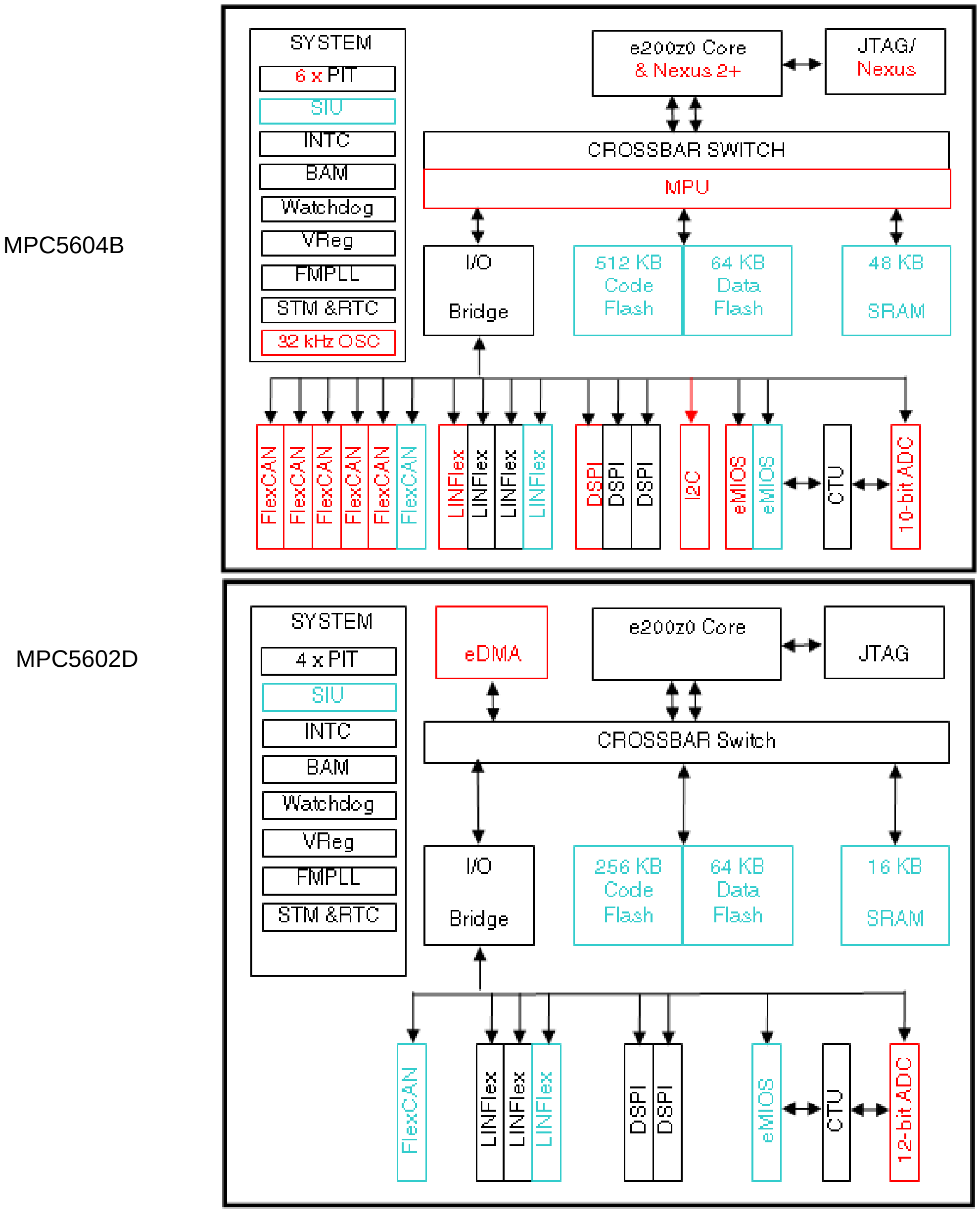
The following use cases will be addressed:

- Migrating from the MPC5602D to the MPC5604B
- Migrating from the MPC5604B to the MPC5602D

1 MPC5602D and MPC5604B comparison overview

Features of the MPC5602D are, in general, a subset of the features available on the MPC5604B. However, in some cases additional features have been added or enhancements have been made; therefore, it is imperative to understand the differences between the devices when designing an application that may be ported between the MPC5604B and the MPC5602D.

Figure 1 highlights the key differences between these devices.



Key:	
Common to both devices	⬛
Only available on highlighted device.	🟥
Differences Between Modules	🟦

Figure 1. MPC5604B/C and MPC5602D comparison overview

2 List of differences between the MPC5604B and the MPC5602D

2.1 Introduction

For an overview of general differences between members of the MPC560xB/C/D family of devices, please refer to the document “MPC560xB/C/D Family - Product Differences”.

The sections hereafter describe in more detail the specific differences between the MPC5604B and the MPC5602D that the user must be aware of when porting applications between these devices.

2.2 ADC

The MPC5604B implementation of ADC follows:

- One 10-bit ADC with:
  - — 16 high precision “ADC0_P” channels
  - — 16 normal “ADC0_S” channels
  - — 4 normal “ADC0_X”channels that can be entries for external multiplexing for up to 32 external channels
  - — PIT2 injection trigger
  - — 4 analog thresholds

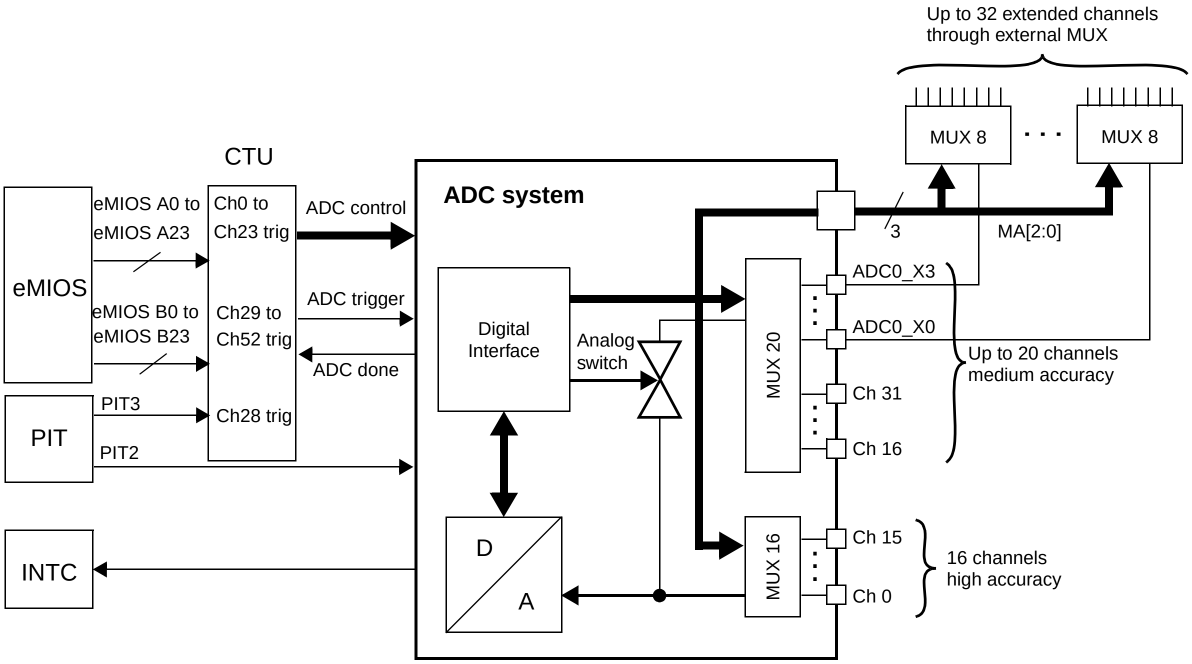


Figure 2. ADC implementation of the MPC5604B

The MPC5602D implementation of ADC follows:

- One 12-bit ADC with:

- 16 high precision “ADC1_P” channels
- 13 normal “ADC1_S” channels
- 4 normal “ADC1_X” channels can be entries for external multiplexing for up to 32 external channels
- PIT2 injection trigger
- 3 analog thresholds

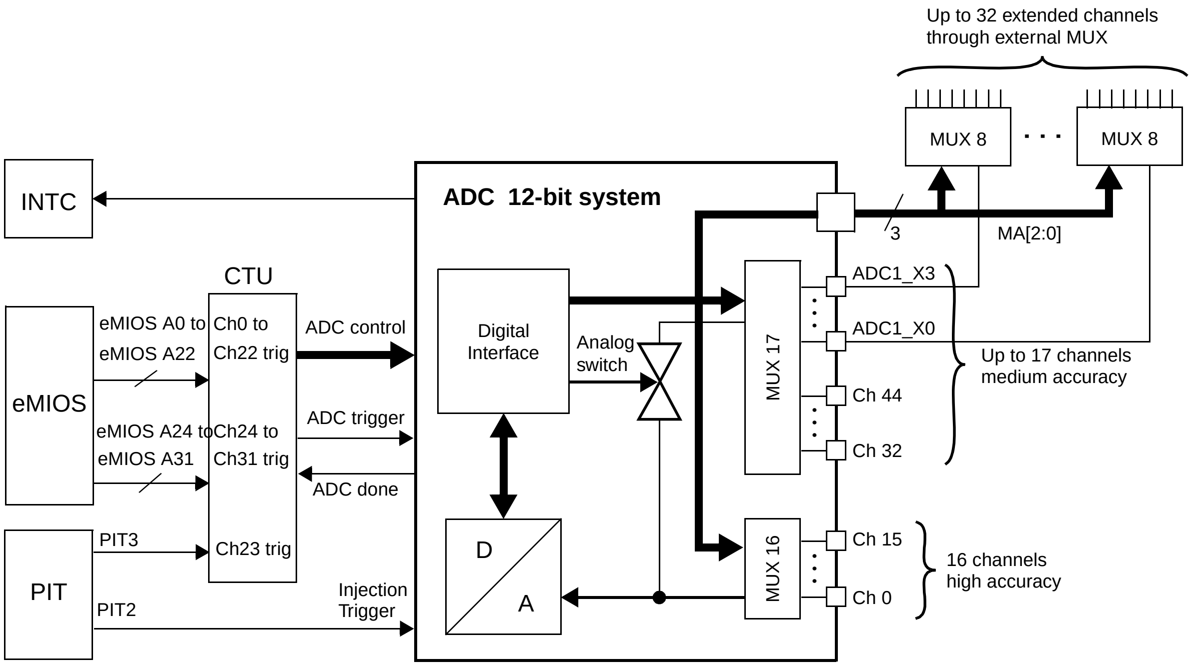


Figure 3. ADC implementation of the MPC5602D

The results of a conversion are stored to the appropriate results register. Software should account for the effective 2-bit offset of the MSB of the result between 10-bit ADC results and 12-bit ADC results.

In addition, the analog threshold mechanism is different between the MPC5602D and the MPC5604B:

- MPC5604B uses four possible analog threshold ranges. Each single range can be allocated to one single channel.
- MPC5602D uses three possible analog threshold ranges. Each single range can be shared between several ADC channels.

The respective sets of registers to handle analog thresholds are different. This should be taken into accoutn when designing applications that are to be ported between the MPC5602D and the MPC5604B.

2.3 eMIOS

The eMIOS modules can have following channel types:

Table 1. eMIOS channel types

Description	Name	Channel type				
		Type X	Type Y	Type F	Type G	Type H
General purpose input / output	GPIO	x	x	x	x	x
Single action input capture	SAIC	x	x	x	x	x
Single action output compare	SAOC	x	x	x	x	x
Modulus counter	MC	x	—	—	—	—
Modulus counter buffered (up / down)	MCB	x	—	—	x	—
Input pulse width measurement	IPWM	—	—	—	x	x
Input period measurement	IPM	—	—	—	x	x
Double action output compare	DAOC	—	—	—	x	x
Output pulse width and frequency modulation buffered	OPWFMB	x	—	—	x	—
Center aligned output PWM buffered with dead time	OPWMCB	—	—	—	x	—
Output pulse width modulation buffered	OPWMB	x	x	—	x	x
Output pulse width modulation trigger	OPWMT	x	x	—	x	x

The MPC5604B contains two eMIOS modules (0 and 1) organized as shown in Figure 4.

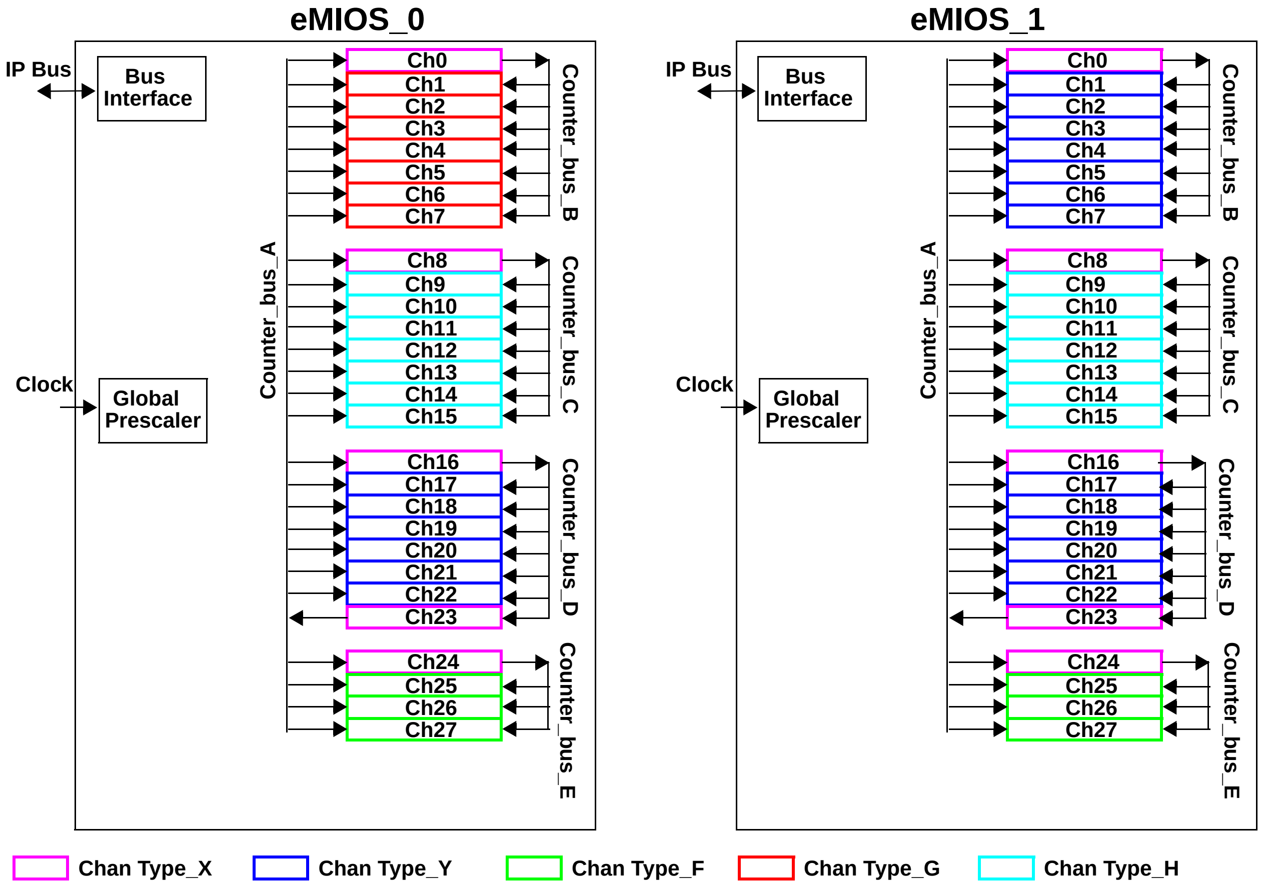


Figure 4. eMIOS implementation of the MPC5604B

The MPC5602D contains one eMIOS module (0) organized as in Figure 5.

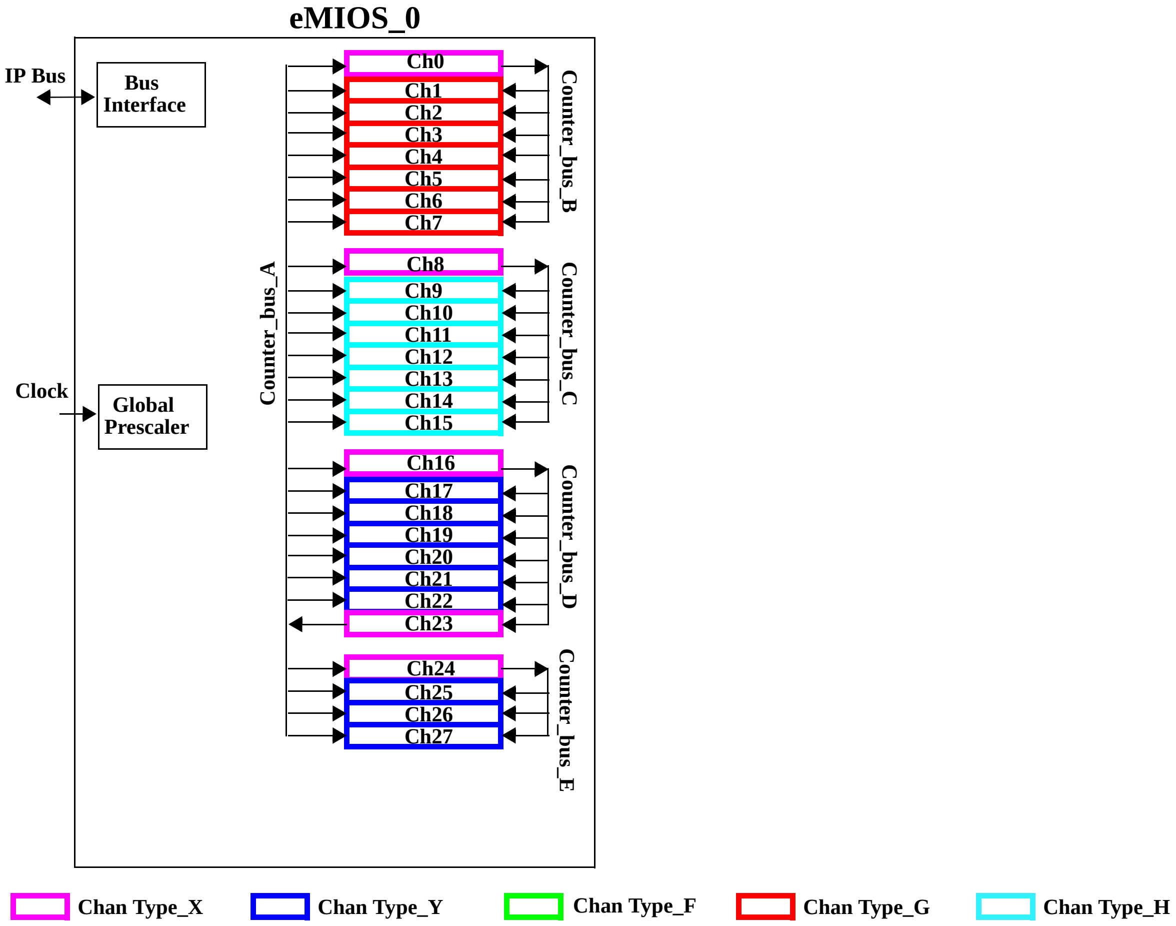


Figure 5. eMIOS implementation of the MPC5602D

2.4 LINFlex

The MPC5604B contains four LINFlex modules. None of them are capable of issuing DMA requests.

TheMPC5602D contains three LINFlex modules. LINFlex 0 is capable of issuing DMA requests:

- LINFlex 0 can issue DMA requests
- LINFlex 1 and 2 are not DMA enabled

2.5 Flash memory

2.5.1 ECC algorithms

Different ECC algorithms are implemented on the MPC5604B and the MPC5602D. These provide the same error detection and error correction features (single-bit error correction and double-bit error detection).

ECC algorithms are implemented in such a way as to get the same ECC syndrome for several data sets. If used correctly, this can allow certain data to be overwritten without having to erase an entire flash sector.

For instance, both sets of flash have the following “rule” activated:

```
Considering a doubleword (64 bits) composed of 4 halfwords with 16 bits each, every one of the
4 halfwords can be written at 0xffff, 0x55aa and 0x0000 in any order. For instance, on both
product sets, the following data will get exactly the same ECC syndrome:

0xffffffff_ffffffff
0x55aaffff_55aaffff
0xffff55aa_ffff55aa
0x55aa55aa_55aa55aa
0x55aa0000_55aa0000
0x000055aa_000055aa
0x00000000_00000000
```

This feature enables censorship without having to erase the shadow sector.

The two ECC algorithms do not use the same “rule” to handle EEPROM emulation; refer to Section 2.5.1.1, “MPC5604B rule” and Section 2.5.1.2, “MPC5602D rule.”

2.5.1.1 MPC5604B rule

```
Considering a doubleword (64 bits) composed by 4 halfwords of 16 bits each, the 4 halfwords can
be written bit by bit in any order (so up to 16 times) with the only constraint being that the
4 halfwords must always be written at the same value. Therefore, all the following doublewords
have the same ECC and can be overwritten:

0xffffffff_ffffffff
0xfffefffe_fffefffe
0xfffcfffc_fffcfffc
0xfff8fff8_fff8fff8
0xfff0fff0_fff0fff0
0xffe0ffe0_ffe0ffe0
0xffc0ffc0_ffc0ffc0
0xff80ff80_ff80ff80
0xff00ff00_ff00ff00
0xfe00fe00_fe00fe00
0xfc00fc00_fc00fc00
0xf800f800_f800f800
0xf000f000_f000f000
0xe000e000_e000e000
0xc000c000_c000c000
0x80008000_80008000
0x00000000_00000000
```

2.5.1.2 MPC5602D rule

```
Considering a doubleword (64 bits) composed by 8 bytes of 8 bits each, the 8 bytes can be written
at 0x55 or 0xaa in any order (so up to 2 times) and in an independent way (so 8 bytes written
2 times = 16 writes). Therefore, all the following doublewords have the same ECC and can be
overwritten:

0xffffffff_ffffffff
0xffffffff_ffffff55
0xffffffff_ffffff00
```

```
0xffffffff_ffff5500
0xffffffff_ffff0000
0xffffffff_ff550000
0xffffffff_ff000000
0xffffffff_55000000
0xffffffff_00000000
0xffffff55_00000000
0xffffff00_00000000
0xffff5500_00000000
0xffff0000_00000000
0xff550000_00000000
0xff000000_00000000
0x55000000_00000000
0x00000000_00000000
```

EEPROM emulation driver provided by Freescale addresses these differences in the ECC mechanism.

2.5.2 Data flash

The data flash arrays are 64 KB with 16 KB sectors on both MPC5604B and MPC5602D.

However, the data flash was optimized on MPC5602D to reduce silicon size. Table 2 highlights the differences between the data flash arrays.

Table 2. MPC5602D and MPC5604B data flash differences

Feature	MPC5604B	MPC5602D
Reads	128 bits	32 bits
Writes	64 bits	32 bits
ECC	Calculated on 64 bits with syndrome encoded in 8 bits.	Calculated on 32 bits with syndrome encoded in 7 bits.
Register UT0	Bits DSI[0:7] contain the 8-bit ECC syndrome.	Bits DSI[0:6] contain the 7-bit ECC syndrome.
Register UT2	Contains bits 32-64 of doubleword used in ECC check.	Not implemented.
Registers UMISR[n]	UMISR0 to UMISR4 contain ECC bits for a whole array: 2 doubleword + ECC 8 bits + information on double- and single-error detection.	UMISR0 to UMISR2 contain ECC bits for a whole array: 32 bits of data + ECC 7 bits + information on double- and single-error detection. UMISR3 and UMISR4 are not implemented.
Power supply dependencies	The code flash and data flash can be powered independently.	The code flash supplies power and critical signals to the data flash.

NOTE

On the MPC5602D device, as a consequence of the dependency of the data flash on the code flash power supply:

- Putting code flash in sleep or power down modes will power down data flash.
- Data flash cannot independently enter sleep mode.

- The user ensures the code flash is operating in normal mode using the data flash.

2.5.3 Code flash

The code flash must be powered up on MPC5602D if the data flash is to be used.

3 Packages and pinout

- The differences between the analog and digital functionality multiplexed onto the pins of the MPC5604B and the MPC5602D devices are summarized in Table 3. In this table the 100LQFP package has been described since it is the only common package between these devices.

Key

🟩 Function unique to MPC5602D
🟦 Function unique to MPC5604B
Function Common to MPC5604B and MPC5602D

Table 3. 100LQFP MPC5602D to MPC5604B comparison

Pin	Pad	Alternate input funtions			Alternate I/O functions			
					ALT0	ALT1	ALT2	ALT3
1	PB[3]	WKUP[11]	LIN0RX		GPIO[19]		🟦 SCL	
2	PC[9]	WKUP[13]	LIN2RX		GPIO[41]		E0UC[7]	
3	PC[14]	EIRQ[8]			GPIO[46]	E0UC[14]	🟦 SCK_2	
4	PC[15]	🟩 EIRQ[20]			GPIO[47]	E0UC[15]	🟦 CS0_2	
5	PA[2]	WKUP[3]			GPIO[2]	E0UC[2]		🟩 MA[2]
6	PE[0]	WKUP[6]	🟦 CAN5RX		GPIO[64]	E0UC[16]	🟦 CAN_sampRX	
7	PA[1]	WKUP[2]			GPIO[1]	E0UC[1]	NMI[0]	
8	PE[1]				GPIO[65]	E0UC[17]	🟦 CAN5TX	
9	PE[8]				GPIO[72]	🟦 CAN2TX	E0UC[22]	🟦 CAN3TX
10	PE[9]	WKUP[7]	🟦 CAN2RX	🟦 CAN3RX	GPIO[73]	🟦 CAN_Samp2_RX	E0UC[23]	🟦 CAN_samp3_RX
11	PE[10]	EIRQ[10]			GPIO[74]	🟦 LIN3TX	CS3_1	
12	PA[0]	WKUP[19]			GPIO[0]	E0UC[0]	CLKOUT	E0UC[13]
13	PE[11]	WKUP[14]	🟦 LIN3RX		GPIO[75]	🟩 E0UC[24]	CS4_1	
14	Vpp							
15	VDD_HV							
16	VSS_HV							
17	RESET							
18	VSS_LV							

Table 3. 100LQFP MPC5602D to MPC5604B comparison (continued)

Pin	Pad	Alternate input funtions			Alternate I/O functions			
					ALT0	ALT1	ALT2	ALT3
19	VDD_LV							
20	VDD_BV							
21	PC[11]	WKUP[5]	CAN1RX	CAN4RX	GPIO[43]	CAN_Samp1_RX	CAN_Samp4_RX	MA[2]
22	PC[10]				GPIO[42]	CAN1TX	CAN4TX	MA[1]
23	PB[0]				GPIO[16]	CAN0TX		LIN0TX
24	PB[1]	WKUP[4]	CAN0RX	LIN0RX	GPIO[17]	CAN_Samp0_RX		
25	PC[6]				GPIO[38]	LIN1TX		
26	PC[7]	WKUP[12]	LIN1RX		GPIO[39]			
27	PA[15]	WKUP[10]			GPIO[15]	CS0_0	SCK_0	E0UC[1]
28	PA[14]	EIRQ[4]			GPIO[14]	SCK_0	CS0_0	E0UC[0]
29	PA[4]	WKUP[9]			GPIO[4]	E0UC[4]		CS0_1
30	PA[13]				GPIO[13]	SOUT_0		
31	PA[12]	EIRQ[17]	SIN_0		GPIO[12]			CS3_1
32	VDD_LV							
33	VSS_LV							
34	XTAL							
35	VSS_HV							
36	EXTAL							
37	VDD_HV							
*38	PB[9]	WKUP[26]	ADC1_S[5]	ADC0_S[1]	GPIO[25]			
*39	PB[8]	WKUP[25]	ADC1_S[4]	ADC0_S[0]	GPIO[24]			
40	PB[10]	WKUP[8]	ADC1_S[6]	ADC0_S[2]	GPIO[26]			
41	PD[0]	WKUP[27]	ADC1_P[4]	ADC0_P[4]	GPIO[48]			
42	PD[1]	WKUP[28]	ADC1_P[5]	ADC0_P[5]	GPIO[49]			
43	PD[2]		ADC1_P[6]	ADC0_P[6]	GPIO[50]			
44	PD[3]		ADC1_P[7]	ADC0_P[7]	GPIO[51]			
45	PD[4]		ADC1_P[8]	ADC0_P[8]	GPIO[52]			
46	PD[5]		ADC1_P[9]	ADC0_P[9]	GPIO[53]			
47	PD[6]		ADC1_P[10]	ADC0_P[10]	GPIO[54]			
48	PD[7]		ADC1_P[11]	ADC0_P[11]	GPIO[55]			
49	PD[8]		ADC1_P[12]	ADC0_P[12]	GPIO[56]			
50	PB[4]		ADC1_P[0]	ADC0_P[0]	GPIO[20]			

Table 3. 100LQFP MPC5602D to MPC5604B comparison (continued)

Pin	Pad	Alternate input funtions			Alternate I/O functions			
					ALT0	ALT1	ALT2	ALT3
51	VSS_HV_ADR0							
52	VDD_HV_ADC0							
53	PB[5]		ADC1_P[1]	ADC0_P[1]	GPIO[21]			
54	PB[6]		ADC1_P[2]	ADC0_P[2]	GPIO[22]			
55	PB[7]		ADC1_P[3]	ADC0_P[3]	GPIO[23]			
56	PD[9]		ADC1_P[13]	ADC0_P[13]	GPIO[57]			
57	PD[10]		ADC1_P[14]	ADC0_P[14]	GPIO[58]			
58	PD[11]		ADC1_P[15]	ADC0_P[15]	GPIO[59]			
59	PB[11]		ADC1_S[12]	ADC0_S[3]	GPIO[27]	E0UC[3]		CS0_0
60	PD[12]		ADC1_S[8]	ADC0_S[4]	GPIO[60]	CS5_0	E0UC[24]	
61	PB[12]		ADC1_X[0]	ADC0_X[0]	GPIO[28]	E0UC[4]		CS1_0
62	PD[13]		ADC1_S[9]	ADC0_S[5]	GPIO[61]	CS0_1	E0UC[25]	
63	PB[13]		ADC1_X[1]	ADC0_X[1]	GPIO[29]	E0UC[5]		CS2_0
64	PD[14]		ADC1_S[10]	ADC0_S[6]	GPIO[62]	CS1_1	E0UC[26]	
65	PB[14]		ADC1_X[2]	ADC0_X[2]	GPIO[30]	E0UC[6]		CS3_0
66	PD[15]		ADC1_S[11]	ADC0_S[7]	GPIO[63]	CS2_1	E0UC[27]	
67	PB[15]		ADC1_X[3]	ADC0_X[3]	GPIO[31]	E0UC[7]		CS4_0
68	PA[3]	EIRQ[0]	ADC1_S0		GPIO[3]	E0UC[3]		CS4_1
69	VSS_HV							
70	VDD_HV							
71	PA[7]	EIRQ[2]	ADC1_S[1]		GPIO[7]	E0UC[7]	LIN3TX	
72	PA[8]	EIRQ[3]	ABS[0]	LIN3RX	GPIO[8]	E0UC[8]	E0UC[14]	
73	PA[9]		FAB		GPIO[9]	E0UC[9]		CS2_1
74	PA[10]		ADC1_S[2]		GPIO[10]	E0UC[10]	SDA	LIN2TX
75	PA[11]	EIRQ[16]	ADC1_S[3]	LIN2RX	GPIO[11]	E0UC[11]	SCL	
76	PE[12]	EIRQ[11]	ADC1_S[7]	SIN_2	GPIO[76]		E1UC[19]	
77	PC[3]	EIRQ[6]	CAN4RX	CAN1RX	GPIO[35]	CS0_1	ADC_MA[0]	
78	PC[2]	EIRQ[5]			GPIO[34]	SCK_1	CAN4TX	
79	PA[5]				GPIO[5]	E0UC[5]		
80	PA[6]	EIRQ[1]			GPIO[6]	E0UC[6]		CS1_1
81	PH[10]				GPIO[122]		TMS	
82	PC[1]				GPIO[33]		TDO	
83	VSS_HV							

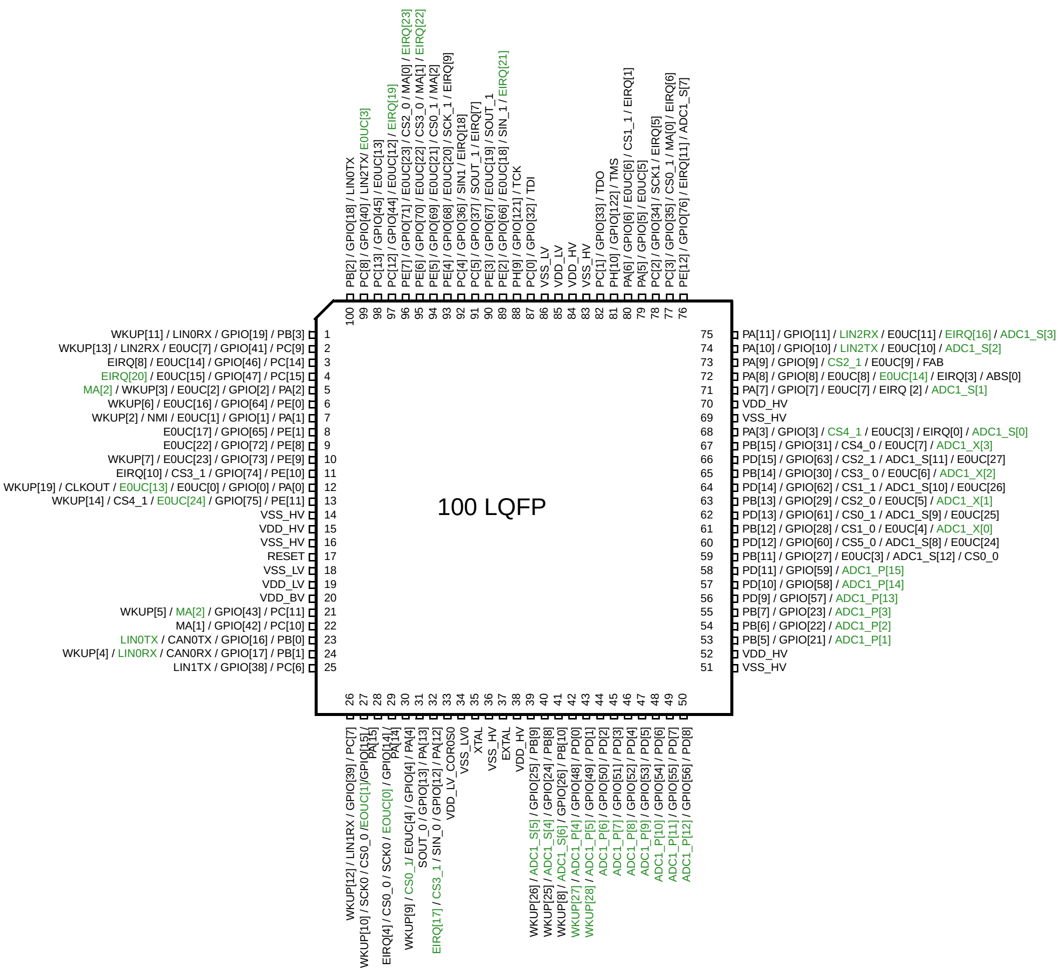
Table 3. 100LQFP MPC5602D to MPC5604B comparison (continued)

Pin	Pad	Alternate input funtions			Alternate I/O functions			
					ALT0	ALT1	ALT2	ALT3
84	VDD_HV							
85	VDD_LV							
86	VSS_LV							
87	PC[0]				GPIO[32]		TDI	
88	PH[9]				GPIO[121]		TCK	
89	PE[2]	EIRQ[21]	SIN_1		GPIO[66]	E0UC[18]		
90	PE[3]				GPIO[67]	E0UC[19]	SOUT_1	
91	PC[5]	EIRQ[7]			GPIO[37]	SOUT_1	CAN3TX	
92	PC[4]	EIRQ[18]	SIN_1	CAN3RX	GPIO[36]			
93	PE[4]	EIRQ[9]			GPIO[68]	E0UC[20]	SCK_1	
94	PE[5]				GPIO[69]	E0UC[21]	CS0_1	MA[2]
95	PE[6]	EIRQ[22]			GPIO[70]	E0UC[22]	CS3_0	MA[1]
96	PE[7]	EIRQ[23]			GPIO[71]	E0UC[23]	CS2_0	MA[0]
97	PC[12]	EIRQ[19]	SIN_2		GPIO[44]	E0UC[12]		
98	PC[13]				GPIO[45]	E0UC[13]	SOUT_2	
99	PC[8]				GPIO[40]	LIN2TX	E0UC[3]	
100	PB[2]				GPIO[18]	LIN0TX	SDA	

NOTE

Pins 38 and 39 may be used as the XTAL and EXTAL inputs of the 32 kHz oscillator on the MPC5604B device only.

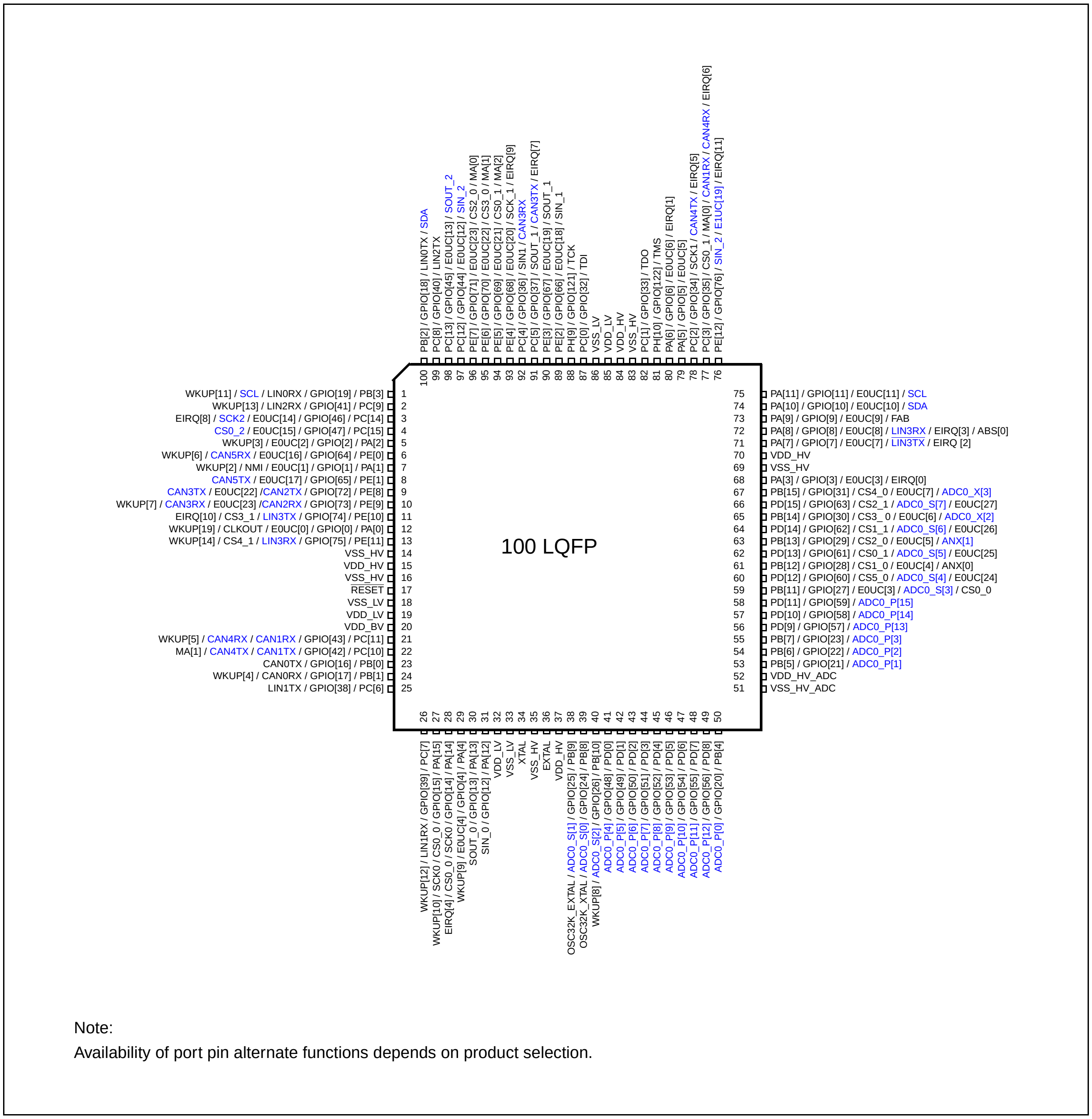
The following package-oriented views illustrate these differences further.


100 LQFP
1 WKUP[11] / LIN0RX / GPIO[19] / PB[3]
2 WKUP[13] / LIN2RX / E0UC[7] / GPIO[41] / PC[9]
3 EIRQ[8] / E0UC[14] / GPIO[46] / PC[14]
4 EIRQ[20] / E0UC[15] / GPIO[47] / PC[15]
5 MA[2] / WKUP[3] / E0UC[2] / GPIO[2] / PA[2]
6 WKUP[6] / E0UC[16] / GPIO[64] / PE[0]
7 WKUP[2] / NMI / E0UC[1] / GPIO[1] / PA[1]
8 E0UC[17] / GPIO[65] / PE[1]
9 E0UC[22] / GPIO[72] / PE[8]
10 WKUP[7] / E0UC[23] / GPIO[73] / PE[9]
11 EIRQ[10] / CS3_1 / GPIO[74] / PE[10]
12 WKUP[19] / CLKOUT / E0UC[13] / E0UC[0] / GPIO[0] / PA[0]
13 WKUP[14] / CS4_1 / E0UC[24] / GPIO[75] / PE[11]
14 VSS_HV
15 VDD_HV
16 VSS_HV
17 RESET
18 VSS_LV
19 VDD_LV
20 VDD_BV
21 WKUP[5] / MA[2] / GPIO[43] / PC[11]
22 MA[1] / GPIO[42] / PC[10]
23 LIN0TX / CAN0TX / GPIO[16] / PB[0]
24 WKUP[4] / LIN0RX / CAN0RX / GPIO[17] / PB[1]
25 LIN1TX / GPIO[38] / PC[6]
26 WKUP[12] / LIN1RX / GPIO[39] / PC[7]
27 WKUP[10] / SCK0 / CS0_0 /EOUC[1]/GPIO[15] / PA[15]
28
29 EIRQ[4] / CS0_0 / SCK0 / EOUC[0] / GPIO[14] / PA[14]
30 WKUP[9] / CS0_1/ E0UC[4] / GPIO[4] / PA[4]
31 SOUT_0 / GPIO[13] / PA[13]
32 EIRQ[17] / CS3_1 / SIN_0 / GPIO[12] / PA[12]
33 VDD_LV_COR0S0
34 VSS_LV0
35 XTAL
36 VSS_HV
37 EXTAL
38 VDD_HV
39 WKUP[26] / ADC1_S[5] / GPIO[25] / PB[9]
40 WKUP[25] / ADC1_S[4] / GPIO[24] / PB[8]
41 WKUP[8] / ADC1_S[6] / GPIO[26] / PB[10]
42 WKUP[27] / ADC1_P[4] / GPIO[48] / PD[0]
43 WKUP[28] / ADC1_P[5] / GPIO[49] / PD[1]
44 ADC1_P[6] / GPIO[50] / PD[2]
45 ADC1_P[7] / GPIO[51] / PD[3]
46 ADC1_P[8] / GPIO[52] / PD[4]
47 ADC1_P[9] / GPIO[53] / PD[5]
48 ADC1_P[10] / GPIO[54] / PD[6]
49 ADC1_P[11] / GPIO[55] / PD[7]
50 ADC1_P[12] / GPIO[56] / PD[8]
51 VSS_HV
52 VDD_HV
53 PB[5] / GPIO[21] / ADC1_P[1]
54 PB[6] / GPIO[22] / ADC1_P[2]
55 PB[7] / GPIO[23] / ADC1_P[3]
56 PD[9] / GPIO[57] / ADC1_P[13]
57 PD[10] / GPIO[58] / ADC1_P[14]
58 PD[11] / GPIO[59] / ADC1_P[15]
59 PB[11] / GPIO[27] / E0UC[3] / ADC1_S[12] / CS0_0
60 PD[12] / GPIO[60] / CS5_0 / ADC1_S[8] / E0UC[24]
61 PB[12] / GPIO[28] / CS1_0 / E0UC[4] / ADC1_X[0]
62 PD[13] / GPIO[61] / CS0_1 / ADC1_S[9] / E0UC[25]
63 PB[13] / GPIO[29] / CS2_0 / E0UC[5] / ADC1_X[1]
64 PD[14] / GPIO[62] / CS1_1 / ADC1_S[10] / E0UC[26]
65 PB[14] / GPIO[30] / CS3_ 0 / E0UC[6] / ADC1_X[2]
66 PD[15] / GPIO[63] / CS2_1 / ADC1_S[11] / E0UC[27]
67 PB[15] / GPIO[31] / CS4_0 / E0UC[7] / ADC1_X[3]
68 PA[3] / GPIO[3] / CS4_1 / E0UC[3] / EIRQ[0] / ADC1_S[0]
69 VSS_HV
70 VDD_HV
71 PA[7] / GPIO[7] / E0UC[7] / EIRQ [2] / ADC1_S[1]
72 PA[8] / GPIO[8] / E0UC[8] / E0UC[14] / EIRQ[3] / ABS[0]
73 PA[9] / GPIO[9] / CS2_1 / E0UC[9] / FAB
74 PA[10] / GPIO[10] / LIN2TX / E0UC[10] / ADC1_S[2]
75 PA[11] / GPIO[11] / LIN2RX / E0UC[11] / EIRQ[16] / ADC1_S[3]
76 PE[12] / GPIO[76] / EIRQ[11] / ADC1_S[7]
77 PC[3] / GPIO[35] / CS0_1 / MA[0] / EIRQ[6]
78 PC[2] / GPIO[34] / SCK1 / EIRQ[5]
79 PA[5] / GPIO[5] / E0UC[5]
80 PA[6] / GPIO[6] / E0UC[6] / CS1_1 / EIRQ[1]
81 PH[10] / GPIO[122] / TMS
82 PC[1] / GPIO[33] / TDO
83 VSS_HV
84 VDD_HV
85 VDD_LV
86 VSS_LV
87 PC[0] / GPIO[32] / TDI
88 PH[9] / GPIO[121] / TCK
89 PE[2] / GPIO[66] / E0UC[18] / SIN_1 / EIRQ[21]
90 PE[3] / GPIO[67] / E0UC[19] / SOUT_1
91 PC[5] / GPIO[37] / SOUT_1 / EIRQ[7]
92 PC[4] / GPIO[36] / SIN1 / EIRQ[18]
93 PE[4] / GPIO[68] / E0UC[20] / SCK_1 / EIRQ[9]
94 PE[5] / GPIO[69] / E0UC[21] / CS0_1 / MA[2]
95 PE[6] / GPIO[70] / E0UC[22] / CS3_0 / MA[1] / EIRQ[22]
96 PE[7] / GPIO[71] / E0UC[23] / CS2_0 / MA[0] / EIRQ[23]
97 PC[12] / GPIO[44] / E0UC[12] / EIRQ[19]
98 PC[13] / GPIO[45] / E0UC[13]
99 PC[8] / GPIO[40] / LIN2TX/ E0UC[3]
100 PB[2] / GPIO[18] / LIN0TX

Note:

Availability of port pin alternate functions depends on product selection.

Figure 6. MPC5602D 100LQFP pin configuration (top view)


100 LQFP
1 WKUP[11] / SCL / LIN0RX / GPIO[19] / PB[3]
2 WKUP[13] / LIN2RX / GPIO[41] / PC[9]
3 EIRQ[8] / SCK2 / E0UC[14] / GPIO[46] / PC[14]
4 CS0_2 / E0UC[15] / GPIO[47] / PC[15]
5 WKUP[3] / E0UC[2] / GPIO[2] / PA[2]
6 WKUP[6] / CAN5RX / E0UC[16] / GPIO[64] / PE[0]
7 WKUP[2] / NMI / E0UC[1] / GPIO[1] / PA[1]
8 CAN5TX / E0UC[17] / GPIO[65] / PE[1]
9 CAN3TX / E0UC[22] /CAN2TX / GPIO[72] / PE[8]
10 WKUP[7] / CAN3RX / E0UC[23] /CAN2RX / GPIO[73] / PE[9]
11 EIRQ[10] / CS3_1 / LIN3TX / GPIO[74] / PE[10]
12 WKUP[19] / CLKOUT / E0UC[0] / GPIO[0] / PA[0]
13 WKUP[14] / CS4_1 / LIN3RX / GPIO[75] / PE[11]
14 VSS_HV
15 VDD_HV
16 VSS_HV
17 RESET
18 VSS_LV
19 VDD_LV
20 VDD_BV
21 WKUP[5] / CAN4RX / CAN1RX / GPIO[43] / PC[11]
22 MA[1] / CAN4TX / CAN1TX / GPIO[42] / PC[10]
23 CAN0TX / GPIO[16] / PB[0]
24 WKUP[4] / CAN0RX / GPIO[17] / PB[1]
25 LIN1TX / GPIO[38] / PC[6]
26 WKUP[12] / LIN1RX / GPIO[39] / PC[7]
27 WKUP[10] / SCK0 / CS0_0 / GPIO[15] / PA[15]
28 EIRQ[4] / CS0_0 / SCK0 / GPIO[14] / PA[14]
29 WKUP[9] / E0UC[4] / GPIO[4] / PA[4]
30 SOUT_0 / GPIO[13] / PA[13]
31 SIN_0 / GPIO[12] / PA[12]
32 VDD_LV
33 VSS_LV
34 XTAL
35 VSS_HV
36 EXTAL
37 VDD_HV
38 OSC32K_EXTAL / ADC0_S[1] / GPIO[25] / PB[9]
39 OSC32K_XTAL / ADC0_S[0] / GPIO[24] / PB[8]
40 WKUP[8] / ADC0_S[2] / GPIO[26] / PB[10]
41 ADC0_P[4] / GPIO[48] / PD[0]
42 ADC0_P[5] / GPIO[49] / PD[1]
43 ADC0_P[6] / GPIO[50] / PD[2]
44 ADC0_P[7] / GPIO[51] / PD[3]
45 ADC0_P[8] / GPIO[52] / PD[4]
46 ADC0_P[9] / GPIO[53] / PD[5]
47 ADC0_P[10] / GPIO[54] / PD[6]
48 ADC0_P[11] / GPIO[55] / PD[7]
49 ADC0_P[12] / GPIO[56] / PD[8]
50 ADC0_P[0] / GPIO[20] / PB[4]
51 VSS_HV_ADC
52 VDD_HV_ADC
53 PB[5] / GPIO[21] / ADC0_P[1]
54 PB[6] / GPIO[22] / ADC0_P[2]
55 PB[7] / GPIO[23] / ADC0_P[3]
56 PD[9] / GPIO[57] / ADC0_P[13]
57 PD[10] / GPIO[58] / ADC0_P[14]
58 PD[11] / GPIO[59] / ADC0_P[15]
59 PB[11] / GPIO[27] / E0UC[3] / ADC0_S[3] / CS0_0
60 PD[12] / GPIO[60] / CS5_0 / ADC0_S[4] / E0UC[24]
61 PB[12] / GPIO[28] / CS1_0 / E0UC[4] / ANX[0]
62 PD[13] / GPIO[61] / CS0_1 / ADC0_S[5] / E0UC[25]
63 PB[13] / GPIO[29] / CS2_0 / E0UC[5] / ANX[1]
64 PD[14] / GPIO[62] / CS1_1 / ADC0_S[6] / E0UC[26]
65 PB[14] / GPIO[30] / CS3_ 0 / E0UC[6] / ADC0_X[2]
66 PD[15] / GPIO[63] / CS2_1 / ADC0_S[7] / E0UC[27]
67 PB[15] / GPIO[31] / CS4_0 / E0UC[7] / ADC0_X[3]
68 PA[3] / GPIO[3] / E0UC[3] / EIRQ[0]
69 VSS_HV
70 VDD_HV
71 PA[7] / GPIO[7] / E0UC[7] / LIN3TX / EIRQ [2]
72 PA[8] / GPIO[8] / E0UC[8] / LIN3RX / EIRQ[3] / ABS[0]
73 PA[9] / GPIO[9] / E0UC[9] / FAB
74 PA[10] / GPIO[10] / E0UC[10] / SDA
75 PA[11] / GPIO[11] / E0UC[11] / SCL
76 PE[12] / GPIO[76] / SIN_2 / E1UC[19] / EIRQ[11]
77 PC[3] / GPIO[35] / CS0_1 / MA[0] / CAN1RX / CAN4RX / EIRQ[6]
78 PC[2] / GPIO[34] / SCK1 / CAN4TX / EIRQ[5]
79 PA[5] / GPIO[5] / E0UC[5]
80 PA[6] / GPIO[6] / E0UC[6] / EIRQ[1]
81 PH[10] / GPIO[122] / TMS
82 PC[1] / GPIO[33] / TDO
83 VSS_HV
84 VDD_HV
85 VDD_LV
86 VSS_LV
87 PC[0] / GPIO[32] / TDI
88 PH[9] / GPIO[121] / TCK
89 PE[2] / GPIO[66] / E0UC[18] / SIN_1
90 PE[3] / GPIO[67] / E0UC[19] / SOUT_1
91 PC[5] / GPIO[37] / SOUT_1 / CAN3TX / EIRQ[7]
92 PC[4] / GPIO[36] / SIN1 / CAN3RX
93 PE[4] / GPIO[68] / E0UC[20] / SCK_1 / EIRQ[9]
94 PE[5] / GPIO[69] / E0UC[21] / CS0_1 / MA[2]
95 PE[6] / GPIO[70] / E0UC[22] / CS3_0 / MA[1]
96 PE[7] / GPIO[71] / E0UC[23] / CS2_0 / MA[0]
97 PC[12] / GPIO[44] / E0UC[12] / SIN_2
98 PC[13] / GPIO[45] / E0UC[13] / SOUT_2
99 PC[8] / GPIO[40] / LIN2TX
100 PB[2] / GPIO[18] / LIN0TX / SDA

Note:

Availability of port pin alternate functions depends on product selection.

Figure 7. MPC5604B 100LQFP pin configuration (top view)

4 Migrating from the MPC5602D to the MPC5604B

The following sections indicate important information the user must know while migrating an application from the MPC5602D to the MPC5604B.

4.1 Pins

The multiplexing on the device pins varies between the MPC5602D and the MPC5604B. Referring to Table 3, the user should be sure not to use any features highlighted in dark green since these features are specific to the MPC5602D and will not be available on the MPC5604B.

4.2 Frequency

The MPC5602D’s maximum frequency is 48 MHz. The MPC5604B’s maximum frequency is 64 MHz. Thus, if a frequency greater than 48 MHz is used on the MPC5604B then all the prescalars (peripheral sets, communication modules, and so forth) must be recalculated appropriately.

4.3 RAM

The MPC5602D has 16 KB of RAM in power domain 0, while the MPC5604B can have either 8 KB or 32 KB of RAM in this domain. This is controlled by the user configuration using the PCU_PCONF2 register.

If using more than 8 KB standby RAM in the application, user should activate 32 KB of RAM using this register, ensuring that at least 16 KB of RAM will be available.

4.4 Flash

On the MPC5604B, the code flash and the data flash are independent. On the MPC5602D, the code flash provides power supply and necessary signals to the data flash. As a consequence, the user should not assume correct data flash operation while changing settings on the code flash. Any code developed with this assumption should be altered to work properly on the MPC5604B.

The MPC5604B and the MPC5602D do not share the same ECC algorithm. Any code manipulating the ECC data/registers directly should be altered appropriately. If an application uses the Freescale EEPROM emulation drivers, then the user should ensure the drivers for the respective target are used.

Data flash timings are slower on the MPC5602D than on the MPC5604B; refer to the electrical specifications in MPC5602D data sheet for more details. Any code making assumptions on these timings should be adjusted accordingly.by providing the data.

4.5 ADC

The MPC5604B does not have 12-bit resolution ADC channels. All results are provided as 10-bit results with 10-bit accuracy. The MPC5602D only has 12-bit resolution ADC channels. All results are provided as 12-bit results although accuracy varies from 12 bits to 10 bits depending on the specific channel type used. (refer to Section 2.2, “ADC”). Therefore, software should be adapted to handle the 2-bit offset in the MSB of the results provided in the relevant results register.

Not all ADC channels present on the MPC5602D are present on the MPC5604B. Specifically pads PA[7, 10, and 11] and PE[12] do not have ADC functionality multiplexed onto them on the MPC5604B. Therefore, if designing an application to be ported from the MPC5602D to the MPC5604B, these pads should not be used as ADC channels.

The analog threshold implementation is also different. An application using them on MPC5604B should be modified as follows to migrate to MPC5602D:

- Do not use the Threshold Control Registers (TRC[0..3]). These are unavailable on MPC5602D.
  - Instead, use the Channel Watchdog Enable Register (CWEN0), with Channel Watchdog Selection Registers (CWSEL[0..1]).
- Rewrite code that uses the Watchdog Threshold Interrupt Mask Register (WTIMR) and Watchdog Threshold Interrupt Status Register (WTISR).
  - MPC5604B low and high threshold bits are “grouped” in the registers.
  - MPC5602D low and high threshold bits are “grouped” two by two. Therefore, these registers usage must be rewritten.
  - In addition, MPC5602D Analog Watchdog Out of Range Register (AWORR0) gives information about channel numbers that were out of analog range.

4.6 LINFlex

The MPC5604B LINFlex 3 cannot be used on the MPC5602D. Further, the LINFlex 0 on the MPC5602D supports DMA requests, while the MPC5604B does not have DMA.

4.7 eMIOS

eMIOS channels 25, 26, 27, and 28 on the MPC5602D contain a superset of the functionality available on the equivalent eMIOS module on the MPC5604B. Specifically these channels are of “Type Y” on the MPC5602D and “Type F” on the MPC5604B. This means that the OPWMB and OPWMT modes should not be used on these channels if the application is to be ported from the MPC5602D to the MPC5604B.

4.8 Device ID

The MCU ID registers MIDR1 and MIDR2 contain information pertaining to the device including part number, package type, maskset information, and parametric data such as flash size and inclusion of data flash.

The device identification register within the JTAG controller is read by debuggers to identify the device under test.

Table 4 shows the register content for each device and package option. When porting code between the MPC5602D and the MPC5604B any software that depends on the contents of these registers should be modified appropriately. Refer to the respective device reference manuals for full bit-level descriptions of these registers.

Table 4. Device ID registers

Device	Package	Flash Size	MIDR1	MIDR2	JTAGC ID
MPC5604C	100 LQFP	512 KB	0x5604_34XX	0x2800_4310	0x0AE4401D
MPC5604B	144 LQFP	512 KB	0x5604_34XX	0x2800_4210	0x0AE4401D
MPC5604B	100 LQFP	512 KB	0x5604_24XX	0x2800_4210	0x0AE4401D
MPC5603C	100 LQFP	384 KB	0x5603_24XX	0x2200_4310	0x0AE4401D
MPC5603B	144 LQFP	384 KB	0x5603_34XX	0x2200_4210	0x0AE4401D
MPC5603B	100 LQFP	384 KB	0x5603_24XX	0x2200_4210	0x0AE4101D
MPC5602C	100 LQFP	256 KB	0x5602_24XX	0x2000_4310	0x0AE4101D
MPC5602B	144 LQFP	256 KB	0x5602_34XX	0x2000_4210	0x0AE4101D
MPC5602B	100 LQFP	256 KB	0x5602_24XX	0x2000_4210	0x0AE4101D
MPC5601D	100 LQFP	128 KB	0x5601_24XX	0x1800_4410	0x0AE4401D
MPC5601D	64 LQFP	128 KB	0x5601_04XX	0x1800_4410	0x0AE4401D
MPC5602D	100 LQFP	256 KB	0x5602_24XX	0x2000_4410	0x0AE4401D
MPC5602D	64 LQFP	256 KB	0x5602_04XX	0x2000_4410	0x0AE4401D

NOTE

0xXX denote mask set and revision number.

5 Migrating from the MPC5604B to the MPC5602D

The following sections indicate important information the user must know while migrating an application from the MPC5604B to the MPC5602D.

5.1 Pins

The MPC5604B will be available in 100, 144, and 176 LQFP, and 208 BGA packages, while the MPC5602D will be available in 64, 80, and 100 LQFP packages. The only common package is the 100 LQFP, for which the pinouts will be similar (refer to the exceptions listed in Section 3, “Packages and pinout”). In any case, porting an application from larger package to smaller package may require some software modifications since there will be fewer features available.

5.2 Frequency

The MPC5602D maximum frequency is 48 MHz. If a higher frequency was used on the MPC5604B, all prescalars (peripheral sets, communication modules, and so forth) must be recalculated based on this maximum achievable speed of 48 MHz.

5.3 32 kHz external oscillator

The MPC5602D does not support the 32 kHz external oscillator. As a consequence, an MPC5604B application using this oscillator to clock API/RTC should be changed to another clock source.

5.4 RAM

The MPC5602D has 16 KB of RAM in power domain 0, while the MPC5604B can have either 8 KB or 32 KB of RAM in this domain, according to the user’s configuration, using the PCU_PCONF2 register.

If migrating from the MPC5604B to the MPC5602D, the user application has to fit into the 16 KB available on the MPC5602D.

5.5 Flash

Code flash and data flash are independent on the MPC5604B. Code flash provides the power supply and the clock to the data flash on the MPC5602D. As a consequence, the user cannot put the data flash in power down mode on the MPC5602D. Special attention should be given to code putting the code flash in power down mode, as it will put data flash in power down mode on the MPC5602D. Software needs to take this situation into account.

The MPC5604B and MPC5602D do not share the same ECC algorithm. Any code directly manipulating ECC data/registers should be rewritten. If an application uses Freescale’s EEPROM emulation driver, the user should adapt the driver for the respective MPC560xB/C/D target.

Data flash timings are slower on the MPC5602D than the MPC5604B. Any code making assumptions on these timings should be rewritten.

5.6 MPU

The MPC5604B has an MPU. The MPC5602D does not. Do not use this feature if the application is to be compatible between the MPC5602D and the MPC5604B.

5.7 Nexus 2+

The MPC5604B supports Nexus 2+ (including instruction trace capability) in certain packages, while the MPC5602D supports only Nexus class 1 (including basic run control) over the standard JTAG port.

5.8 PIT

The MPC5604B has six periodic interrupt timers; the MPC5602D has four. The respective implementations are shown in Table 5 and Table 6.

Table 5. MPC5604B PIT details

PIT number	Interrupt	Peripheral Trigger
0	YES	NO
1	YES	NO
2	YES	10-bit ADC
3	YES	CTU ch28
4	YES	NO
5	YES	NO

Table 6. MPC5602D PIT details

PIT number	Interrupt	Peripheral Trigger	DMA trigger
0	YES	NO	YES
1	YES	NO	YES
2	YES	12-bit ADC	NO
3	YES	CTU ch23	NO

5.9 eMIOS

The MPC5604B has two eMIOS modules, eMIOS_0 and eMIOS_1. The MPC5602D has only eMIOS_0 implemented.

5.10 ADC

The MPC5604B has a 10-bit resolution ADC (ADC0 10 bit). The MPC5602D has one ADC 12 bit. Any application making use of ADC0 on the MPC5604B will have to be modified to use ADC1 of the MPC5602D.

In addition, an application making use of analog threshold feature will have to be re-coded with scheme and quantities of thresholds available on MPC5604B. Refer to Section 4.5, “ADC.”

5.11 CTU

All CTU channels above 28 on the MPC5604B do not exist on the MPC5602D.

5.12 LINFlex

The MPC5604B LINFlex 3 can not be used on the MPC5602D. Do not use this feature if the application is to be compatible between the MPC5602D and the MPC5604B.

5.13 I^2C

The MPC5604B has one I^2C. The MPC5602D has none. Do not use this feature if the application is to be compatible between the MPC5602D and the MPC5604B.

5.14 FlexCAN and CANSampler

The MPC5604B FlexCAN 1 to 5 cannot be used on the MPC5602D. In addition, message filters are not present on the MPC5602D FlexCAN. Further, the FlexCAN implemented on the MPC5602D contains only 32 message buffers compared with the 64 message buffers implemented on the FlexCAN modules on the MPC5604B.

The MPC5604B CANSampler is not present on the MPC5602D. Do not use this feature if the application is to be compatible between the MPC5602D and the MPC5604B.

5.15 DSPI

MPC5604B DSPI 2 cannot be used on the MPC5602D. Do not use this feature if the application is to be compatible between the MPC5602D and the MPC5604B.

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