Freescale Semiconductor
Application Note

Hardware Basic Recommendations for Prototyping with the i.MX31

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This application note describes the basic recommendations that should be implemented when an application using the i.MX31 processor is at the prototyping stage. This document explains the minimal system required to boot the device and attach more devices to it.

Contents

1   i.MX31 Minimal System

The i.MX31 minimal system includes the following:

- Power Management (PMIC or any other power circuitry)
- Non-Volatile Memory (NOR or NAND)
- Volatile Memory (SDR, SRAM, PSRAM or LPDDR)
- Debug Interface (JTAG and UART)
- BOOT Modes Access

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Figure 1 shows the i.MX31 minimal system that includes the PMIC, FLASH, RAM, UART and JTAG interfaces.
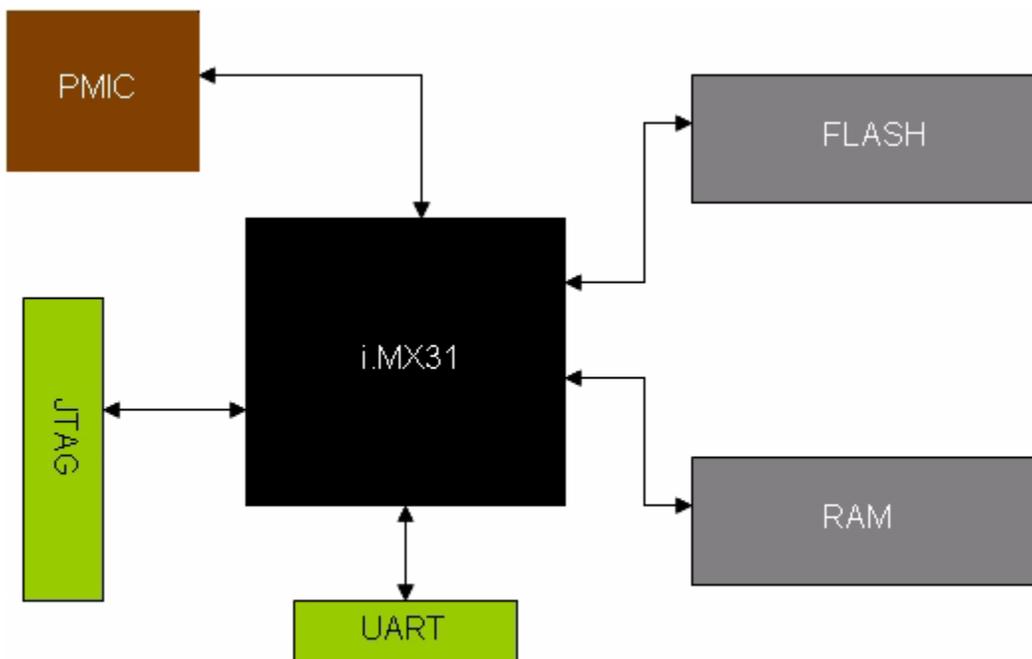

Figure 1. i.MX31 Minimal System

2 Power Management Integrated Circuit

The Power Management Integrated Circuit (PMIC) is one of the most important parts used in the minimal system. It provides and manages the power supplies when the processor is operated under any of the power modes. The i.MX31 processor uses Serial Peripheral Interface (SPI) communication to interact and intimates the PMIC about the power mode being used. The PMIC responds by changing the power supplies characteristics. Other devices such as LDOs or Buck-Boost switching regulators can be used to manage the power for the i.MX31 processor, but it would be more difficult for the processor to have control over these devices as the i.MX31 processor does not have an easy and fast way to communicate its power needs.

To have good connectivity from the power supply to the i.MX31 processor, ensure that all the internal power domains are connected to a proper voltage as described in the *i.MX31 Multimedia Applications Processor Data Sheet* (MCIMX31). Ensure that the voltage levels are correct for all power domains. It is recommended to add test points and/or 0 Ω resistors or jumpers across all the power sources.

If devices other than PMIC are used, ensure that they meet the power up ramps, voltage and current levels. The best way to do this is to cascade the LDOs and turn them ON sequentially according to the datasheet. The board design must guarantee that supplies reach 90% of the level before transition to the next state using PMIC or other power circuitry.

To boot the system, turn ON the following signals or pads in the order shown below:

1. Hold Power On Reset (POR) signal asserted.
2. QVCC, QVCC1 and QVCC4 (Group 1)
3. IOQVDD, NVCC1, NVCCx (1.8 V), NVCCx (2.8 V) (Group 2)
4. FVCC, MVCC, SVCC, UVCC (Group 3)
5. BOOT [4:0] must be set before RESET.
6. Release POR signal to the i.MX31 processor.

Figure 2 shows power-up ramps for the i.MX31 processor using MC13783 (Atlas) chip (recommended by Freescale).
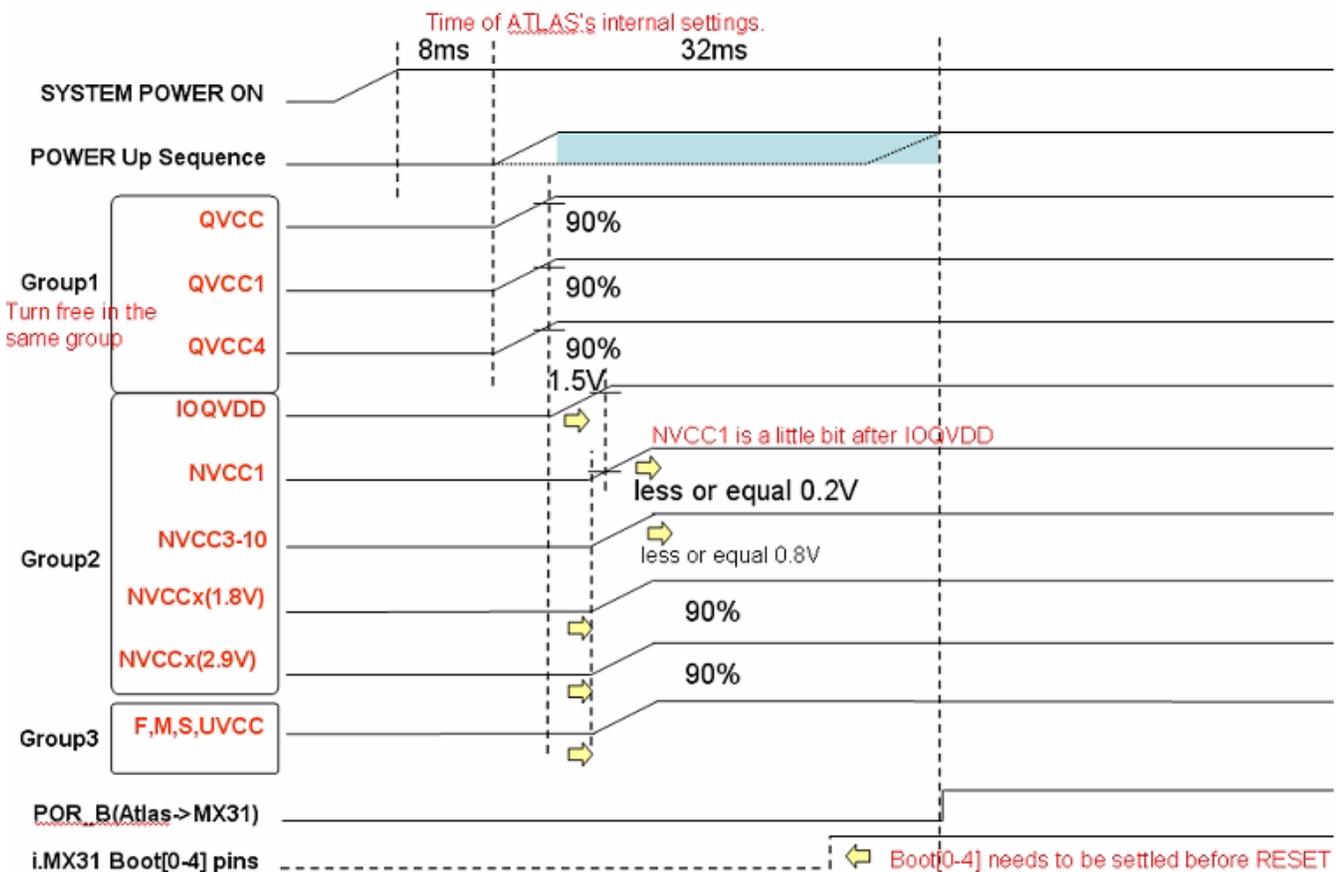
Figure 2. i.MX31 Recommended Power Up Sequence

2.1   General Recommendations

Follow the recommendations given below:

- FUSE_VDD—Add two test points or two 0 Ω resistors from this pin, one across 1.8 V power rail and another across 3.3 V power rail, to have the option of populating or de-populating them.
- IOQVDD—Ensure that it is connected at 1.8 V. Do not connect at 2.8 V or above.

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- FVCC, MVCC, UVCC and SVCC—This voltage is not dependent on core (TO2.0 and newer). It can be connected at 1.5 V.
- QVCC, QVCC1 and QVCC4—Connect them across the same voltage. It is recommended to keep them gated independently to enter into any of the low power modes. Add test points across these voltage rails.
- NVCC6, NVCC9—Ensure that they are connected together.
- NVCC2, NVCC21-22—Connect them together. This is the voltage rail for Double Data Rate (DDR) memory.

If DDR and peripheral voltages are grouped, it affects other peripherals because of the noise generated by the DDR. Add a ferrite bead to minimize the noise inducted by DDR switching.

It is recommended to add a current monitor chip to track the current or power consumption of the system (for example, MAX4071). If this chip receives power from the source used by the main system and the processor enters into any of the low power modes, the power supply is turned OFF and the power sensing chips do not work properly. So the measurement turns unreliable. Therefore, place the current monitoring circuitry in a separate board to measure externally.

3 Volatile and Non-Volatile Memories

The basic application with the i.MX31 processor includes two kinds of memories, one for storage and another for temporary transactions.

Non-volatile memory, such as flash, stores data (for example, operating system) required to turn ON the system. Volatile memory such as RAM is used as temporary data storage. Ensure that i.MX31's communication with the memory is functional. The i.MX31 minimal system needs at least two kinds of memories to operate, for example, NOR or NAND and RAM which can be either Single Data Rate (SDR) or Low Power Double Data Rate (LPDDR) SRAM/PSRAM. These memories can be connected and used in one single board or by using a motherboard with several daughter boards.

The NAND memory must be connected to NAND Flash Controller (NANDFC), NOR to Wireless External Interface Module (WEIM) and SDRAM to Enhanced SDRAM Controller (ESDCTL). The address bus is shared internally between WEIM and ESDCTL and the data bus is shared between NANDFC and WEIM. A single data bus is assigned for ESDCTL.

If specific NAND, NOR or RAM memories are chosen to test the prototype board, assemble them on the processor board itself. This increases the signal integrity and also avoids building more prototypes.

Figure 3 shows the memory interconnections.
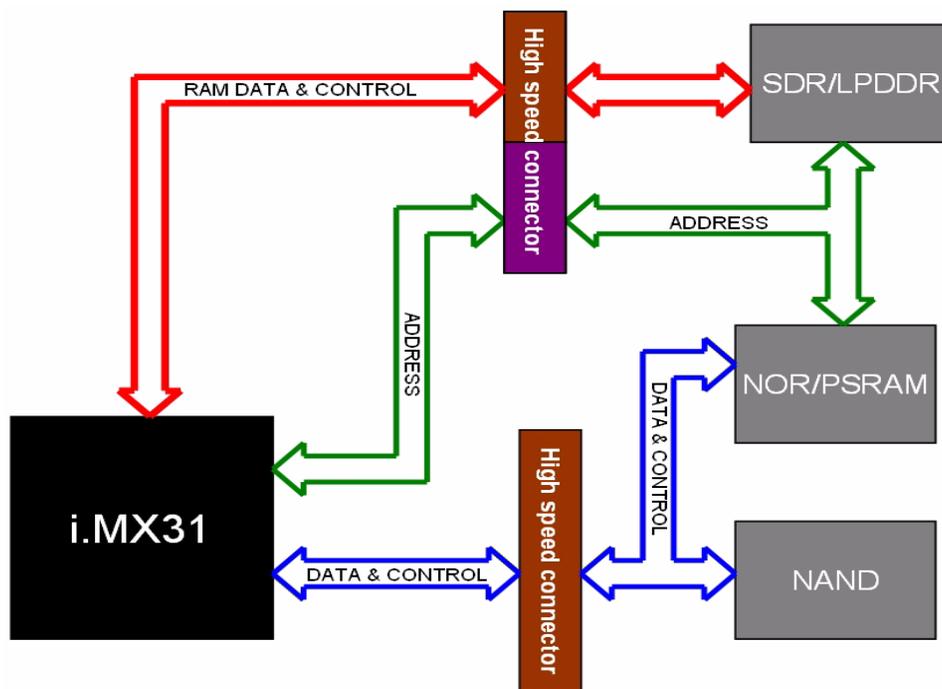
Figure 3. Memory Interconnections

The first connector is a single high speed connector and it is divided into two sections: Address and Data. Using this connector, RAM data and address lines are shared. It has address lines shared by RAM and NOR/PSRAM devices. The second connector has control lines for NAND device and data for both NAND and NOR/PSRAM devices. Plug-in the first connector to measure RAM data or address. Plug-in the second connector to measure NAND data and control. Use both the connectors to measure NOR/PSRAM data or address.

It is recommended to keep the memories close to the i.MX31 processor so that the space between the processor, connectors and memories is constrained. In case the memory devices are to be replaced with new ones at a later stage, distance them from the connector to avoid the heat that may damage the connector and the memory devices. The shared lines must be daisy chained to avoid extra stubs.

It is recommended to use Platform Independent Storage Module (PISMO) standard boards to test or validate different memory devices because the separate approach would be difficult. Many manufacturers distribute their memories in PISMO boards.

3.1   Analysis of PISMO Card

PISMO standard is an effort by the memory manufacturers and some microprocessor companies to create a unique interface for debugging and interfacing the memory modules. It is not a protocol implementation or a generic standardization of memories. PISMO is more like a hardware predefined module to interface any kind of memory with a system having a PISMO interface.

For the High Speed connectors from SAMTEC:

- Male Connector Part Number: SEAM-40-02.0-SM-8-2-A-K
- Female Connector Part Number: SEAF-40-05.0-SM-8-2-A-K

Figure 4 shows PISMO Cards arrangement.
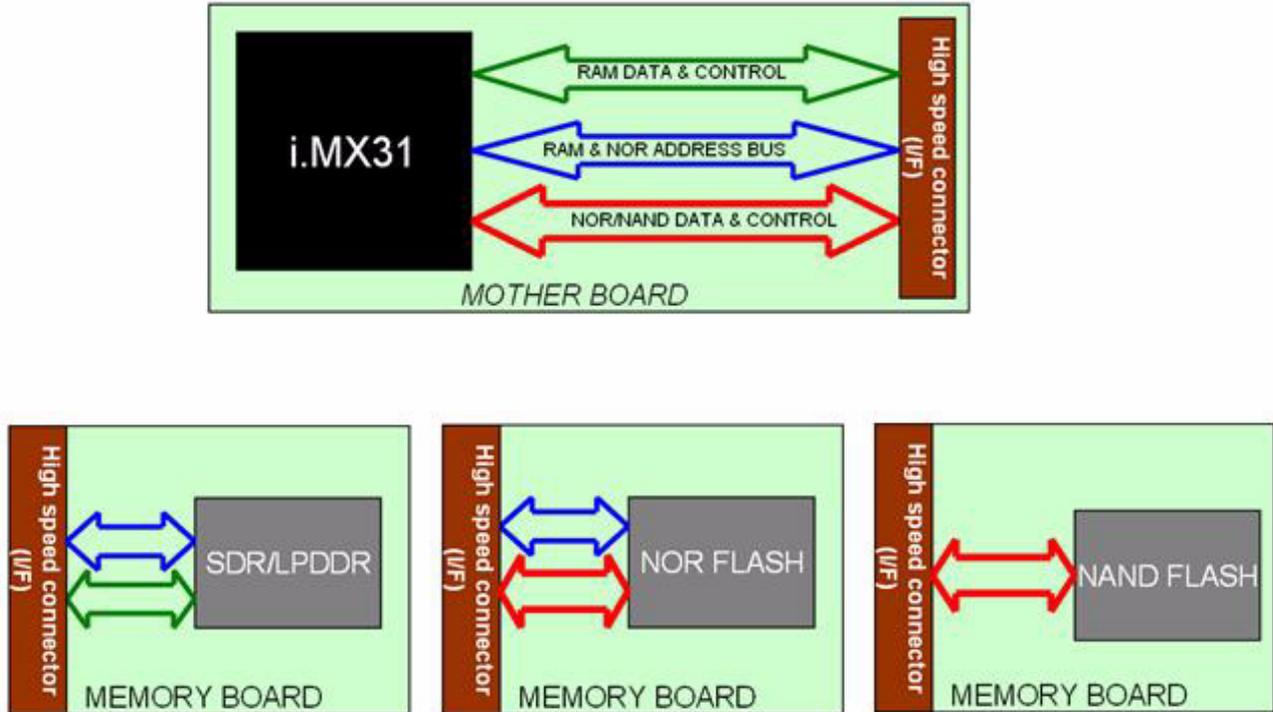
Figure 4. PISMO Cards

PISMO boards can be stacked as shown in Figure 5.
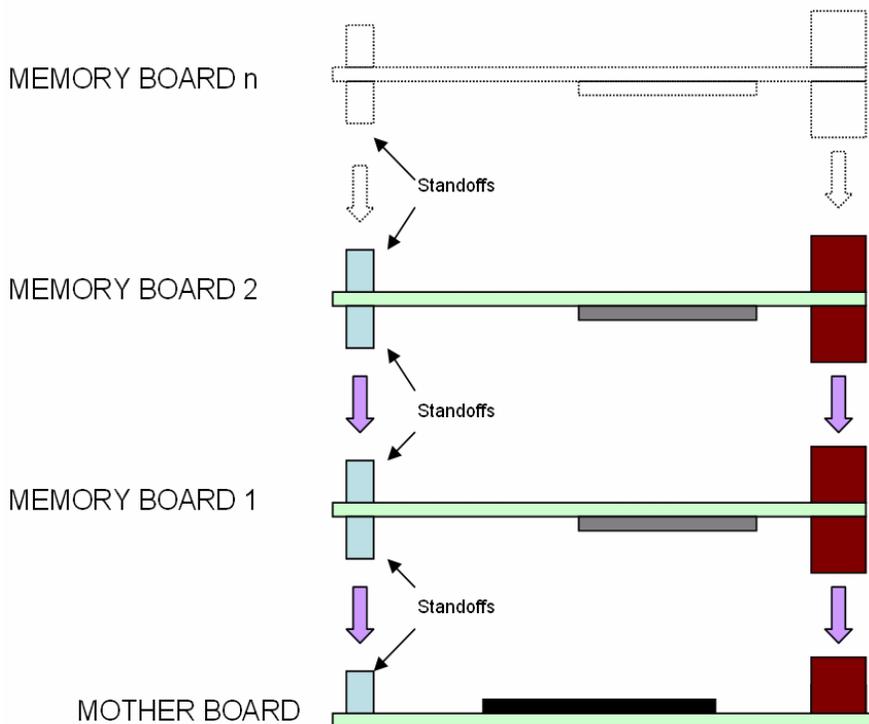
Figure 5. Stacked PISMO Cards

Tune all the traces as short as possible to avoid losses. This also increases the signal quality.

At times, memory devices work at different voltage rates, as the data and the address buses are shared between them and therefore there may be a need to add a level translator from 1.8 V to 2.8–3.3 V and vice versa.

Figure 6 shows how to analyze the data buses in PISMO cards with another card which has the matching connector as that of PISMO.
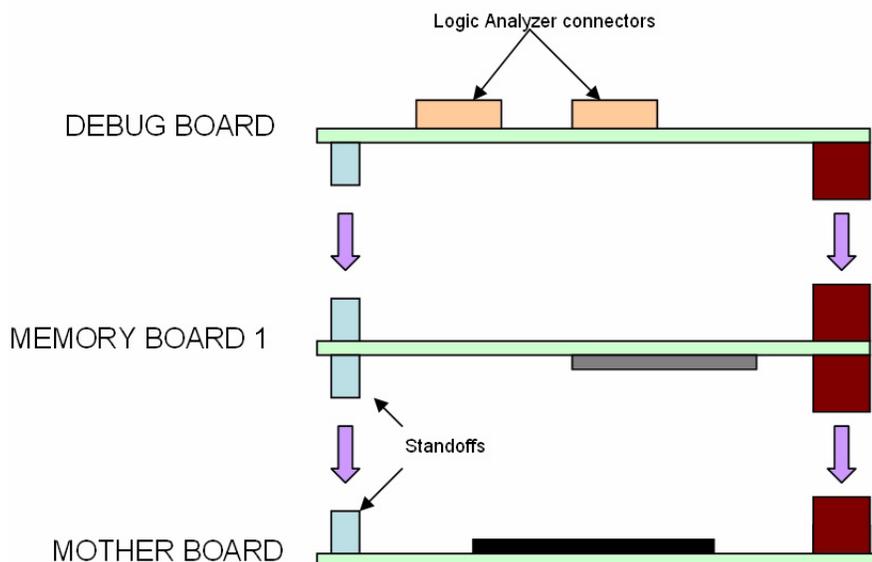
Figure 6. PISMO Cards with Logic Analyzer Option

This approach affects the signal integrity as the measurements are not taken from the data received by DDR/NAND/NOR memories. The data is first received by the memory device and then by the logic analyzer. Due to this, reflections occur and the signal turns noisy. To minimize the noise effect, keep the logic analyzer connector close to the SAMTEC connector that connects the memory board.

4   Debug Interface

JTAG is the most common interface used for debugging ARM based microprocessors. JTAG is compliant with the IEEE1149.1 testability standard. Universal asynchronous receiver/transmitter (UART) is one of the easiest ways to debug hardware or software. It involves sending output messages to a terminal (whether JTAG is used or not). Any UART on the i.MX31 processor can be used for debugging. UART1 is the only port used for programming or erasing NOR and NAND memories in bootstrap mode (for example, by using Advanced Toolkit software). Hence, it is used in this document.

These interfaces are the only way to get into the chip and help to diagnose where the processor or memories may not work properly. Pull-up and pull-down resistors are part of the JTAG standard as shown in Figure 7.

Figure 7 shows JTAG recommended connections.
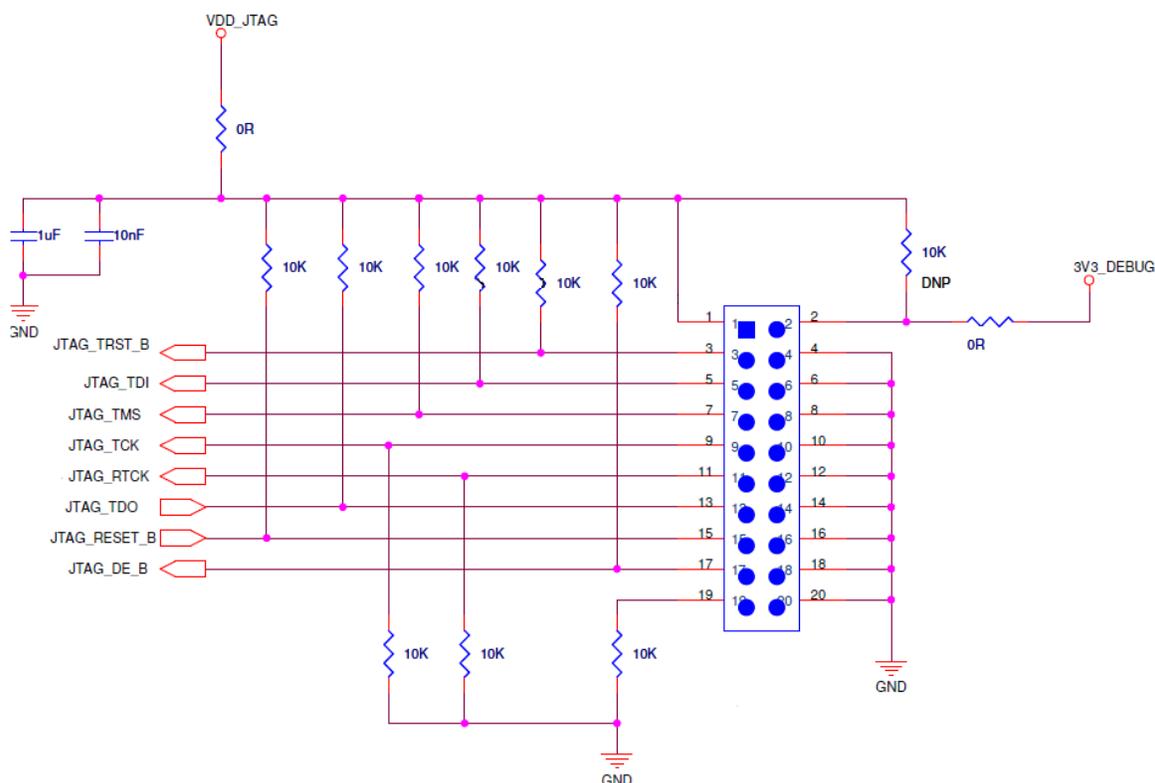
Figure 7. JTAG Recommended Connections

If customer does not want to have this interface on the final board, add this circuitry only to the prototypes. Remove the JTAG connector and circuitry at the stage of final production. Leave the JTAG signals routed to any connector so that it can be connected to another board which contains all other circuitry.

To connect an RS232 terminal to the i.MX31 processor, an RS232 (such as SP232) transceiver is needed. When the processor enters into bootstrap mode, the serial interface is used either for programming or debugging.

UART1 is a UART boot device. UART driver uses the communication parameters as shown in Table 1.

Table 1. UART Parameters for Booting

Parameter	Value
Baud Rate	115.2 KBaud
Parity Check	Disabled
Word Size	8 bits
Stop Bits	1 bit
RTS	Ignored
CTS	Controlled by host

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Table 1. UART Parameters for Booting (continued)

Parameter	Value
Receive Pin	RX1
Transmit Pin	TXD1

It supports two wire or four wire communication with the i.MX31 processor.

5   Boot Modes

The i.MX31 processor supports booting from several sources such as UART, USB, NAND, NOR and so on. When a prototype board is used, it is advisable to have all the boot modes available to test different devices or debug them. The recommended circuitry is a dip-switch device connected directly to the i.MX31.

Figure 8 shows the dip-switch arrangement connected to the i.MX31 processor.
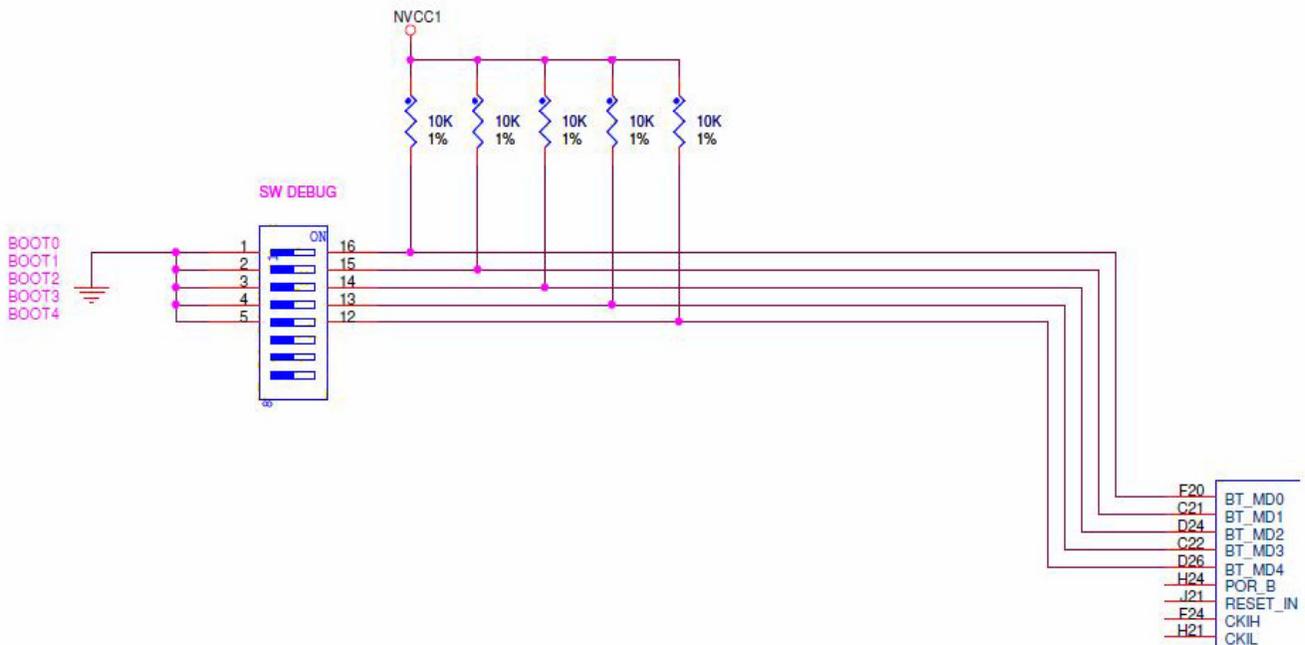
Figure 8. Dip-switch Connected to the i.MX31 Processor

It is recommended to add test points across all the signals to check if the boot mode is set correctly. At final production, remove the dip switch and replace it with single resistors. It is recommend to leave some resistors as Do Not Populate (DNP) so that the board can be triggered into the bootstrap mode at later stages to debug the design.

6 Revision History

Table 2 provides a revision history for this application note.

Table 2. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	01/2010	Initial release.

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