Freescale Semiconductor
Application Note

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i.MX233 CPU and HCLK Power Saving Features

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This application note describes the CPU Interrupt-Wait and the HCLK Auto-Slow features. It explains the procedure to enable each feature and also provides information about power saving.

The i.MX233 application processor integrates the clock power saving features that requires minimal development. After enabling these features, the hardware controls all the clock gating and divider operations without firmware. The battery power is reduced by 10% when these features are enabled. Also, when the processor is operated at the highest frequency, the battery power is reduced by 75%.

The information provided in this document is intended to supplement the i.MX233 Reference Manual.

Contents

1 Concept

The Interrupt-Wait feature is a hardware-controlled automatic clock gate for the CPU. Generally, when the CPU has completed all its outstanding instructions, it goes into idle mode and waits for the next instruction from an interrupt. Instead of being idle and wasting clock cycles and power, the Interrupt-Wait feature gates off the CPU clock until an interrupt is generated.

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This feature reduces the power used by the CPU, especially at higher frequencies that require high core voltages. Power management development also becomes easier. The firmware does not handle incremental CPU frequencies, instead it configures the CPU clock (PCLK) to the maximum frequency allowed by the current core voltage. When the CPU enters an idle state, excess clock is gated.

The HCLK Auto-Slow feature is similar to the Interrupt-Wait feature of the CPU. This feature reduces the frequency by a constant factor (normally set to 32), instead of gating the clock. The hardware monitors the HCLK bus (HBUS) for specific type of traffic and reduces the frequency when traffic is not present. The types of traffic to monitor are configurable. As the HCLK frequency is derived from the CPU frequency, the power consumed by the HCLK increases linearly with the CPU frequency. The Auto-Slow feature minimizes the power used by the HCLK to offset the dependency.

Each feature requires a couple of steps to be enabled and should be turned ON during the application's initialization routine. Once initialized, the hardware controls enabling or disabling the feature. The CPU is gated only when it is idle and HCLK slows down when there is no traffic. Hence, any program that requires high processing power still has all CPU and HCLK cycles available to meet the performance requirements.

2 Enabling Features

The power savings features explained below are enabled during the initialization. Each of these features require enabling at the hardware level. Once it is enabled, it does not require any application level handling and is automatically enabled and disabled by the hardware.

2.1 Enabling CPU Interrupt-Wait Feature

To enable Interrupt-Wait mode, perform the following actions:

- Modify the CPU clock control register to enable hardware ability.
- Call move-to-coprocessor (MCR) instruction to enable the internal gating signal

The INTERRUPT_WAIT bit is similar to the Wait-for-Interrupt (WFI) enable bit. Hence, it must be set prior to execution of MCR instruction.

The following steps are to be performed during initialization to optimize power savings:

1. The Interrupt-Wait feature is controlled by the INTERRUPT_WAIT bit in the HW_CLKCTRL_CPU register. Writing into the INTERRUPT_WAIT bitfield requires a read-modify-write (RMW) instruction.

Example 1. Read-Modify-Write Instruction

```
uclkctrl = HW_CLKCTRL_CPU_RD();
uclkctrl |= BM_CLKCTRL_CPU_INTERRUPT_WAIT;
HW_CLKCTRL_CPU_WR(uclkctrl);
```

2. After enabling the INTERRUPT_WAIT bit, add the following coprocessor instructions to the firmware's scheduler to enable the internal gating signal. This signal ensures that the Write buffers are drained and the processor is in idle state. On execution of the MCR instruction, the CPU clock stops and the processor halts the instruction, waiting for an interrupt.

Example 2. Coprocessor Instruction

```
asm (
// Note: R0 is used in the following example, but any usual
// <Rd> register may be used.
"mov R0, 0;" // Rd SBZ (should be zero)
"mcr p15,0,r0,c7,c0,4;"//Drain write buffers, idle CPU clock & processor,
// and stop processor at this instruction
"nop"); // The lr sent to handler points here after RTI
```

After execution of the MCR WFI command, the processor halts the MCR instruction. When an interrupt or Fast Interrupt Request (FIQ) occurs, the MCR instruction is executed and the Interrupt Request (IRQ) or FIQ handler is entered normally. The return link passed to the handler is automatically adjusted by the above MCR instruction such that, a normal return from the interrupt results in continuing the execution of the instruction that immediately follows MCR. The Link Register (LR) contains the address of the MCR instruction plus eight, such that a typical return from interrupt instruction (for example, `subs pc, LR, 4`) returns to the instruction that immediately follows MCR (like the NOP in Example 2).

When the clock control INTERRUPT_WAIT bit is set and the MCR WFI instruction is executed, the CPU stops until an interrupt occurs. The actual condition that restarts the CPU is determined by ORing all enabled interrupt requests, including the interrupts directed to the FIQ CPU input. The ICOLL_BUSY output signal from the Interrupt Collector (ICOLL) communicates this information to the clock control. This function does not pass through the normal ICOLL state machine. It starts the CPU clock after an enabled interrupt arrives.

2.2 Enabling HCLK Auto-Slow Feature

The HCLK Auto-Slow feature is a dynamic clock frequency management controller that monitors system performance requirements and scales HCLK to meet the performance needs. It monitors the HBUS for traffic. Depending on the type, it scales down the frequency to save power or restores the frequency to its normal value for performance.

To enable the HCLK Auto-Slow feature, perform the following steps:

1. Select the HBUS traffic to monitor enabling or disabling each activity in the HW_CLKCTRL_HBUS register as shown below:

```
HW_CLKCTRL_HBUS.B.DCP_AS_ENABLE = 1;
HW_CLKCTRL_HBUS.B.PXP_AS_ENABLE = 1;
HW_CLKCTRL_HBUS.B.CPU_DATA_AS_ENABLE = 1;
HW_CLKCTRL_HBUS.B.CPU_INSTR_AS_ENABLE = 1;
```

2. Enable the Auto-Slow feature.

```
HW_CLKCTRL_HBUS.B.AUTO_SLOW_MODE = 1;
```

The controller monitors eight different activities and enables the slow divider value. Some activities are based on bus traffic and others are based on coprocessor or CPU access activity. Change the monitoring activities to optimize an application. In some cases, disabling a specific activity to Auto-Slow mode increases the performance or the power usage because of the overhead necessary to perform the frequency changes.

3. Select the slow divide value.

```
HW_CLKCTRL_HBUS.B.SLOW_DIV = BV_CLKCTRL_HBUS_SLOW_DIV__BY32;
```

The slow divider values can be 1, 2, 4, 8, 16, or 32. The best power usage is achieved with a divider of 32. Different values allow optimization for specific applications. For activities that operate at high frequencies, set the divider value less than 32, as it increases the performance and saves power.

3 Power Measurement Analysis

The Interrupt-Wait mode reduces system power automatically in the hardware after configuring the feature in the application's initialization routine. On enabling this feature, it provides at least 3% power saving at 12 MHz CPU frequency and 38% power saving at 454 MHz CPU frequency.

3.1 Comparison Between Enabling and Disabling the Features

The power savings of the Interrupt-Wait and Auto-Slow features can be best visualized by varying the CPU frequency and by forcing the core voltage and HCLK divider to remain constant. These are not the normal settings for the core voltage and HCLK divider, but they allow to visualize the significant benefits of enabling these features.

Figure 1 illustrates the power used in the following conditions (as shown in the legend):

- Either of the features is not enabled
- Interrupt-Wait is enabled
- Interrupt-Wait and Auto-Slow features are enabled

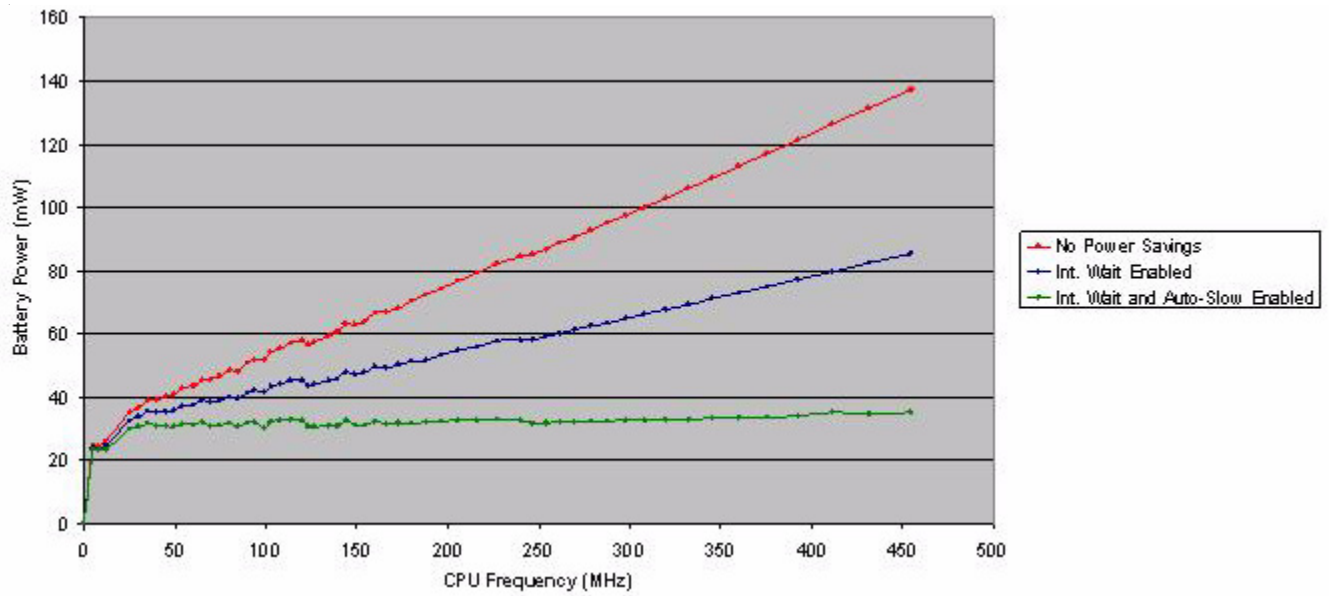

Figure 1. Battery Power with Constant Core Voltage and Constant HCLK Divider

The CPU frequency is swept from 0 to 454 MHz. The HCLK divider remains at 3 and the core voltage remains constant at 1.55V. The battery voltage is maintained at 3.7V throughout the measurements. The data for Figure 1 is available in Appendix A.

Figure 1 shows that the Interrupt-Wait mode decreases the battery power. But the power curve increases with the CPU frequency as HCLK frequency is branched from the CPU clock through an integer divider. It is not gated when the CPU is gated as the peripheral blocks may still use the HBUS when the CPU is idle (for example, the operation of the DMA Controller). The power used by the HBUS can still be reduced.

The Auto-Slow feature automatically reduces the HCLK frequency which in turn reduces the power. The maximum HCLK frequency for the i.MX233 is 205 MHz. When the maximum slow divide value is 32, the HCLK is forced to 6.4 MHz approximately, which is the worst case low power frequency.

The Int. Wait and Auto-Slow Enabled curve in Figure 1 shows another interesting characteristic of the power saving modes. The battery power consumed is nearly constant for the CPU and the HCLK from 24 MHz to 454 MHz, when the core voltage and the HCLK divider remain constant. In fact, the power varies by 5 mW between 24 MHz and 454 MHz when the Phase Locked Loop (PLL) is ON.

Table 1 shows the power differences at different CPU frequencies, when both the Interrupt-Wait and the HCLK Auto-Slow features are enabled and disabled.

Table 1. Power Differences Calculated at Different CPU Frequencies

CPU (MHz)	Battery Power (mW)		
	Both Features Disabled	Both Features Enabled	Difference
12[1]	25.8	23.3	2.5
30	36.7	30.5	6.2
60	43.7	31.1	12.6
120	57.9	32.5	25.4
240	84.5	32.6	51.9
320	103.0	32.8	70.2
360	113.0	33.5	79.5
454	137.2	35.2	102.0

1 At 12 MHz, the PLL is turned OFF. PCLK and HCLK are sourced from a 24 MHz crystal.

As shown in Table 1, there is significant difference in power when both features are enabled and disabled. At 12 MHz, the difference in power is 2.5 mW which is approximately a 10% reduction in power. At 454 MHz, the power is reduced approximately by 75% when both features are enabled.

3.2 Common Usage Power Comparison

Under normal operation, the HCLK divider and the core voltage changes dynamically as the CPU frequency changes. The settings for the HCLK divider and the core voltage have been optimized in the BSP to minimize the battery power usage. Figure 2 illustrates the difference in battery power when both the Interrupt-Wait and the HCLK Auto-Slow features are enabled and disabled. The CPU is minimally loaded with the test case and is restarted for every 10 ms of the OS tick.

The Freescale BSP uses discrete power states and takes the advantage of the Interrupt-Wait and the Auto-Slow features to reduce the battery power. The power states are selected by choosing the highest CPU frequency supported by a voltage setting. As shown in Figure 2, the core voltage increases as the CPU frequency increases. As the Interrupt -Wait and the Auto-Slow features reduce the power curve to a flat slope (as shown in Figure 1), the increase in power as CPU frequency increases can be attributed to the increase in the core voltage.

Figure 2 shows a graph plot between CPU frequency (MHz) and Battery Power (mW) when both the features are enabled and disabled.

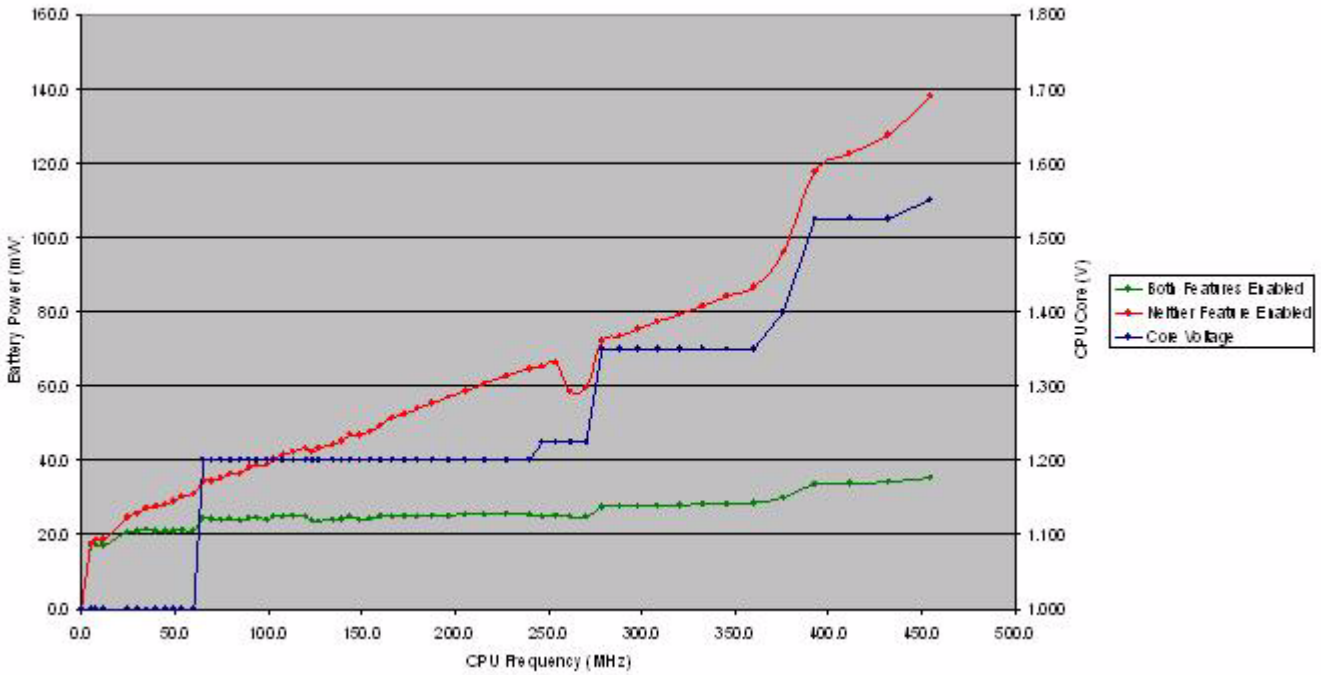

Figure 2. Battery Power with Variable HCLK Divider and VDDD voltage

NOTE

There are three local minima in the power curve close to 64 MHz, 127 MHz and 261 MHz. These data points are real and functions of the HCLK divider and the core voltage setting. For more information, see Appendix C.

3.3 Discrete Power States

The power usage at each core voltage setting allows the power management driver to use discrete power states with large CPU frequency steps between each state. Table 2 lists the minimum and maximum power used at each voltage setting. The values are obtained from Appendix B.

Table 2 shows that the largest difference in power is 2.0 mW at 1.2 V core voltage. This corresponds to the CPU frequency range of 64 MHz–240 MHz. As shown in Figure 2, the maximum and minimum power values do not necessarily correspond to the maximum and minimum CPU frequencies. The maximum power used is at 227 MHz and the minimum power used is at 127 MHz (see Appendix B). These variations are the results of the PLL fractional divider values used to achieve the resolution needed for the specified frequency.As the worst case difference in power is 2.0 mW, creating more states with finer resolution for the CPU frequency results in minimal additional power saving. It would be better if the development and optimization time is spent on other components of the application.

Table 2 shows the power difference at each core voltage step.

Table 2. Power Differences at Each Core Voltage Step

Core Voltage (V)	Battery Power (mW)[1]		
	Minimum	Maximum	Difference
1.000[2]	17.2	17.3	2.5
1.000[3]	20.6	21.3	0.7
1.200	23.7	25.7	2.0
1.225	24.8	25.0	0.2
1.350	27.5	28.4	1.0
1.400	29.9	29.9	0.0
1.525	33.4	34.1	0.6

1 Battery voltage is 3.7 V.
2 At CPU frequencies of 24 MHz and below where the PLL is OFF.
3 At CPU frequencies above 24 MHz where the PLL is ON.

4 Conclusion

The i.MX233 application processor offers a simple but robust power saving features. The Interrupt -Wait mode for the CPU gates unnecessary clock cycles and the HCLK Auto-Slow feature decreases the HCLK frequency when the bus is not in use. These features require some register configurations during the initialization sequence but require no firmware management after the initial setup and are completely controlled by the hardware. Additionally, the two power saving features create a flat power curve. This allows a simpler power management driver that uses discrete states with large frequency ranges.

The features can be implemented with minimum development time. It can easily achieve nearly 75% power reduction at 454 MHz. The battery power also reduces at least by 10% when these features are enabled. Enable these features to obtain the most optimized power consumption for an application.

5 References

i.MX23 Applications Processor Data Sheet (IMX23EC) available at the link on the last page of this document.

6 Revision History

Table 3 provides a revision history for this application note.

Table 3. Document Revision History

Rev. Number	Date	Substantive Change(s)
0	01/2010	Initial release.

Appendix A Constant Core Voltage and Constant HCLK Divider Current and Power Measurements

Table 4 shows the current and power readings at different CPU frequencies when the Interrupt-Wait and the HCLK Auto-Slow feature are enabled and/or disabled (Constant Core voltage and HCLK divider).

Table 4. Current and Power Readings (Constant Core Voltage and HCLK Divider)

Chip Settings				Battery Measurements					
Frequency		Core Voltage		Voltage	Current		Power		
CPU (MHz)	HCLK (MHz)	VDDD (v)	VDDDBO (V)	BATTERY VOLTAGE (V)	INT_WAIT ENABLED	INT_WAIT DISABLED	No Power Savings	Int. Wait Enabled	Int Wait and Auto-Slow Enabled
0.0	0.0	1.550	1.450	3.7	0.0	0.0	0.0	0.0	0.0
4.8	1.6	1.550	1.450	3.7	6.5	6.7	24.8	23.9	23.3
8.0	2.7	1.550	1.450	3.7	6.4	6.6	24.3	23.5	23.3
12.0	4.0	1.550	1.450	3.7	6.7	7.0	25.8	24.6	23.3
24.8	8.3	1.550	1.450	3.7	8.8	9.5	35.2	32.7	30.0
30.0	10.0	1.550	1.450	3.7	9.1	9.9	36.7	33.6	30.5
35.0	11.7	1.550	1.450	3.7	9.6	10.5	38.9	35.6	31.6
40.0	13.3	1.550	1.450	3.7	9.5	10.6	39.2	35.1	30.9
45.0	15.0	1.550	1.450	3.7	9.6	10.8	40.1	35.5	30.7
49.7	16.6	1.550	1.450	3.7	9.7	11.1	40.9	35.8	30.6
54.0	18.0	1.550	1.450	3.7	10.0	11.5	42.7	37.1	31.4
60.0	20.0	1.550	1.450	3.7	10.1	11.8	43.7	37.4	31.1
65.0	21.7	1.550	1.450	3.7	10.5	12.2	45.1	39.0	32.1
69.7	23.2	1.550	1.450	3.7	10.3	12.3	45.4	38.2	30.9
74.5	24.8	1.550	1.450	3.7	10.5	12.6	46.7	39.0	31.1
80.0	26.7	1.550	1.450	3.7	10.8	13.1	48.4	40.1	31.7
84.7	28.2	1.550	1.450	3.7	10.7	13.0	48.2	39.4	30.5
90.0	30.0	1.550	1.450	3.7	11.2	13.7	50.7	41.3	31.8
93.9	31.3	1.550	1.450	3.7	11.3	14.0	51.8	42.0	32.0
99.3	33.1	1.550	1.450	3.7	11.2	14.0	51.9	41.6	30.3
102.9	34.3	1.550	1.450	3.7	11.7	14.6	54.1	43.4	32.4
108.0	36.0	1.550	1.450	3.7	11.9	15.0	55.5	44.1	32.7
113.7	37.9	1.550	1.450	3.7	12.2	15.4	57.0	45.1	33.0
120.0	40.0	1.550	1.450	3.7	12.2	15.7	57.9	45.3	32.5
123.4	41.1	1.550	1.450	3.7	11.8	15.3	56.6	43.6	30.5

Table 4. Current and Power Readings (Constant Core Voltage and HCLK Divider) (continued)

Chip Settings				Battery Measurements					
127.1	42.4	1.550	1.450	3.7	11.9	15.5	57.5	44.1	30.6
135.0	45.0	1.550	1.450	3.7	12.2	16.1	59.4	45.2	30.7
139.4	46.5	1.550	1.450	3.7	12.4	16.3	60.5	45.8	30.9
144.0	48.0	1.550	1.450	3.7	13.0	17.1	63.2	48.0	32.6
149.0	49.7	1.550	1.450	3.7	12.7	17.0	62.7	47.1	31.1
154.3	51.4	1.550	1.450	3.7	12.9	17.3	64.1	47.8	31.2
160.0	53.3	1.550	1.450	3.7	13.4	18.0	66.6	49.6	32.4
166.2	55.4	1.550	1.450	3.7	13.3	18.1	66.9	49.3	31.5
172.8	57.6	1.550	1.450	3.7	13.6	18.4	68.1	50.3	31.7
180.0	60.0	1.550	1.450	3.7	13.8	19.0	70.3	51.2	31.8
187.8	62.6	1.550	1.450	3.7	14.0	19.6	72.3	51.7	32.0
196.4	65.5	1.550	1.450	3.7	14.4	20.1	74.4	53.4	32.2
205.7	68.6	1.550	1.450	3.7	14.8	20.7	76.7	54.7	32.5
216.6	72.0	1.550	1.450	3.7	15.2	21.4	79.3	56.1	32.7
227.4	75.8	1.550	1.450	3.7	15.6	22.2	82.2	57.6	33.0
240.0	80.0	1.550	1.450	3.7	15.7	22.8	84.5	58.0	32.6
246.9	82.3	1.550	1.450	3.7	15.8	23.0	85.0	58.3	31.6
254.1	84.7	1.550	1.450	3.7	16.0	23.5	86.8	59.2	31.7
261.8	87.3	1.550	1.450	3.7	16.3	24.0	88.7	60.2	31.9
270.0	90.0	1.550	1.450	3.7	16.6	24.5	90.7	61.3	32.0
278.7	92.9	1.550	1.450	3.7	16.9	25.1	92.8	62.4	32.2
288.0	96.0	1.550	1.450	3.7	17.2	25.7	95.1	63.6	32.3
297.9	99.3	1.550	1.450	3.7	17.5	26.4	97.5	64.9	32.5
308.6	102.9	1.550	1.450	3.7	17.9	27.1	100.2	66.3	32.6
320.0	106.7	1.550	1.450	3.7	18.3	27.8	103.0	67.7	32.8
332.3	110.8	1.550	1.450	3.7	18.7	28.7	106.0	69.3	33.0
345.6	115.2	1.550	1.450	3.7	19.2	29.5	109.2	71.1	33.3
360.0	120.0	1.550	1.450	3.7	19.7	30.5	113.0	72.9	33.5
375.7	125.2	1.550	1.450	3.7	20.3	31.6	117.0	75.0	33.8
392.7	130.9	1.550	1.450	3.7	20.9	32.8	121.3	77.2	34.0
411.4	137.1	1.550	1.450	3.7	21.5	34.1	126.1	79.7	35.0
432.0	144.0	1.550	1.450	3.7	22.3	35.5	131.5	82.4	34.7
454.7	151.6	1.550	1.450	3.7	23.1	37.1	137.2	85.5	35.2

Appendix B Variable Core Voltage and Variable HCLK Divider Current and Power Measurements

Table 5 shows the current and power readings at different CPU frequencies when the Interrupt-Wait and the HCLK Auto-Slow feature are enabled and/or disabled (Variable Core voltage and HCLK divider).

Table 5. Current and Power Readings (Variable Core Voltage and HCLK Divider)

Chip Settings				Battery Measurements				
Frequency		Core Voltage		Voltage	Current		Power	
CPU (MHz)	HCLK (MHz)	Core Voltage	VDDDBO (V)	BATTERY VOLTAGE (V)	INT_WAIT ENABLED	INT_WAIT DISABLED	Both Features Enabled	Neither Features Enabled
0.0	0.0	1.000	0.925	3.7	0.0	0.0	0.0	0.0
4.8	4.8	1.000	0.925	3.7	4.7	4.8	17.2	17.6
8.0	8.0	1.000	0.925	3.7	4.7	5.0	17.2	18.6
12.0	12.0	1.000	0.925	3.7	4.7	5.0	17.3	18.5
24.8	24.8	1.000	0.925	3.7	5.6	6.7	20.6	24.6
30.0	30.0	1.000	0.925	3.7	5.6	6.9	20.8	25.7
35.0	35.0	1.000	0.925	3.7	5.8	7.3	21.3	27.0
40.0	40.0	1.000	0.925	3.7	5.7	7.4	21.0	27.5
45.0	45.0	1.000	0.925	3.7	5.7	7.7	21.0	28.3
49.7	49.7	1.000	0.925	3.7	5.7	7.8	21.0	29.0
54.0	54.0	1.000	0.925	3.7	5.7	8.1	21.2	30.1
60.0	60.0	1.000	0.925	3.7	5.7	8.4	21.2	30.0
65.0	65.0	1.200	1.100	3.7	6.6	9.3	24.6	34.3
69.7	69.7	1.200	1.100	3.7	6.5	9.3	23.9	34.3
74.5	74.5	1.200	1.100	3.7	6.5	9.5	24.0	35.2
80.0	80.0	1.200	1.100	3.7	6.6	9.8	24.3	36.4
84.7	84.7	1.200	1.100	3.7	6.4	9.8	23.7	36.4
90.0	90.0	1.200	1.100	3.7	6.6	10.3	24.4	38.0
93.9	93.9	1.200	1.100	3.7	6.6	10.5	24.6	38.8
99.3	99.3	1.200	1.100	3.7	6.5	10.5	24.0	39.0
102.9	102.9	1.200	1.100	3.7	6.7	10.9	24.8	40.4
108.0	108.0	1.200	1.100	3.7	6.7	11.2	24.9	41.4
113.7	113.7	1.200	1.100	3.7	6.8	11.5	25.1	42.4
120.0	120.0	1.200	1.100	3.7	6.7	11.7	24.8	43.1
123.4	123.4	1.200	1.100	3.7	6.4	11.5	23.7	42.4

Table 5. Current and Power Readings (Variable Core Voltage and HCLK Divider) (continued)

Chip Settings				Battery Measurements				
127.1	127.1	1.200	1.100	3.7	6.4	11.6	23.8	43.1
135.0	135.0	1.200	1.100	3.7	6.5	12.0	23.9	44.4
139.4	139.4	1.200	1.100	3.7	6.5	12.2	23.9	45.2
144.0	144.0	1.200	1.100	3.7	6.7	12.7	24.9	47.0
149.0	149.0	1.200	1.100	3.7	6.5	12.7	24.1	46.8
154.3	154.3	1.200	1.100	3.7	6.5	12.9	24.2	47.8
160.0	160.0	1.200	1.100	3.7	6.7	13.4	24.8	49.4
166.2	166.2	1.200	1.100	3.7	6.7	13.9	24.8	51.4
172.8	172.8	1.200	1.100	3.7	6.7	14.2	24.9	52.6
180.0	180.0	1.200	1.100	3.7	6.7	14.6	24.9	53.9
187.8	187.8	1.200	1.100	3.7	6.8	15.0	25.1	55.4
196.4	98.2	1.200	1.100	3.7	6.8	15.4	25.2	56.9
205.7	102.9	1.200	1.100	3.7	6.9	15.9	25.3	58.6
216.0	108.0	1.200	1.100	3.7	6.9	16.4	25.5	60.6
227.4	113.7	1.200	1.100	3.7	7.0	16.9	25.7	62.7
240.0	120.0	1.200	1.100	3.7	6.9	17.4	25.4	64.5
246.9	123.4	1.225	1.125	3.7	6.7	17.6	24.9	65.2
254.1	127.1	1.225	1.125	3.7	6.8	18.0	25.0	66.5
261.8	130.9	1.225	1.125	3.7	6.7	15.8	24.8	58.5
270.0	135.0	1.225	1.125	3.7	6.7	16.1	24.9	59.7
278.7	139.4	1.350	1.250	3.7	7.4	19.4	27.5	71.9
288.0	144.0	1.350	1.250	3.7	7.4	19.9	27.5	73.5
297.9	149.0	1.350	1.250	3.7	7.5	20.4	27.7	75.3
308.6	154.3	1.350	1.250	3.7	7.5	20.9	27.8	77.2
320.0	160.0	1.350	1.250	3.7	7.6	21.4	27.9	79.3
332.3	166.2	1.350	1.250	3.7	7.6	22.0	28.1	81.5
345.6	172.8	1.350	1.250	3.7	7.7	22.7	28.3	84.0
360.0	120.0	1.350	1.250	3.7	7.7	23.4	28.4	86.6
375.7	125.2	1.400	1.300	3.7	8.1	25.9	29.9	95.9
392.7	130.9	1.525	1.425	3.7	9.0	31.8	33.4	117.7
411.4	137.1	1.525	1.425	3.7	9.1	33.1	33.7	122.4
432.0	144.0	1.525	1.425	3.7	9.2	34.5	34.1	127.5
454.7	151.6	1.550	1.450	3.7	9.5	37.3	35.3	137.9

Appendix C Power Curve Local Minima

There are power measurements that do not fit in the curves for Interrupt -Wait Enabled and Disabled. These points are real and are functions of the HCLK divider and the core voltage settings. The HCLK divider is increased by one, before increasing the core voltage.

Figure 3 shows that the drop in power occurs when the HCLK divider increases, but the core voltage has not increased.

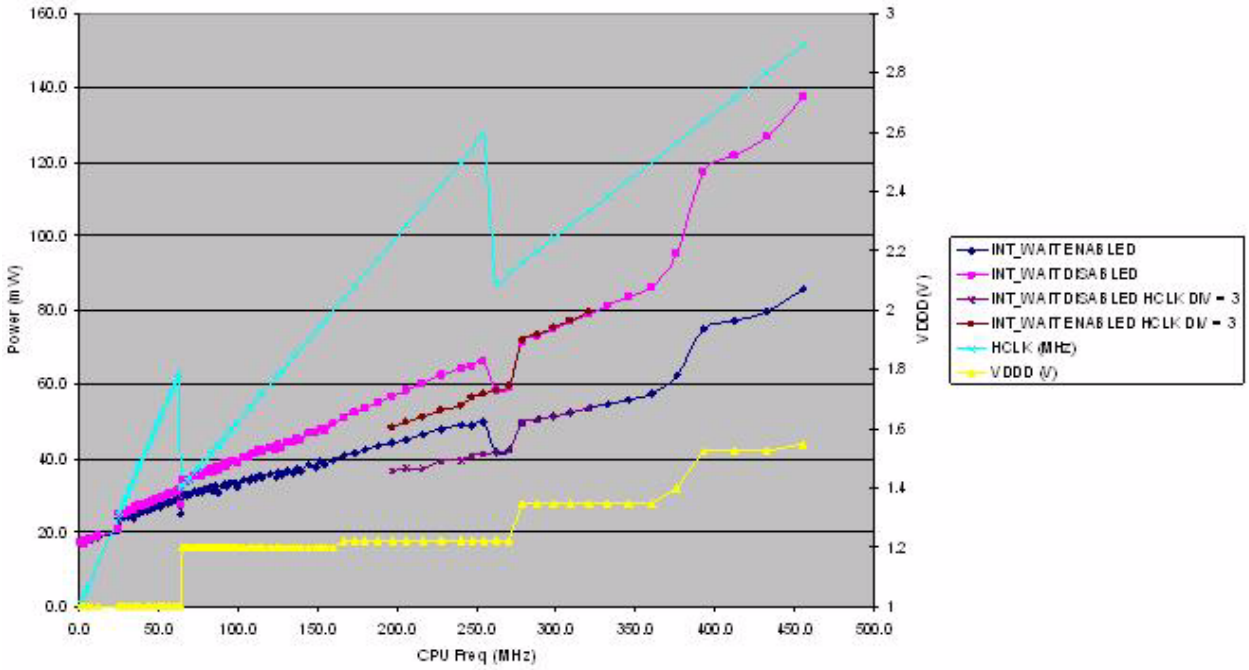

Figure 3. Power Curve Local Minima

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