Freescale Semiconductor
Application Note

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i.MX51 Power-Up Sequence

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This application note describes the power-up sequence that should be met for the i.MX51 processor. It also explains the timing diagrams when the Atlas AP Lite (MC13892) is used as Power Management Integrated Circuit (PMIC).

Contents

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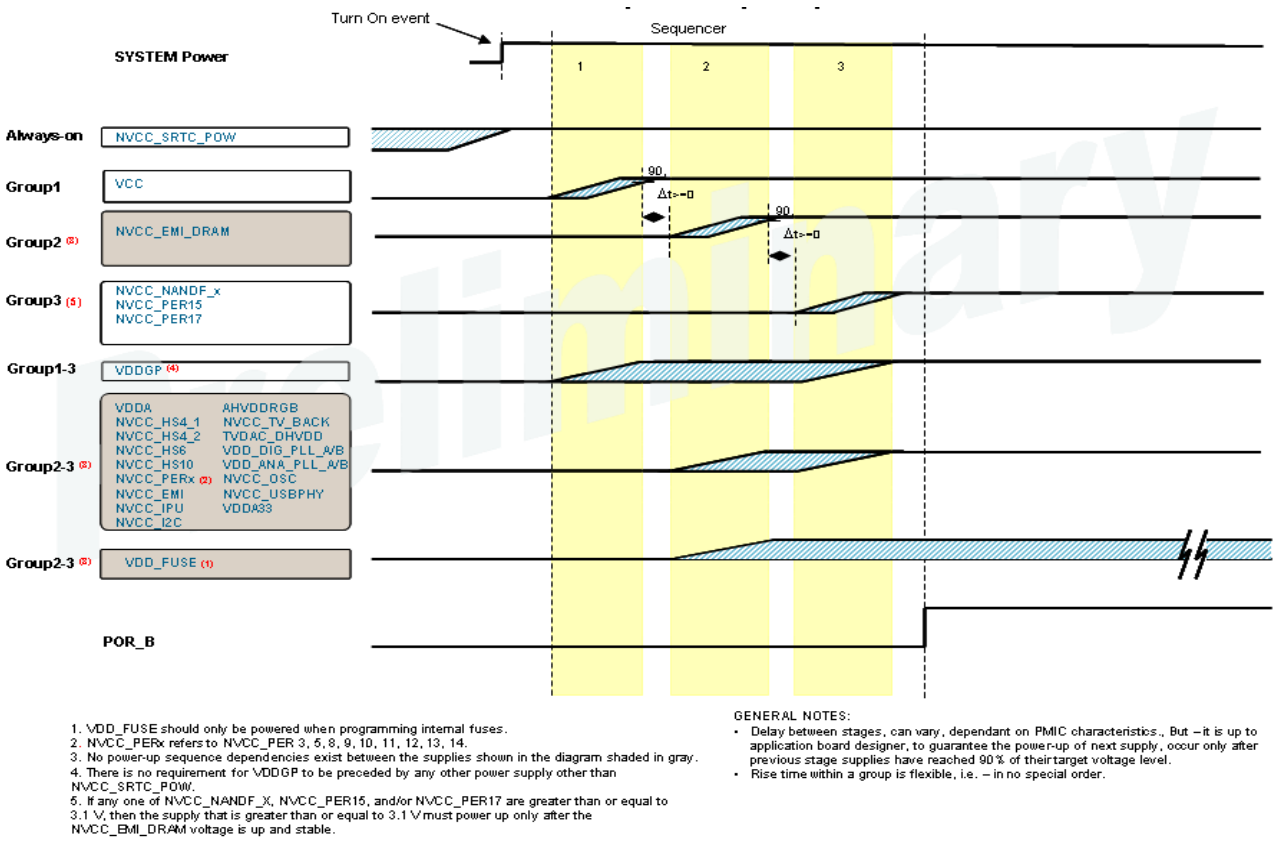
1 Power-Up Sequence

Figure 1 and Figure 2 show the timing diagrams for the power-up sequence of the i.MX51.



1. VDD_FUSE should only be powered when programming internal fuses.
2. NVCC_PERx refers to NVCC_PER 3, 5, 8, 9, 10, 11, 12, 13, 14.
3. No power-up sequence dependencies exist between the supplies shown in the diagram shaded in gray.
4. There is no requirement for VDDGP to be preceded by any other power supply other than NVCC_SRTC_POW.
5. If any one of NVCC_NANDF_X, NVCC_PER15, and/or NVCC_PER17 are greater than or equal to 3.1 V, then the supply that is greater than or equal to 3.1 V must power up only after the NVCC_EMI_DRAM voltage is up and stable.

GENERAL NOTES:

- Delay between stages, can vary, dependant on PMIC characteristics., But – it is up to application board designer, to guarantee the power-up of next supply, occur only after previous stage supplies have reached 90% of their target voltage level.
- Rise time within a group is flexible, i.e. – in no special order.

Figure 1. Timing Diagram for the Power-Up Sequence when NVCC_NANDF_X, NVCC_PER15, and NVCC_PER17 are greater than or equal to 3.1 V

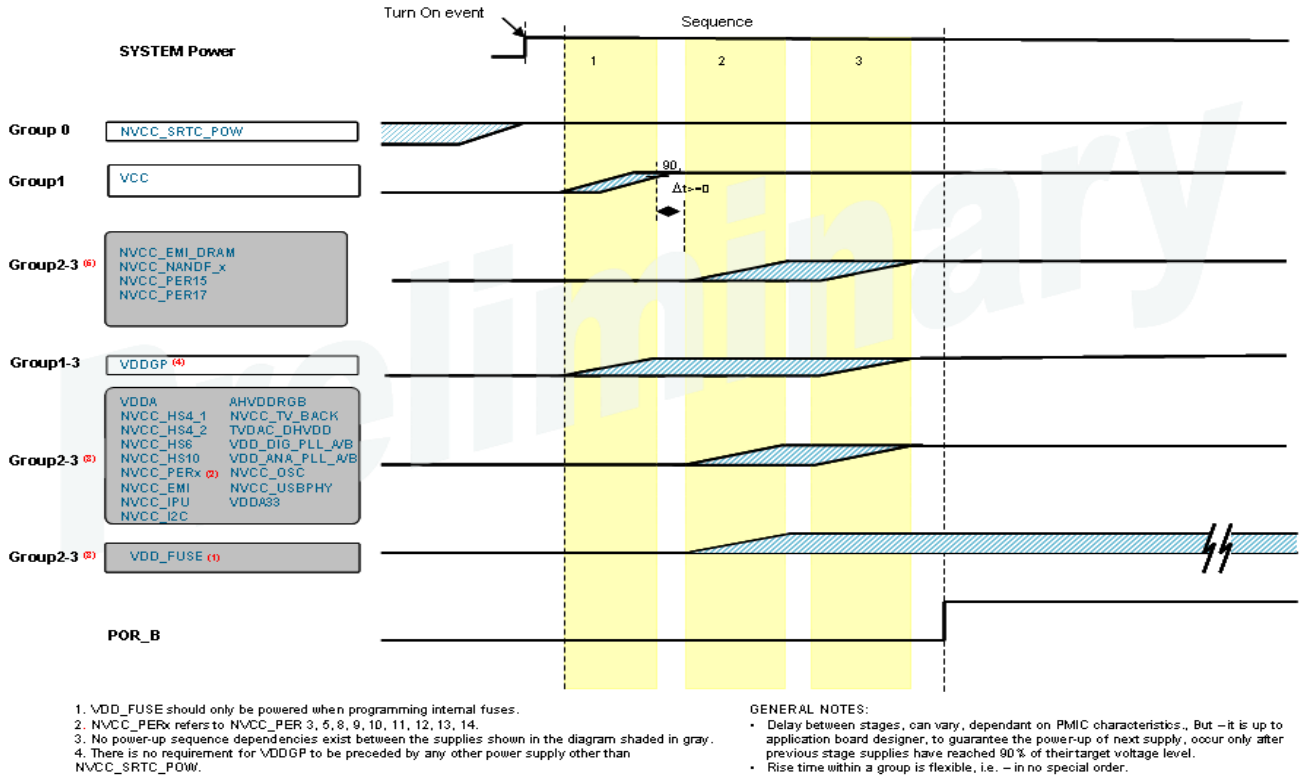


Figure 2. Timing Diagram for the Power-Up Sequence when NVCC_PER15, NVCC_PER17, and NVCC_NANDF_x are less than 3.1 V

Refer to the section, Power-Up Sequence, in the *i.MX51 Applications Processors for Consumer and Industrial Products* (IMX51CEC), for more information on the i.MX51 power-up sequence.

2 Timing Diagrams

Figure 3 shows the timing diagram and the sequence of the power rails implemented on the i.MX51 EVK board. The timing is given by MC13982.

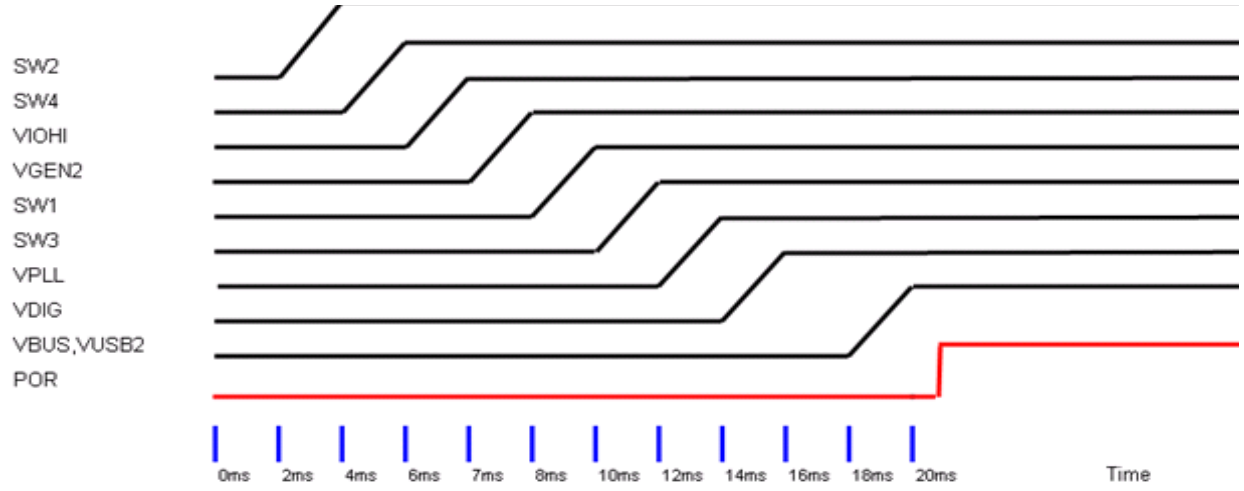


Figure 3. Timing Diagram for the Power-Up Sequence of the i.MX51 Using MC13982.

Table 1 and Table 2 show the power rails connected to the switching regulator and LDO (Low-Dropout Regulator) from the Atlas.

Table 1. Power Rails Connected to the i.MX51

VSRTC	SW1	SW2	SW3	SW4	SWBST	VUSB
NVCC_SRTC_POW	VDDGP	VCC	VDDA	NVCC_EMI_DRAM	For LEDS	VDDA33
—	—	—	VDD_DIG_PLL_A	NVCC_NANDF_A1	—	—
—	—	—	VDD_DIG_PLL_B	NVCC_NANDF_A2	—	—
—	—	—	VREG	NVCC_NANDF_B	—	—
—	—	—	—	NVCC_NANDF_C	—	—
—	—	—	—	NVCC_EMI_DRAM	—	—
—	—	—	—	NVCC_PER3	—	—
—	—	—	—	NVCC_PER11	—	—
—	—	—	—	NVCC_PER14	—	—
—	—	—	—	NVCC_I2C	—	—
—	—	—	—	NVCC_HS4_1	—	—

Table 2. Power Rails Connected to the i.MX51

VUSB2	VPLL	VDIG	VIOHI	VGEN2
NVCC_USBPHY	VDD_ANA_PLL_B	For Audio	NVCC_HS10	VDD_FUSE
NVCC_OSC	VDD_ANA_PLL_A	—	NVCC_HS6	NVCC_PER15

Table 2. Power Rails Connected to the i.MX51 (continued)

VUSB2	VPLL	VDIG	VIOHI	VGEN2
—	—	—	NVCC_HS4_2	—
—	—	—	NVCC_IPU	—
—	—	—	NVCC_PER5	—
—	—	—	NVCC_PER8	—
—	—	—	NVCC_PER9	—
—	—	—	NVCC_PER10	—
—	—	—	NVCC_PER12	—
—	—	—	NVCC_PER13	—

The VDDGP is powered at the fifth step of the PMIC sequence. The RTC module turns ON the NVCC_SRTC_POW from MC13892. The 2 ms step is given by the MC13892. The USB supply, VUSB is enabled only if a 5 V supply is available on UVBUS. The SWBST is enabled through the SPI control bit.

3 Dependencies between Supplies

Due to the nature of the design, dependencies between the supplies exist in the following cases:

- If the power supply of any of the NVCC_HSx (grouping NVCC_HS6, NVCC_HS10, NVCC_HS4_1, and NVCC_HS4_2 supplies) supplies or VREG supply is pulled down, it results in high leakage current from VCC through the supply that is pulled down.
- If the power supply of NVCC_NANDFx, NVCC_PER15 or NVCC_PER17 is pulled down when NVCC_EMI_DRAM is ON, it results in some leakage from NVCC_EMI_DRAM through the supply that is pulled down. Though this is part of the recommended power-up sequence, it is not desirable if NVCC_NANDFx is to be powered OFF for long time when NVCC_EMI_DRAM is ON.
- If the power supply of VDD_ANA_PLLx is pulled down, when VDD_DIG_PLLx is ON, it results in small leakage (couple of mA) from VDD_DIG_PLLx through VDD_ANA_PLLx. Though this occurs during the power-up sequence, it is not desirable if VDD_ANA_PLLx is to be powered OFF for long time, when VDD_DIG_PLLx is ON.
- If these supplies are not pulled down and left unconnected with high resistive path to ground or at high impedance state, the leakage is not observed. Consider the potential leakage paths when designing the board or when the power supplies are turned OFF (for example, when the device is in the suspended mode), to avoid power wastage.

4 Guidelines and Limitations for Power Supplies

If any supply (NVCC_NANDFx, NVCC_PER15, or NVCC_PER17) for UHVIO cells is greater than or equal to 3.1 V (at maximum, not nominal), then it must be powered up after NVCC_EMI_DRAM. For example, a supply of 2.9 V +/- 0.1 V is acceptable and has no restriction with respect to

NVCC_EMI_DRAM. Violating this requirement causes reliability issues to the design circuitry as NVCC_EMI_DRAM is used as bias voltage for the UHVIO cells.

VREG supply pin is not used and it should remain floated. FASTR_ANA and FASTR_DIG supply pins are reserved for Freescale manufacturing use and should be connected to ground.

If TVE module is not used, it is recommended to tie the supplies: TVDAC_DHVDD, NVCC_TV_BACK,and AHVDDRGB to ground. The x_back signals are feedback signals and it is recommended to connect them to ground. Comp pin should be left unconnected. Also, the TVE supplies and signals could remain floating for additional flexibility.

Consider the following points:

- Check if the sequence and voltage levels for the i.MX51 are correct, when PMICs other than the MC13892 are used to supply the i.MX51.
- Follow the recommended parameters and values for the passive components for the MC13892.
- The PMIC layout can influence the behavior of the voltage measurements.

5 Revision History

Table 3 provides a revision history for this application note.

Table 3. Document Revision History

Rev. Number	Date	Substantive Change(s)
4	10/2010	The following changes have been made: • Updated Figure 1 • Updated Figure 2 • Updated Section 4, “Guidelines and Limitations for Power Supplies”
3	06/2010	The following changes have been made: • Updated Section 1, “Power-Up Sequence” • Updated Figure 1
2	06/2010	Updated Figure 3 and added Figure 2.
1	05/2010	Updated voltages in Note in Section 1, “Power-Up Sequence” Removed comments in Section 3, “Dependencies between Supplies”
0	04/2010	Initial release.

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