Freescale Semiconductor
Application Note

Document Number: AN4054
Rev. 2, 10/2010

Interfacing mDDR and DDR2 Memories with the i.MX51

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This application note describes the interfacing of Mobile Double Data Rate (mDDR) and Double Data Rate 2 (DDR2) memories with the i.MX51 processor. The application note also describes the routing guidelines with figures and examples.

Contents

1 i.MX51 SDRAM Controller

The i.MX51 Synchronous Dynamic Random Access Memory (SDRAM) controller can be interfaced with Single Data Rate SDRAM (SDR SDRAM), mDDR or DDR2 SDRAM memories. The DDR controller of the i.MX51 conforms to the immediate signals to interface with the memory devices.

The buses and signals associated with the SDRAM controller are as follows:

- Address bus and their bank control signals:
  - DRAM_A0—DRAM_A12
  - DRAM_SDBA0—DRAM_SDBA2
- Data bus and their buffer control signals:
  - DRAM_D0—DRAM_D31

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  - DRAM_DQS0/DQS0_B—DRAM_DQS3/DQS3_B
  - DRAM_DQM0—DRAM_DQM3
- Control signals:
  - RAS
  - CAS
  - SDWE
  - DRAM_SDCKE0—DRAM_SDCKE1
  - DRAM_CS0—DRAM_CS1
  - DRAM_ODT0—DRAM_ODT1
- Clock signals:
  - DRAM_SDCLK
  - DRAM_SDCLK_B

Figure 1 shows the block diagram of the DDR2 interfaced with the i.MX51 using the Evaluation Kit (EVK) board.

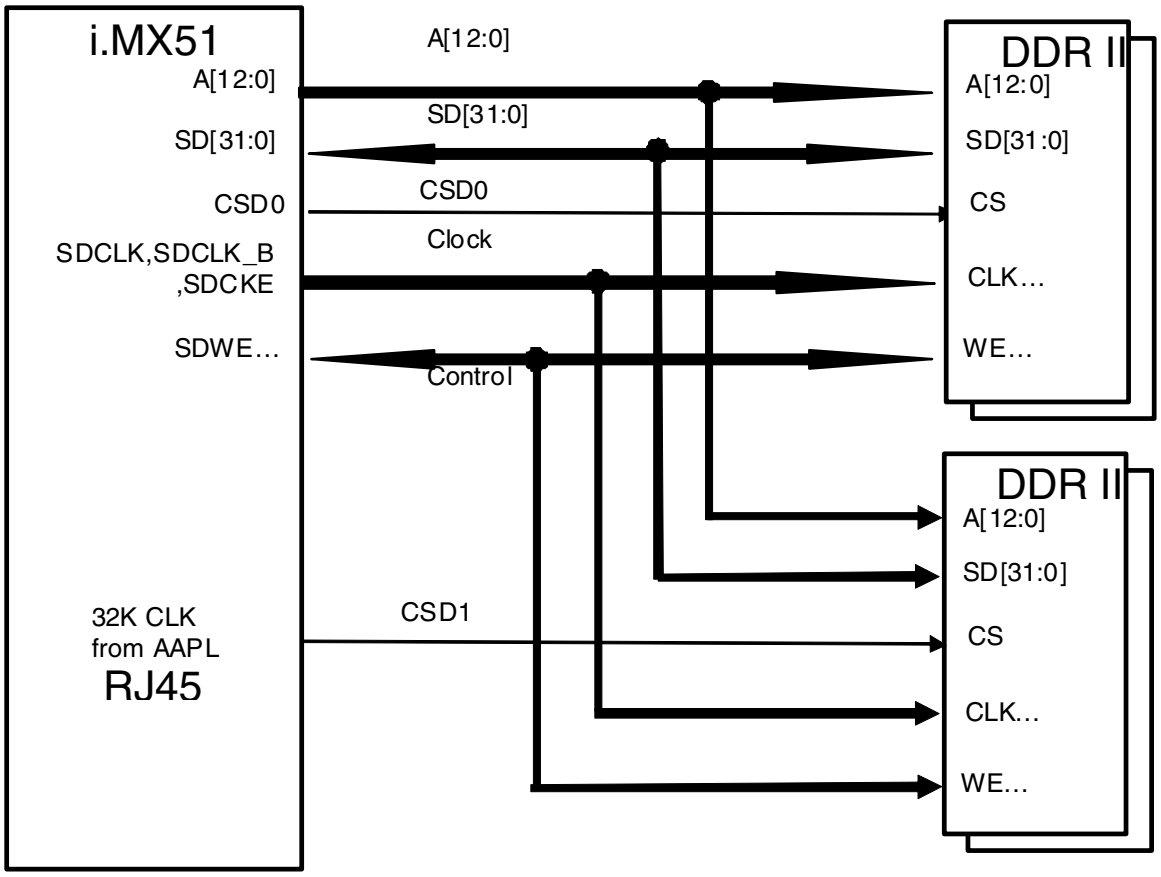

Figure 1. Interfacing between i.MX51 and DDR2

2 Memory Interfacing

This section describes the interfacing of the mDDR and DDR2 memories with the i.MX51 processor.

2.1 mDDR Interfacing

Figure 2 shows the interfacing between the i.MX51 and mDDR. The mDDR device used in Figure 2 is the MT46H64M16LFCK-5.

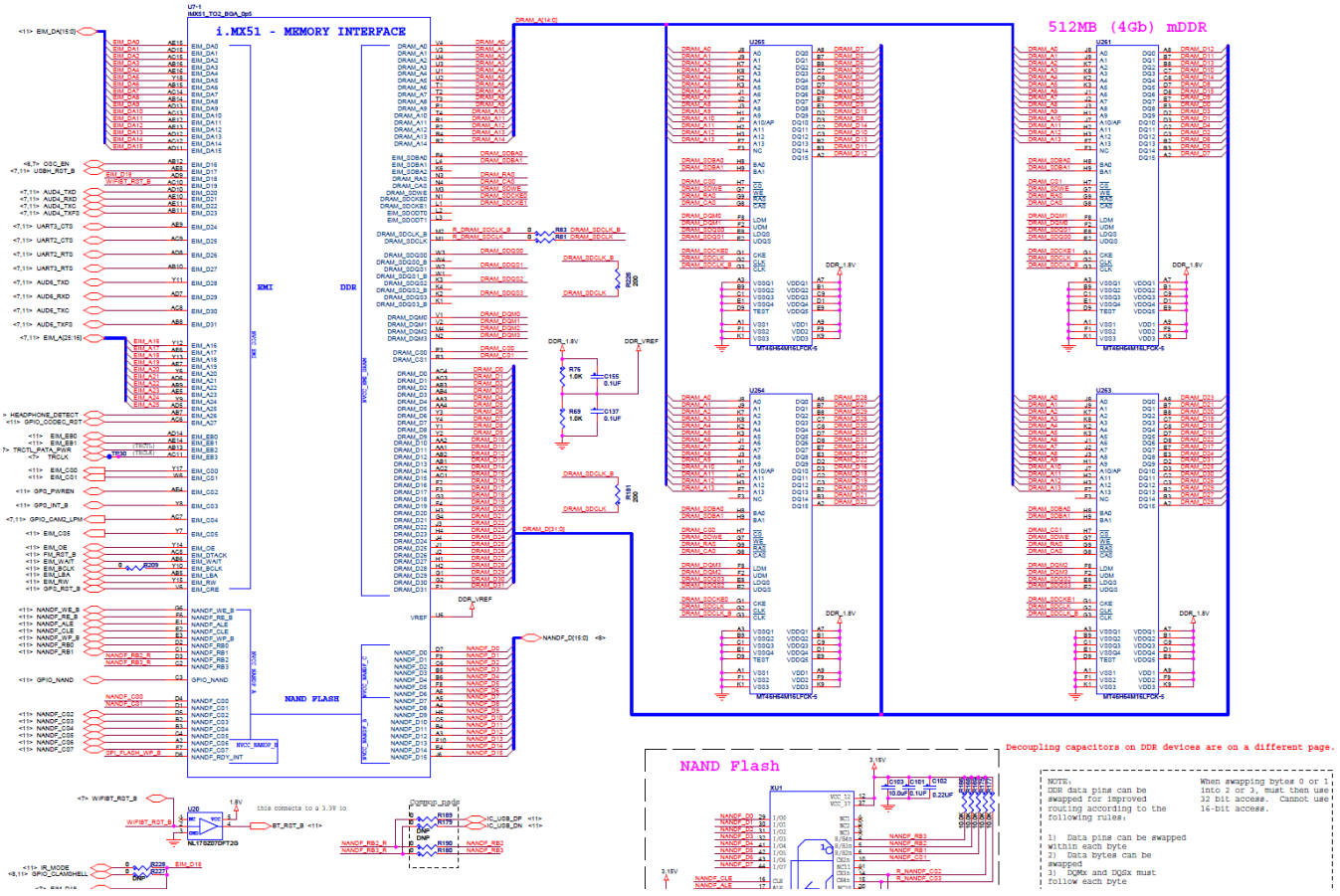

Figure 2. mDDR Memory Interfacing

2.2 DDR2 Interfacing

Figure 3 shows the interfacing between the i.MX51 and DDR2. The DDR2 device used in Figure 3 is the EDE1116AEBG.

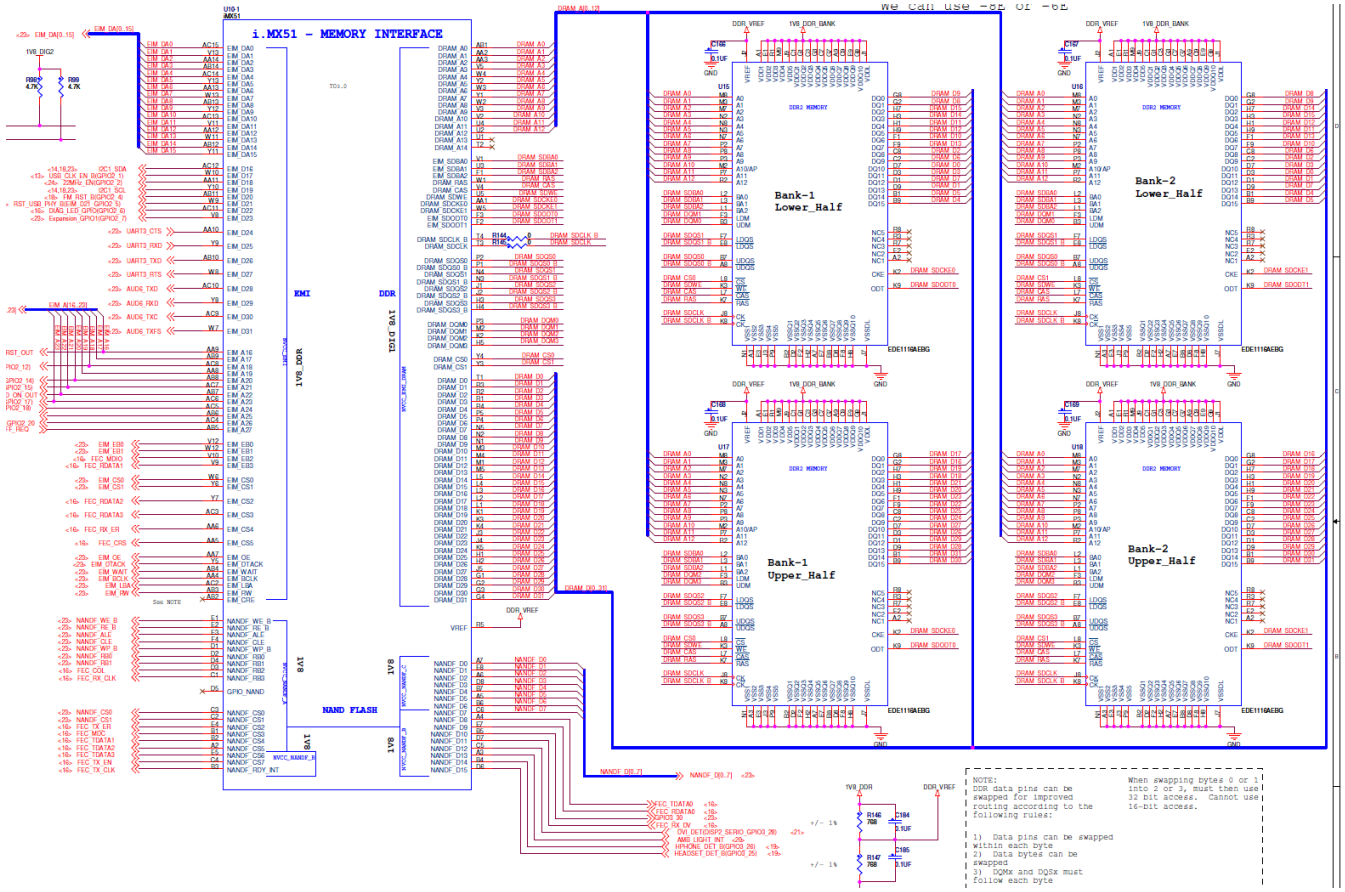

Figure 3. DDR2 Memory Interfacing

The differences between the mDDR and DDR2 memories are as follows:

- The mDDR memories do not have the ODT and VREF signals, unlike the DDR2.
- The DQS signals are routed as differential pairs in DDR2 memories, unlike the mDDR.

NOTE

VREF is used as a reference voltage when ddr_input mode is enabled (non-CMOS mode) for DDR2 I/O. This mode is commonly used for DDR2 memories, especially if ODT (on-die termination) is enabled. For mDDR memories, typically CMOS mode is used and VREF is grounded. However, in some cases (due to board design, routing) non-CMOS mode may provide better performance. Therefore, making provision for VREF options allows flexibility.

3 DDR2 JTAG Script Configuration

The following code configures the DDR2 memory to interface with the i.MX51:

```
//*============================================================================================
//* Copyright (C) 2007, Freescale Semiconductor, Inc. All Rights Reserved
//* THIS SOURCE CODE IS CONFIDENTIAL AND PROPRIETARY AND MAY NOT
//* BE USED OR DISTRIBUTED WITHOUT THE WRITTEN PERMISSION OF
//* Freescale Semiconductor, Inc.
//*============================================================================================
// Initialization script for Elvis EVB
//*============================================================================================
// Revision History:
//                              Modification     Tracking
// Author (core ID)              Date D/M/Y       Number    Description of Changes
// -------------------------   ------------    ----------  ------------------------------------
//                              20-June-2007                 Creation of the file.
//                                           26-Mar-2008         Taken from Marley, changed for
Elvis
//*============================================================================================

wait = on

//*============================================================================================
// init ARM
//*============================================================================================
setreg @CP15_CONTROL=0x00050078
setreg @CPSR=0x1D3

// Setup PLL's
setmem /32 0x83F80004 =0x00000000
setmem /32 0x83F84004 =0x00000000
setmem /32 0x83F88004 =0x00000000

setmem /32 0x83F80000 =0x00001222
setmem /32 0x83F80008 =0x00000070
setmem /32 0x83F8000C =23
setmem /32 0x83F80010 =7

setmem /32 0x83F88000 =0x00000222
setmem /32 0x83F88008 =0x00000091
setmem /32 0x83F8800C =0x00000000
setmem /32 0x83F88010 =0x00000000
// Switch ARM to PLL 3
setmem /32 0x73FD400C =0x00000180
setmem /32 0x73FD400C =0x00000184
setmem /32 0x83F80000 =0x00001232
pause 2
// Switch ARM back to PLL 1
setmem /32 0x73FD400C =0x00000180
setmem /32 0x73FD400C =0x00000000

// Restart PLL 3
setmem /32 0x83F88000 =0x00000232
pause 1

setmem /32 0x83F80004 =0x00000002
```

```
setmem /32 0x83F88004 =0x00000002

// Set the CCM registers
setmem /32 0x73fd4014 = 0x19239100
setmem /32 0x73fd4018 = 0x000020C2
setmem /32 0x73fd401C = 0xA5A2A020
setmem /32 0x73fd4024 = 0x00C30321
setmem /32 0x73fd4060 = 0x010900F0
setmem /32 0x73fa83F4 = 0x00000004
setmem /32 0x73fa83F0 = 0x00000004

//*==========================================================================================
// Initialization script for 32 bit DDR2 (CS0+CS1)
// Starting DDR frequency (after ROM code execution, before "prog_pll") is 150MHz
// Using validation environment (incl. "prog_pll" routine) will set DDR clock to 200MHz
//*==========================================================================================

// DDR2 IOMUX configuration
setmem /32 0x73fa88a0 = 0x00000200 //IOMUXC_SW_PAD_CTL_GRP_INMODE1          DDR2 mode
setmem /32 0x73fa850c = 0x000020c5 //IOMUXC_SW_PAD_CTL_PAD_EIM_SDODT1       Pull-D, HIGH DS
setmem /32 0x73fa8510 = 0x000020c5 //IOMUXC_SW_PAD_CTL_PAD_EIM_SDODT0       Pull-D, HIGH DS
setmem /32 0x73fa883c = 0x00000002 //IOMUXC_SW_PAD_CTL_GRP_DDR_A0           MEDIUM DS
setmem /32 0x73fa8848 = 0x00000002 //IOMUXC_SW_PAD_CTL_GRP_DDR_A1           MEDIUM DS
setmem /32 0x73fa84b8 = 0x000000e7 //IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCLK       MAX DS
setmem /32 0x73fa84bc = 0x00000045 //IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS0       Pull/Keep Disable
setmem /32 0x73fa84c0 = 0x00000045 //IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS1       Pull/Keep Disable
setmem /32 0x73fa84c4 = 0x00000045 //IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS2       Pull/Keep Disable
setmem /32 0x73fa84c8 = 0x00000045 //IOMUXC_SW_PAD_CTL_PAD_DRAM_SDQS3       Pull/Keep Disable
setmem /32 0x73fa8820 = 0x00000000 //IOMUXC_SW_PAD_CTL_GRP_DDRPKS           PUE = Keeper
setmem /32 0x73fa84a4 = 0x00000003 //IOMUXC_SW_PAD_CTL_PAD_DRAM_RAS         MEDIUM DS
setmem /32 0x73fa84a8 = 0x00000003 //IOMUXC_SW_PAD_CTL_PAD_DRAM_CAS         MEDIUM DS
setmem /32 0x73fa84ac = 0x000000e3 //IOMUXC_SW_PAD_CTL_PAD_DRAM_SDWE        MEDIUM DS
setmem /32 0x73fa84b0 = 0x000000e3 //IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCKE0      MEDIUM DS
setmem /32 0x73fa84b4 = 0x000000e3 //IOMUXC_SW_PAD_CTL_PAD_DRAM_SDCKE1      MEDIUM DS
setmem /32 0x73fa84cc = 0x000000e3 //IOMUXC_SW_PAD_CTL_PAD_DRAM_CS0         MEDIUM DS
setmem /32 0x73fa84d0 = 0x000000e2 //IOMUXC_SW_PAD_CTL_PAD_DRAM_CS1         MEDIUM DS

setmem /32 0x73FA882C = 0x4// DRAM_D31-24 to high
setmem /32 0x73FA88a4 = 0x4// DRAM_D0-7 to high
setmem /32 0x73FA88aC = 0x4// DRAM_D8-15 to high
setmem /32 0x73FA88b8 = 0x4// DRAM_D16-23 to high

//13 ROW, 10 COL, 32Bit, SREF=4 Micron Model
//CAS=3,  BL=4
setmem /32 0x83fd9000 = 0x82a20000 // ESDCTL0
setmem /32 0x83fd9008 = 0x82a20000 // ESDCTL1

setmem /32 0x83fd9010 = 0x000ad0d0 // ESDMISC

setmem /32 0x83fd9004 = 0x3F3584AB // ESDCFG0
setmem /32 0x83fd900c = 0x3F3584AB // ESDCFG1

// Init DRAM on CS0
setmem /32 0x83fd9014 = 0x04008008 // ESDSCR
setmem /32 0x83fd9014 = 0x0000801a // ESDSCR
setmem /32 0x83fd9014 = 0x0000801b // ESDSCR
setmem /32 0x83fd9014 = 0x00448019 // ESDSCR
```

```
setmem /32 0x83fd9014 = 0x07328018 // ESDSCR
setmem /32 0x83fd9014 = 0x04008008 // ESDSCR
setmem /32 0x83fd9014 = 0x00008010 // ESDSCR
setmem /32 0x83fd9014 = 0x00008010 // ESDSCR
setmem /32 0x83fd9014 = 0x06328018 // ESDSCR
setmem /32 0x83fd9014 = 0x03808019 // ESDSCR
setmem /32 0x83fd9014 = 0x00408019 // ESDSCR  ODT=150Ohm,CS0
setmem /32 0x83fd9014 = 0x00008000 // ESDSCR

// Init DRAM on CS1
setmem /32 0x83fd9014 = 0x0400800c // ESDSCR
setmem /32 0x83fd9014 = 0x0000801e // ESDSCR
setmem /32 0x83fd9014 = 0x0000801f // ESDSCR
setmem /32 0x83fd9014 = 0x0000801d // ESDSCR
setmem /32 0x83fd9014 = 0x0732801c // ESDSCR
setmem /32 0x83fd9014 = 0x0400800c // ESDSCR
setmem /32 0x83fd9014 = 0x00008014 // ESDSCR
setmem /32 0x83fd9014 = 0x00008014 // ESDSCR
setmem /32 0x83fd9014 = 0x0632801c // ESDSCR
setmem /32 0x83fd9014 = 0x0380801d // ESDSCR
setmem /32 0x83fd9014 = 0x0040801d // ESDSCR  ODT=150Ohm,CS0
setmem /32 0x83fd9014 = 0x00008004 // ESDSCR

setmem /32 0x83fd9000 = 0xb2a20000 // ESDCTL0
setmem /32 0x83fd9008 = 0xb2a20000 // ESDCTL1

setmem /32 0x83fd9010 = 0x000ad6d0 // ESDMISC RALAT=01, NO ODT

setmem /32 0x83fd9034 = 0x90000000 // ESDCDLYGD

setmem /32 0x83fd9014 = 0x00000000 // ESDSCR - clear "configuration request" bit


readfile,raw,gui "X:\redboot\diag-ecos-rel\REDBOOT\bin\mx51_babbage_redboot.bin"=0xAFF00000
setreg @R15=0xAFF00000
```

4 mDDR and DDR2 Routing Rules

The routing is one of the critical procedures while interfacing. The guidelines for the routing are restrictive, and the difficulty to meet the routing guidelines depend on the stackup. However, the routing helps the design to become better and more robust.

The DDR routing is done in two ways:

- Routing all the signals at the same length
- Routing by byte-group

The two routing methods are described as follows:

- Routing all the signals at the same length is a difficult method. However, it is the better way, as it helps easy analysis.

Table 1 gives the specifications for routing the signals at the same length.

Table 1. Specifications for Routing Signals at the Same Length

Signals	Lengths	Considerations
Address and Bank	≤ Clock length	Match the signals ±25 mils
Data and Buffer	≤ Clock length	
Control signals	≤ Clock length	
Clock	≤ Lcritical (3 inches)	Match the signals with the clock signals ±5 mils
DQS and DQS_B	≤ Clock length	Match the signals with the DQS signals ±10 mils

- Routing by byte-group requires a better control of the signals of each group and is more difficult for analysis and constraints settings.

  Table 2 gives the specifications for routing by byte-group.

Table 2. Specifications for Routing by Byte-Group

Signals	Length	Considerations
Address and Bank	(Clock length - 200 mils) ≤ Address and Bank length ≤ Clock length	Match the signals ±25 mils
Byte group 1 DQ0—DQ7, DQS0, DQM0	The max byte group 1 length ≤ Clock length	Match the signals of each byte group ±25 mils
Byte group 2 DQ8—DQ15, DQS1, DQM1	The max byte group 2 length ≤ Clock length	The difference between the byte-groups should be ±50 mils. Match the signals with the DQS signals ±10 mils. (Clock length - 500 mils) ≤ DQS Signals Length ≤ Clock length
Byte group 3 DQ16—DQ23, DQS2, DQM2	The max byte group 3 length ≤ Clock length	
Byte group 4 DQ24—DQ31, DQS3, DQM3	The max byte group 4 length ≤ Clock length	
Control signals	(Clock length - 200 mils) ≤ Control length ≤ Clock length	Match the signals ±50 mils
Clock	≤ Lcritical (3 inches)	Match the signals with the clock signals ± 5 mils

NOTE

The impedance for the signals should be 50 Ω for singled ended and 100 Ω for differential pairs.

5 Routing on i.MX51 EVK

This section describes the EVK implementation for routing the DDR2 memories.

The Figure 4 shows the placement of the i.MX51 in the EVK board. This procedure should be followed to have the memories close to the i.MX51 and for a better control of the signal length.

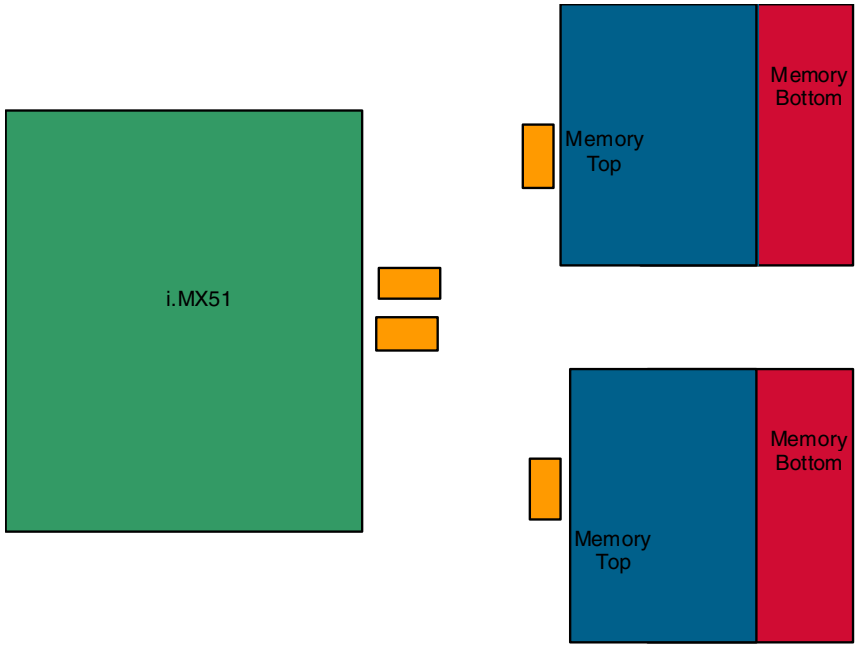

Figure 4. DDR2 Memories and i.MX51 Placement

Figure 5 and Figure 6 show the different ways to route the DDR signals in point to point connection. This type of connection reduces the number of vias and allows routing without layer transitions.

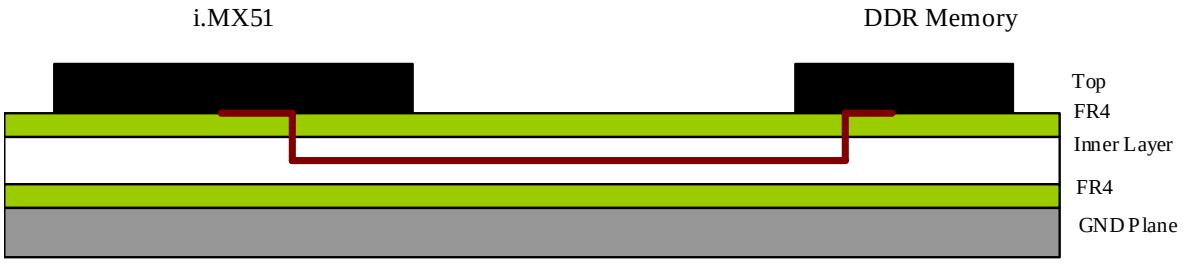

Figure 5. Point to Point Connection

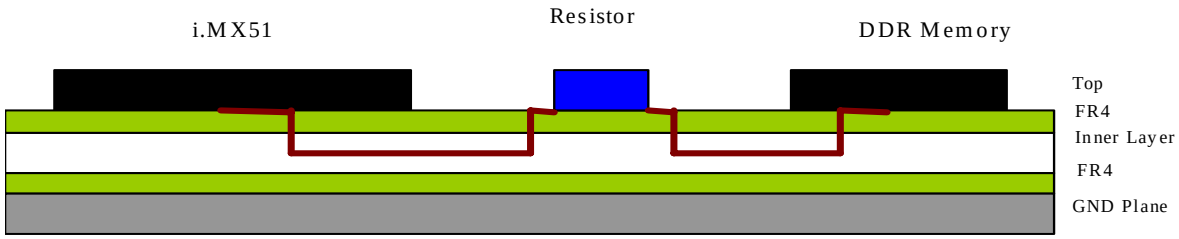

Figure 6. Point to Point Connection Including the Series Resistor

The stackups used for this type of design are as follows:

- 8 layers
  - L1—top signal
  - L2—GND plane
  - L3—internal signal 1
  - L4—PWR plane
  - L5—PWR plane
  - L6—internal signal 2
  - L7—GND plane
  - L8—bottom signal
- 6 layers
  - L1—top signal/power
  - L2—GND plane
  - L3—internal signal 1/power
  - L4—internal signal 2/power
  - L5—GND plane
  - L6—bottom signal/power

Figure 7, Figure 8, Figure 9, Figure 10, and Figure 11, give an example for routing DDR2 memories. This example in effect is the guidelines for layer routing.

- Figure 7 shows the top DDR2 routing.

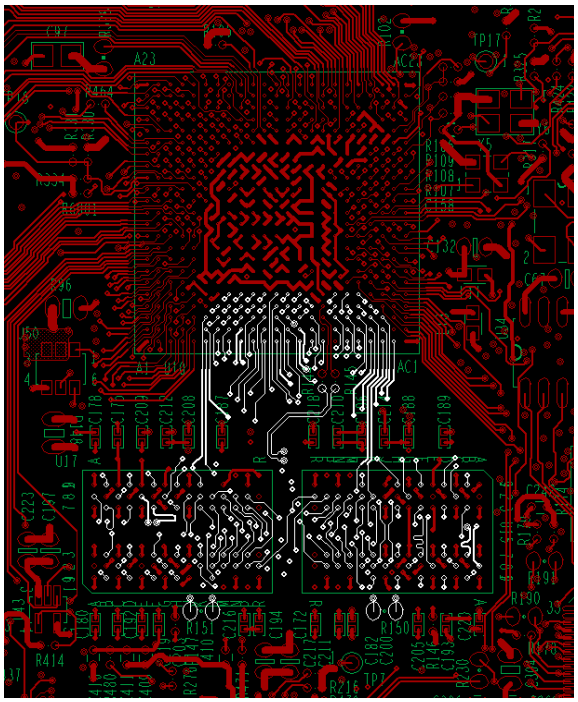

Figure 7. Top DDR2 Routing

- Figure 8 shows the internal 1 DDR2 routing.

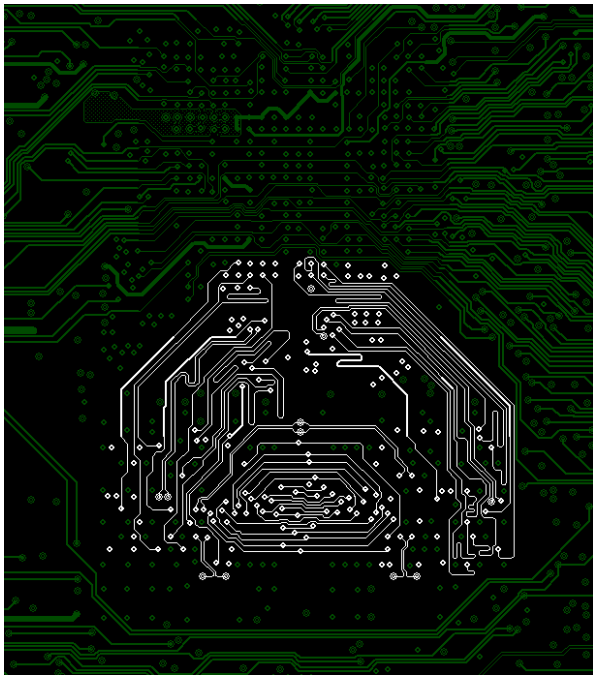

Figure 8. Internal 1 DDR2 Routing

- Figure 9 shows the power 1 DDR2 routing.

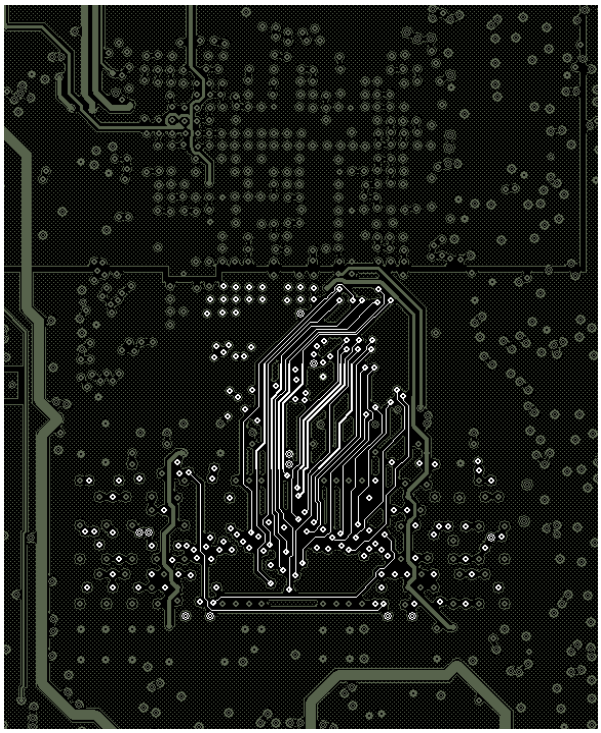

Figure 9. Power 1 DDR2 Routing

- Figure 10 shows the internal 2 DDR2 routing.

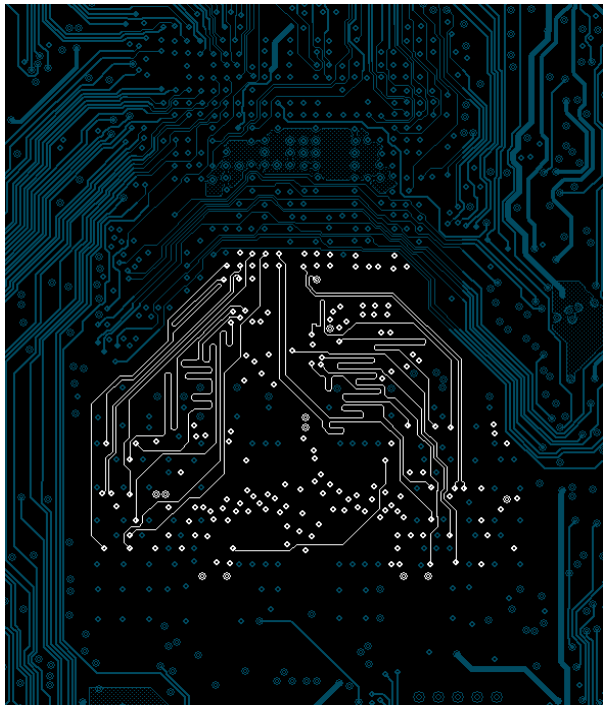

Figure 10. Internal 2 DDR2 Routing

- Figure 11 shows the bottom DDR2 routing.

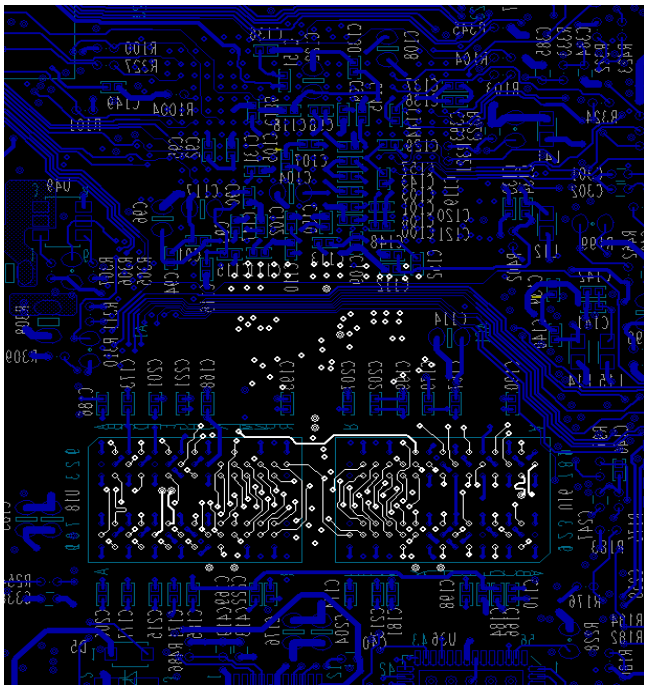

Figure 11. Bottom DDR2 Routing

Table 3 gives the total etch of the signals for the byte 0 and byte 1 groups.

Table 3. Etch for DDR2 Routing

Signals	Length (mils)
DRAM_D0	1141.69
DRAM_D1	1151.25
DRAM_D2	1156.71
DRAM_D3	1057.88
DRAM_D4	1155.42
DRAM_D5	1152.43
DRAM_D6	1159.87
DRAM_D7	1182.69
DRAM_DQM0	1138.23
DRAM_SDQS0	1156.36
DRAM_SDQS0_B	1192.52
DRAM_D8	1037.69
DRAM_D9	1039.47
DRAM_D10	1046.71
DRAM_D11	1038.47
DRAM_D12	1039.58
DRAM_D13	1132.83
DRAM_D14	1057.36
DRAM_D15	1056.28
DRAM_DQM1	10.41.13
DRAM_SDQS1	1046.25
DRAM_SDQS1_B	1045.87
DRAM_SDCLK	1249.02
DRAM_SDCLK_B	1295.91

6 Guidelines for 13 x 13 mm Package

The 13 × 13 mm package has 0.5 mm pitch. So, it is necessary to use the via across the pad and different types of vias, such as buried, blind or stacked.

The design considerations are given as follows:

- Blind via—10 mils pad and 4 mils drill from the top to the internal layer
- Ball Grid Array (BGA) spacing—3.34 mils gap, 3 mils width, and 3.34 mils gap
- Trace width for DDR routing—3 mils

- Stackup for the 10 layers are given as follows:
  - L1—top signal
  - L2—GND plane
  - L3—internal signal 1
  - L4—GND plane
  - L5—power plane
  - L6—power plane
  - L7—GND plane
  - L8—internal signal 2
  - L9—GND plane
  - L10—bottom signal

The strategy to route the mDDR interface are given as follows:

- Use the top side to route in the horizontal way
- Only the two columns of pins, near to the edge of the IC should be routed on the top
- The internal signal 1 and internal signal 2 should be used for DDR routing in horizontal ways and vertical ways, respectively
- Bottom layer should be used for vertical memory connections

Figure 12, Figure 13, Figure 14, and Figure 15 give an example for routing mDDR memories. This example in effect is the guidelines for layer routing.

- Figure 12 shows top DDR routing.

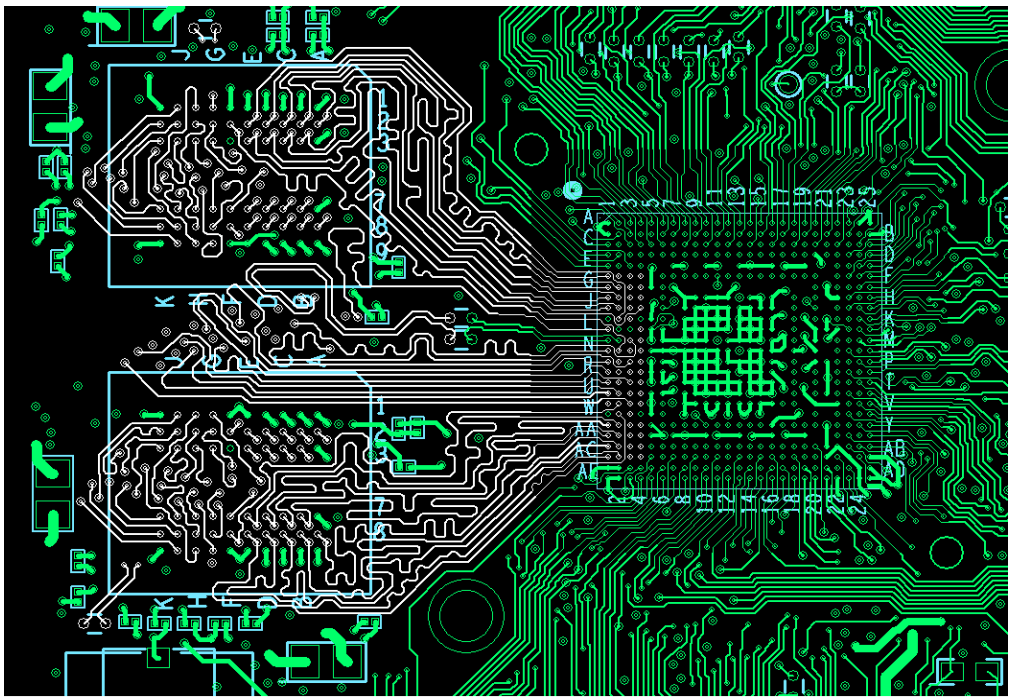

Figure 12. Top DDR Routing

- Figure 13 shows top internal signal 1 routing.

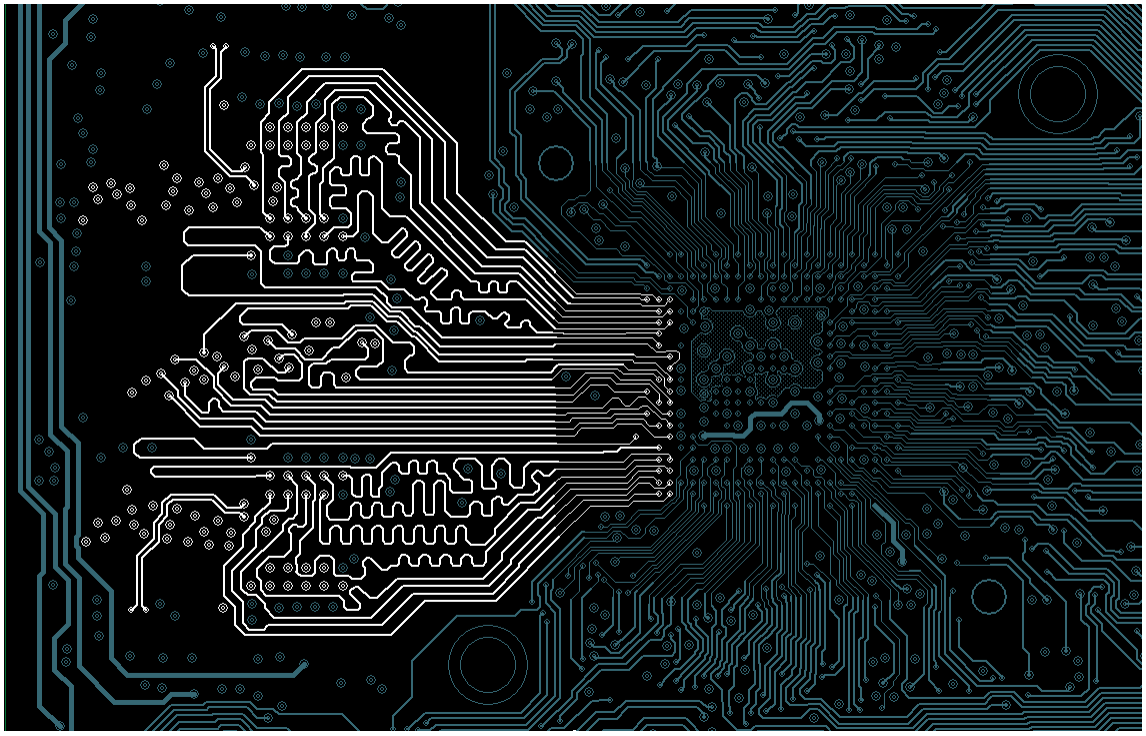

Figure 13. Internal Signal 1 Routing

- Figure 14 shows internal signal 2 routing.

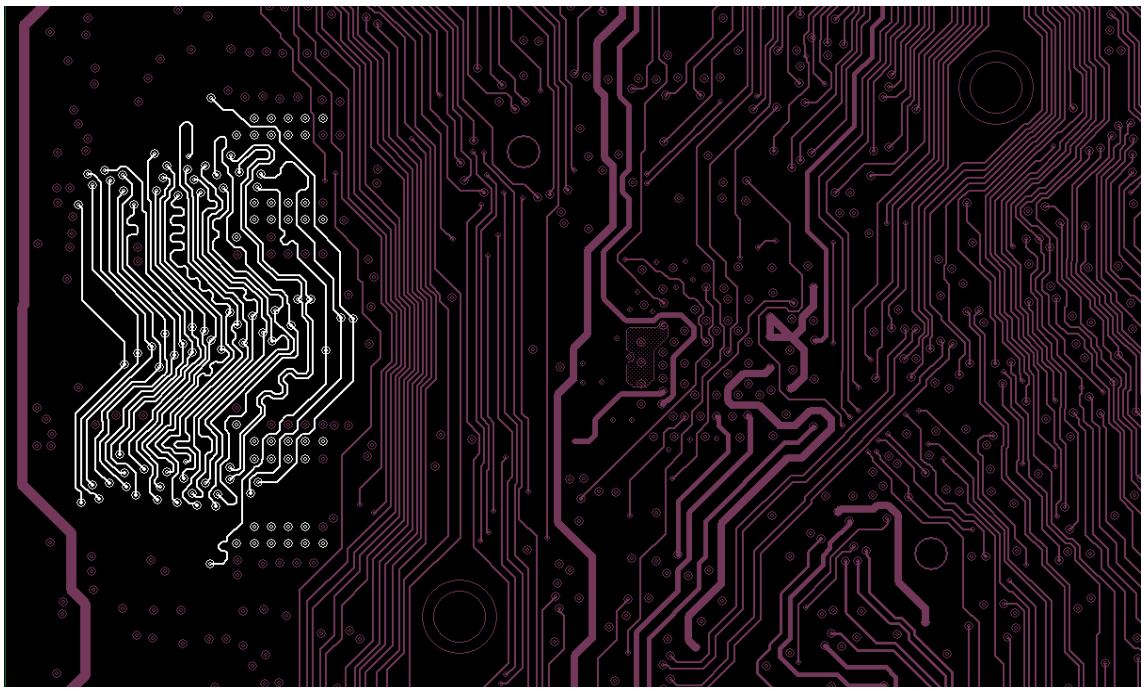

Figure 14. Internal Signal 2 Routing

- Figure 15 shows bottom DDR routing.

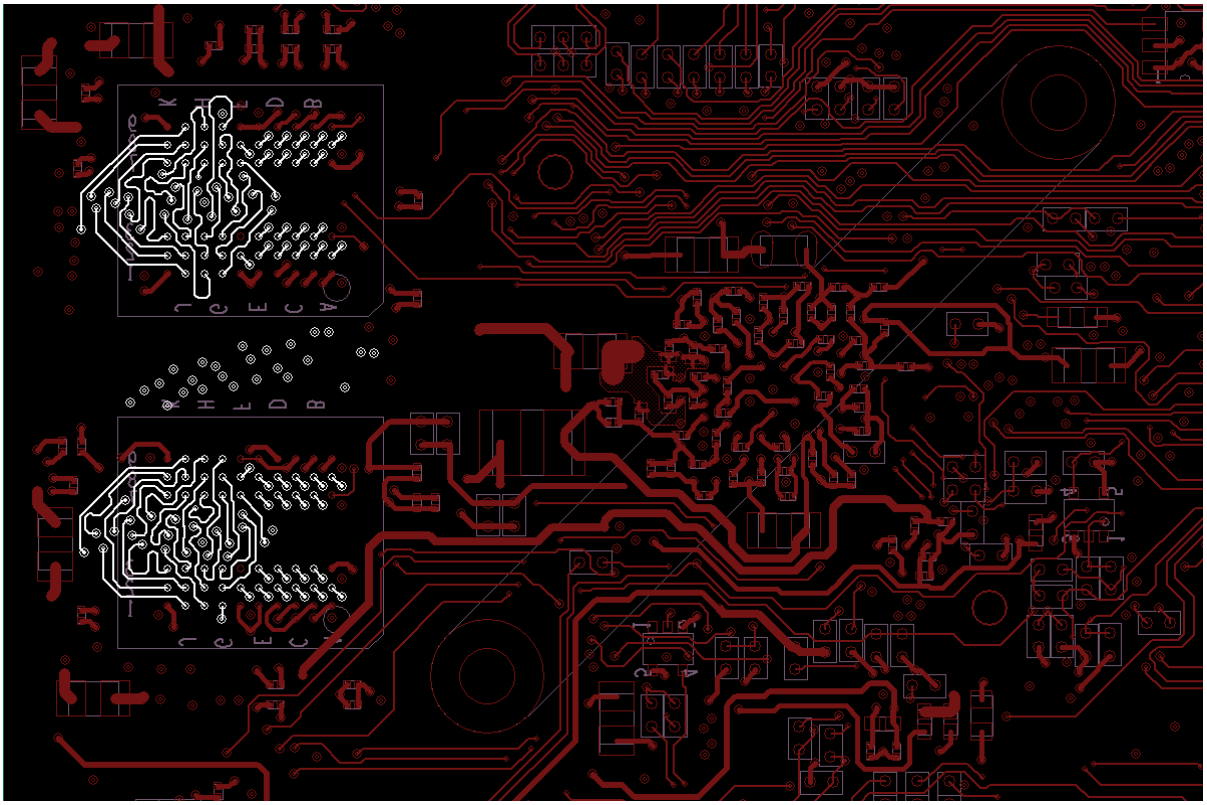

Figure 15. Bottom DDR Routing

Table 4 shows the total etch of the signals for the byte 0 and byte 1 groups.

Table 4. Etch for Byte 0 and Byte 1 Groups

Signals	Length (mils)
DRAM_D0	1170.21
DRAM_D1	1151.90
DRAM_D2	1152.96
DRAM_D3	1161.40
DRAM_D4	1149.45
DRAM_D5	1151.89
DRAM_D6	1168.71
DRAM_D7	1150.21
DRAM_SDQS0	1150.74
DRAM_DQM0	1150.05
DRAM_D8	1168.12
DRAM_D9	1152.29

Table 4. Etch for Byte 0 and Byte 1 Groups (continued)

Signals	Length (mils)
DRAM_D10	1149.49
DRAM_D11	1153.24
DRAM_D12	1149.34
DRAM_D13	1151.75
DRAM_D14	1156.11
DRAM_D15	1150.63
DRAM_SDQS1	1166.04
DRAM_DQM1	1171.87
DRAM_SDCLK	2217.78
DRAM_SDCLK_B	2190.78

7 Revision History

Table 5 provides a revision history for this application note.

Table 5. Document Revision History

Rev. Number	Date	Substantive Change(s)
2	10/2010	Added a note in Section 2.2, “DDR2 Interfacing.”
1	06/2010	In Table 2, changed the clock length: • 200 to 200 mils • 500 to 500 mils
0	04/2010	Initial release.

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Document Number: AN4054
Rev. 2
10/2010