MPC57xx Nexus Debug Connectors

Including the Nexus Aurora Interface for the Automotive MCU Power Architecture

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Contents

1   Introduction

The MPC5744P is the first automotive microcontroller in the MPC57xx family that implements a Nexus high-speed serial[1] (Aurora) trace Auxiliary Output port (AUX) on the production device, in addition to the traditional Nexus parallel Auxiliary Port. The IEEE-ISTO 5001™-2012 standard defines the methodology for embedding the Nexus messages in the Xilinx Aurora protocol transport layer. Additionally, it supports a JTAG run control based either the IEEE 1149.1. Many devices in the MPC57xx family of devices also support the IEEE 1149.7 interface for run control and device access.

The Nexus parallel Auxiliary port on the MPC5744P is the same as implemented on previous MPC5500 and MPC5600 families of devices. The Aurora based serial Auxiliary port is new. It consists of the serial Aux physical interfaces and consists of two[2] LVDS,[3] lanes. To minimize the cost impact of the Nexus Aurora trace port, an external LVDS clock, running at the desired trace frequency, is required to be provided by the tool. (This prevents the requirement to instantiate a dedicated, precision Phase Lock Loop (PLL) in the device to support the trace functions.) Trace clock frequencies between 625 MHz and 1.25 GHz are supported.

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1. The high-speed serial trace port (HSST) is sometimes referenced as the high-bandwidth debug port (HBDP).
2. Four lanes are supported on some devices.
3. Low Voltage Differential Signal.

This application note defines the pin-out definition of the generic Nexus High-speed Serial (Aurora) connector for all of the MPC57xx family devices that support the Nexus high-speed serial (Aurora[4]) trace port. This application note also includes the recommended updated pin-out of a JTAG only connector (backwards compatible). See AN2614 "MPC553x, MPC555x, and MPC556x Family Nexus Interface Connector" and AN3968 "Nexus Interface Connector for the MPC567xF and MPC5676R Families" for connector definitions for devices that support the parallel Nexus Auxiliary (trace) Port.

The following table shows the current (announced) MPC57xx devices and the type of Nexus trace (parallel or serial) that they support. It also shows the width of the trace ports (number of parallel Message Data Outputs [MDO] or the number of serial lanes). Current MPC57xx serial Nexus trace interfaces encode an internal 30-bit MDO (plus 2 Message Start/End Outputs [$\overline{\text{MSEO}}$]) into either 2- or 4-lanes of Aurora data.

Table 1.   MPC57xx family trace support summary

Device	IEEE 1149.7 support	Nexus parallel trace[1]	Nexus serial (Aurora) trace[2]	Nexus trace to memory[3]	Highest Nexus class support[4]
MPC5744P	No	Yes / 4[5]	Yes / 2[6]	No	Class 3+
MPC5746R	Yes	No	No	Yes / 16 KB	Class 3+
MPC5746R emulation device	Yes	No	Yes/4	Yes / 1 MB	Class 3+
MPC574xG/MPC574xC	Yes	Yes[7] / 12 or 16	No	No	Class 3+
MPC577xK	Yes	No[8] / 16	Yes / 4	No	Class 3+
MPC5777C	Yes	Yes / 12 or 16	No	No	Class 3+
MPC5777M	Yes	No	No	Yes / 16 KB	Class 3+
MPC5777M emulation device	Yes	No	Yes / 4	Yes / 2 MB	Class 3+

1. Number of (parallel) Message Data Outputs is shown if supported.
2. Maximum number of Aurora lanes is shown, if supported. Devices that support 4-lanes also support 2-lane operation.
3. Maximum trace memory. This memory can be split between trace use and overlay use.
4. For some devices, all Nexus clients may not implement the full Nexus Class 3+ features. Some clients may only support Class 1 or Class 2+. See the complete device documentation for the Nexus class supported for each of the clients. In this table, if Class 3+ is listed, then at least one Nexus client supports Nexus Class 3+ features.
5. Available in all packages.
6. 257 MAPBGA package only
7. 324 MAPBGA package only
8. Internally, 16 parallel Nexus Message Data Outputs are available, however, these signals are not available in the standard 356 Molded Array Process Ball Grid Array (MAPBGA) device package.

2   Debug overview

The MPC5744P implements multiple sets and types of the Nexus interface signals. It supports both the traditional IEEE-ISTO 5001™ standard parallel trace Auxiliary Port, as well as the newly added (in the IEEE-ISTO 5001-2012 version of the standard) high speed serial Nexus trace Auxiliary Port that utilizes the Xilinx® Aurora physical interface. The Aurora interface allows the Nexus protocol information (Message Data Outputs and Message Start/End Outputs) to be transmitted serially at a high rate of speed over one or more Aurora lanes[5]. The Aurora protocol handles the encoding of the data and stripes the information across the number of lanes available on the device.

The MPC5744P supports the Nexus traditional parallel trace Auxiliary port with four Message Data outputs, similar to the previous MPC5643L. For more information on the parallel implementation and connector, see AN3968 "Nexus Interface Connector for the MPC5674F" and AN2614 "MPC553x,MPC555x, and MPC556x Family Nexus Interface Connector." The

4. Aurora is a transport protocol defined by Xilinx®.
5. The Freescale MPC57xx Automotive MCUs support either two or four lanes of Nexus Aurora data.

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257 MAPBGA version of the MPC5744P evaluation board (EVB) supports the Mictor parallel Nexus connector, as well as the Samtec high speed serial connector (HS34). The MPC5744P only supports 2 high-speed Aurora lanes, however, other devices in the family may support four (4) lanes.

The table below shows number of trace signals available with the different options available.

Table 2. MPC57xx Debug and trace interfaces

Name	Signals used	Data rate
Nexus Parallel Interface[1]	Parallel 4 to 16-bit MDO port with two $\overline{MSEO}$ and clock	80 MHz maximum frequency with up to 16 MDO pins
Nexus Aurora Serial narrow interface	Aurora Serial Two (2) transmit lanes	1.2 GHz signaling rate times 2
Nexus Aurora Serial wide interface	Aurora Serial Four (4) transmit lanes	1.2 GHz signaling rate times 4

1. On some devices, two port sizes are supported, a "reduced" port size and a "full" port size. Devices that support both parallel and serial Nexus ports implement a single parallel port with, along with the serial port. The port size field (reduced/full) selects between the parallel (reduced) or serial (full) port.

The figure below shows a Nexus view of the MPC5744P device from the pins down through the Nexus clients to the cores and peripherals.
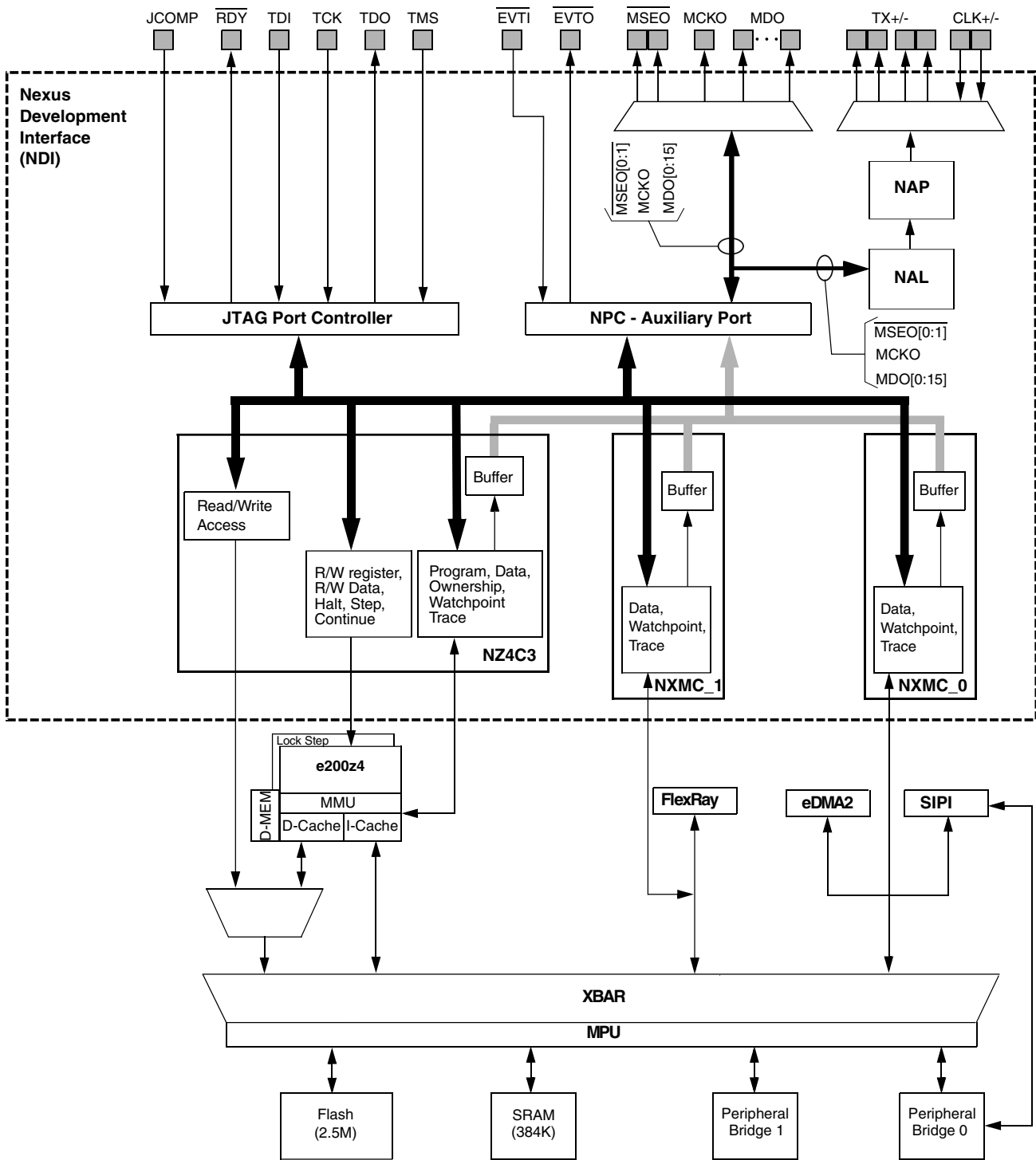
Figure 1. MPC5744P Nexus block diagram

The Nexus Development Interface consists of two major functions that are defined by the Nexus IEEE-ISTO 5001-2012 standard, run-control and trace. Run-control is handled by the JTAG controller that handles the IEEE-1149.1 functions, although many devices also include an optional IEEE-1149.7 interface that can be enabled as a front-end to the JTAG controller. The trace aspect of debug is handled via the Nexus Auxiliary Port. The MPC5744P supports the traditional (IEEE-ISTO 5001-2003) parallel Auxiliary port, or the newly defined (in the IEEE-ISTO 5001-2012 standard) Nexus serial Aurora-based serial trace.

3 Recommended debug connectors and connector pin out definitions

The following table shows the recommended connectors for different applications.

Table 3. Recommended connectors

Connector style	Target system part number	Connector type
14-pin BERG JTAG only	3M 2514–6002UB	JTAG-only configuration[1]
17-position (2 × 17, 34-pin) Samtec	Samtec ASP–137973–01	Serial Nexus configuration (supports up to 8 simplex lanes; fewer lanes are available if duplex support or LFAST support is required)
25-position (2 × 25, 50-pin) Samtec	Samtec ASP–148422–01	Parallel Nexus Configuration (up to 16 MDO signals)[2]
38-pin MICTOR[3]	Tyco 767054-1[4]	Parallel Nexus Configuration (up to 12 MDO signals)[5]

1. The existing MPC5500 and MPC5600 JTAG connector is being reused on the MPC57xx devices with an additional optional signal.
2. For new designs that require 12 or 16 MDO signals, the Samtec connector is highly recommended. It can optionally still be used for fewer MDO signals as well.
3. Recommended for backward compatibility only. Not recommended for 16-bit MDO support. The Lauterbach LA-7631 Mictor adapter has four solder pad options for connecting MDO[12:15]. Older interfaces do not support the 16-bit wide mode.
4. Other compatible part numbers are 2-5767004-2 (RoHS compliant), 2-767004-2, 767061-1, and 767044-1.
5. Although this connector can be used for 16 MDO signals, it is not recommended.

NOTE

Whichever connector is chosen, "keep-out" areas may be required by some tools. Consult the preferred tool vendor to determine any area that must remain clear around the debug connector. Some tool vendors may include an extension cable to minimize "keep-out" areas, but use of an extension will degrade the signal. In many cases, this degradation will be insignificant, but it depends on many factors including clock frequency and target board layout.

4 MPC57xx high-speed serial trace connector

For high speed Nexus Aurora trace applications, the Samtec ERF8 Series connector is recommended in the IEEE-ISTO 5001-2011 standard. For the MPC567xx family, the 17 position (34 pins) connector is recommended. The part numbers of the Samtec connectors are shown in the following table.

Table 4. Recommended high-speed serial trace connector part numbers

Connector	Part number (Samtec)	Style	Description
HS34	ASP-137973-01	Samtec ERF8 Series, 17 position by 2 row	Vertical mount for MCU module
HS34	ASP-177706-02	Samtec ERF8 Series, 17 position by 2 row	Right Angle mount for MCU module

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The Samtec ERF8 series of connectors is intended for high speed applications requiring a minimum footprint size with a reliable, latching connection. The recommended connector has two rows of seventeen contacts each with a spacing of 0.8 mm. The connector provides isolation between the high-speed trace signals and the low-speed JTAG and control signals. It also provides ample ground connections to ensure signal integrity.

If at all possible, the connector should be placed onto the target system with the even numbered pins nearest the edge of the printed circuit board.

In addition, care should be taken in the layout of the high speed Aurora signals (TXn+, TXn-, CLK+, and CLK-) with a good return path (usually ground)..
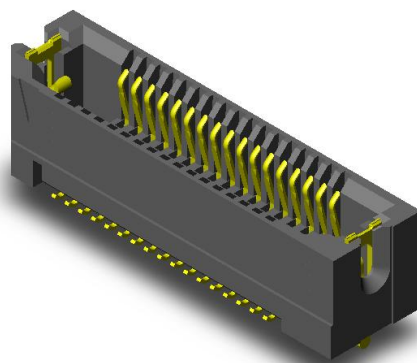
The following picture is courtesy of Samtec U.S.A (http://www.samtec.com/search/NEXUS.aspx).

Figure 2. HS34 (ASP-137973-01) connector

The following shows the recommended pin out for the Samtec connector.

Table 5.   Generic MPC57xx high-speed serial trace connector

Position	MPC57xx Signal	Direction	Pin number	Pin number	Direction[1]	MPC57xx Signal	IEEE-5001-2012 GEN_IO signal name
	GND					GND[2]	
1	TX0+	Out	1	2	Out[3]	VREF	
2	TX0-	Out	3	4	In	TCK/TCKC	
3	GND		5	6	In/Out	TMS/TMSC[4]	
4	TX1+	Out	7	8	In	TDI	
5	TX1-	Out	9	10	Out	TDO	
6	GND		11	12	In	JCOMP	$\overline{\text{TRST}}$
7	TX2+	Out	13	14	Out	$\overline{\text{EVTI1}}$[5]	GEN_IO0

Table continues on the next page...

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Table 5. Generic MPC57xx high-speed serial trace connector (continued)

Position	MPC57xx Signal	Direction	Pin number	Pin number	Direction[1]	MPC57xx Signal	IEEE-5001-2012 GEN_IO signal name
8	TX2-	Out	15	16	In	$\overline{\text{EVTI}}$(0)	
9	GND		17	18	Out	$\overline{\text{EVTO}}$(0)	
10	TX3+	Out	19	20	In/Out	$\overline{\text{RSTOUT}}$[6]	GEN_IO3
11	TX3-	Out	21	22	In/Out	$\overline{\text{RESET}}$[7]	$\overline{\text{RESET}}$
12	GND		23	24		GND	
13	TX4+	Out	25	26	In	CLK+	
14	TX4-[8]	Out	27	28	In[9]	CLK-	
15	GND		29	30		GND	
16	TX5+[8]	Out	31	32	Out	$\overline{\text{RDY}}$[10]	
17	TX5-[8]	Out	33	34	In/Out	WDT[11]	GEN_IO5
	GND[2]					GND[2]	

1. Viewed from the MCU.
2. The connector locking mechanism provides additional ground connections on each end of the connector.
3. This is an output from the connector standpoint. It may or may not be from the MCU.
4. TCKC and TMSC are the IEEE 1149.7 signals on devices that support that interface.
5. Not available on all devices. No connect if the device does not support the signal.
6. $\overline{\text{PORST}}$ on the MPC57xxM and ext_POR on the MPC5744P.
7. $\overline{\text{ESR0}}$ on the some devices
8. Reserved for TXn signals, not currently used.
9. Per the IEEE-ISTO 5001-2012, CLK+ and CLK- can either be outputs from the MCU or inputs to the MCU. For this family of devices, Freescale has defined this to be an input to the MCU. The tool must provide a LVDS clock at the desired Aurora transmission frequency from the MCU.
10. This pin can be used for $\overline{\text{EVTO1}}$ if $\overline{\text{RDY}}$ is not available.
11. WDT is an optional Watchdog Disable signal. It has no defined connection to the MCU. For systems that implement an external hardware watchdog circuit, this signal allows an external tool to disable that watchdog for debug purposes.

4.1 Nexus Aurora target system requirements

The Nexus Aurora interface requires termination and AC coupling of the signals between the target system and the tool. The termination resistor for the Aurora clock is located inside the MCU.

The transmit signals must be terminated, which is normally done inside the tool (sometimes inside the FPGA of the tool).

The following figure shows the typical circuit for the AC coupling capacitor and the termination resistors.
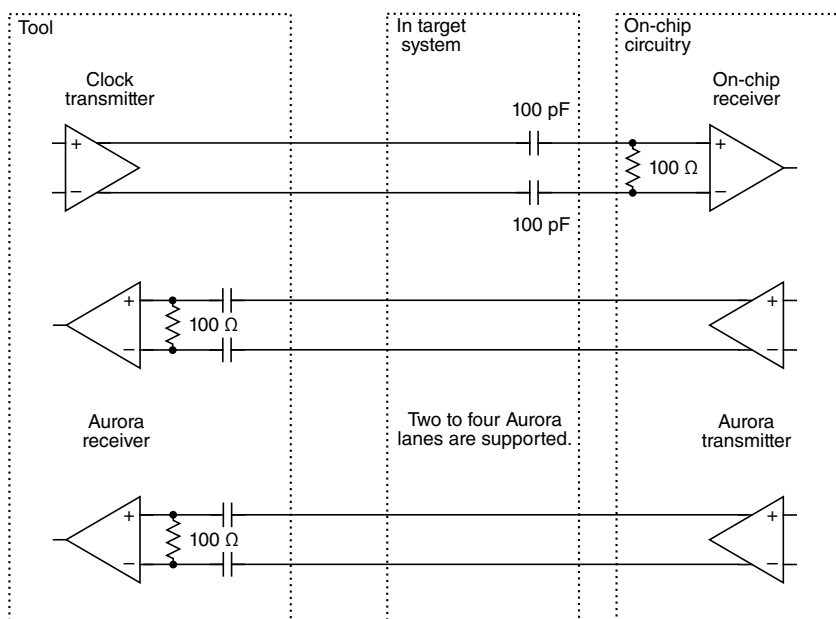
Figure 3. Nexus Aurora termination and coupling circuits

NOTE

It is recommended that the "even" side of the connector be mounted closer to the edge of the printed circuit board to facilitate a direct connection to the tool.

Due to the high speed nature of the Aurora signals, careful routing is required in an engine control module or other application board. The following guidelines will help in designing the PCB[6] :

* A controlled impedance PCB is required.
* The even side of the Samtec trace connector should be parallel to the edge of the board. The odd side of the Samtec connector should be nearest to the MCU. This allows a direct trace from the device to the connector for the high speed Aurora signals.
* The differential LVDS + and – pair should be routed close to, and parallel to, each other. The length of the + and - pairs should be matched to less than 0.05 inches of difference.
* The Nexus Aurora transmit pairs should be of the same approximate length (with a maximum different of 0.1 inches).
* The differential pair should be routed with a maximum of two vias. Ideally, the differential pair should be routed without vias on a single plane of the board (preferably on the top or bottom plane of the board). However, due to pin escape issues with the placement of the high speed signals on the surface mounted devices, routing on a single layer is not possible.
* Keep necking of the signal to less than 0.01 inch to avoid discontinuities. Some necking is usually required in escaping the signals for BGA or LQFP signal feeds to the other layers on the board.
* The differential pair must be routed on a layer that is one dielectric away from ground.
* Picket fence ground vias alongside the pair, spaced at 1/4 wavelength intervals may be required.
* Some tools may have a keep-out requirement. Check with the tool vendor for requirements.
* Use high quality high-speed connectors, such as the recommended SAMTEC connector, at the edge of the board.

4.2   MPC57xx JTAG signals

The following table shows the JTAG signals for the MPC57xx family of devices. This signal set encompasses both the IEEE 1149.1 and the IEEE 1149.7 JTAG standards.

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6.   Printed Circuit Board

Table 6. JTAG connector signal descriptions

IEEE 1149.1 JTAG signal	IEEE 1149.7 JTAG signal[2,1]	Description
TDO (Out)	TDOC (Out)	**JTAG Test Data Output (TDO)**. TDO provides the serial test data output for the on-chip test logic. This signal is not used in IEEE 1149.7 mode.
TDI (In)	TDIC[3] (In)	**JTAG Test Data Input (TDI)**. TDI provides the serial test instruction and data input for the on-chip test logic. This signal is not used in IEEE 1149.7 mode.
TCK (In)	TCKC (In)	**JTAG Test Clock Input (TCK)**. TCK is the clock input to the JTAG TAP controller and should be a maximum of one-fourth of the system clock frequency.
TMS (In)	TMSC (In/Out)	**JTAG Test Mode Select Input (TMS)**. TMS controls test mode operations for the on-chip test logic for boundary scan and debug access. TMSC is the bi-directional TM/TDI/TDO for the IEEE 1149.7 JTAG interface.
$\overline{\text{EVTI}}$ (In)	$\overline{\text{EVTI}}$[4] (In)	**Nexus Event In ($\overline{\text{EVTI}}$)**. After reset, the $\overline{\text{EVTI}}$ pin is used to initiate program and data trace synchronization messages or generate a breakpoint. If asserted during reset, upon negation of $\overline{\text{RESET}}$, the device will enter debug mode and not begin code execution. Some devices support multiple $\overline{\text{EVTI}}$ signals ($\overline{\text{EVTI0}}$ and $\overline{\text{EVTI1}}$) and also support $\overline{\text{EVTI}}$ pins to be configured ans $\overline{\text{EVTO}}$ (output) signals.
$\overline{\text{RDY}}$[4] (Out)	$\overline{\text{RDY}}$[4](Out)	**Nexus Ready Output ($\overline{\text{RDY}}$)**. $\overline{\text{RDY}}$ is an output that indicates to the development tools that the data is ready to be read from or written to the Nexus read/write access registers. On devices that do not support the $\overline{\text{RDY}}$ signal, $\overline{\text{EVTO}}$ can be placed on this pin of the connector for additional functionality.
$\overline{\text{RESET}}$ (In)	$\overline{\text{RESET}}$ (In)	**Reset ($\overline{\text{RESET}}$)**. This is the reset input to the microcontroller. It should be driven by tools to reset the microcontroller. It should be driven by an open drain device. The tool should also monitor this pin to determine if other devices have forced a reset to the microcontroller. It does not reset the JTAG state machine. This reset pin should NOT reset the internal debug blocks.
ext_POR or $\overline{\text{PORST}}$	ext_POR or $\overline{\text{PORST}}$	$\overline{\text{ext\_POR}}$ or $\overline{\text{PORST}}$. This is the power on reset to the microcontroller. Some devices name the pin $\overline{\text{PORST}}$ and some name it $\overline{\text{ext\_POR}}$. This reset clears the state of all registers and modes. It is always a destructive reset.
JCOMP (In)	JCOMP (In)	**JTAG TAP Controller Enable / JTAG Compliancy (JCOMP)**. JCOMP is used to enable the TAP controller for communication to the JTAG state machine for boundary scan and for debug access. A high on this pin enables the TAP controller.[5]
VREF	VREF	**Nexus VREF (VREF)**. Provides a reference for the signal levels of the Nexus device. All input high and low voltages should be referenced to this pin. The Nexus specification defines the input voltages as VIL = 0.3 × VREF and VIH = 0.7 × VREF. **NOTE:** This is a reference for the signal level and may not be the actual power supply for the debug pins. See the device definition for the debug pins in the device reference manual.
GND	GND	**Ground**. This is the negative reference (return) for the interface.

1. Some signals on the JTAG connector are IEEE-ISTO 5001-2012 signals that are not required for JTAG operation, but provide additional capability.
2. The IEEE 1149.7 interface is not supported on all devices.
3. This signal is defined as optional by the IEEE 1149.7 when operating in Class 4 or higher.
4. IEEE-ISTO 5001 Nexus signal.

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5. The IEEE 1149.1 specifies a Test Reset ($\overline{\text{TRST}}$) pin; however, the standard defines that by default the pin should be high (enabled) with an internal pull-up resistor in the device. Since normal operation of the device does not require the JTAG port to be enabled, Freescale uses the JTAG compliancy pin (JCOMP), which performs the same basic function, but is asserted (low) by default to disable the JTAG boundary scan/debug port (for normal operation). The IEEE 1149.7 differentiates the default low signal as nTRST_PD (Test Reset pull-down), instead of $\overline{\text{TRST}}$ with a pull-up.

The recommended voltage of the JTAG connector is a nominal 3.3 V, however some devices may only support a 5 V interface.

4.2.1 MPC57xx standardized/legacy JTAG connector

The gollowing table shows the pin out of the recommended JTAG connector to support the MPC57xxX devices.

This connector for the target system is the Tyco part number 2514-6002UB.

NOTE
This pin out is similar to the previous Freescale MPC5500/MPC5600 family of devices. The differences are shown below.

Table 7. JTAG only connector pin-out

Description	Pin	Pin	Description
TDI	1	2	GND
TDO	3	4	GND
TCK	5	6	GND
EVTI/EVTO[1]	7	8	PORST[2, 3]
RESET/ESR0	9	10	TMS
VREF	11	12	GND
RDY[4]	13	14	JCOMP

1. One set of $\overline{\text{EVTI}}$ and $\overline{\text{EVTO}}$ pins may be multiplexed together in the MCU package. (This pin was $\overline{\text{EVTI}}$-only on the MPC5500/MPC5600 devices).
2. This pin was a no-connect on the MPC55xx and MPC56xx devices.
3. On some devices, this pin is named $\overline{\text{ext\_POR}}$.
4. The $\overline{\text{RDY}}$ signal is not available on the MPC57xxM devices. $\overline{\text{EVTO0}}$ can be placed on this pin instead.

4.3 Nexus Auxiliary port and Aurora trace signals

The following table lists all of the Nexus serial trace signals.

NOTE
The Aurora signals require a 100 Ω termination resistor in the tool. The termination resistor should be located inside the tool near the receiver. In many cases, it may be located internal to the tool receiver.

NOTE
The MPC57xx devices incorporate an internal termination resistor in the Nexus Aurora Physical (NAP) block of the MCU for the LVDS clock (CLKP/CLKN).

Table 8.   Nexus Auxiliary port and Aurora connector signals

Signal name	Full signal name	Description
TXnP (+)	Positive polarity transmit signal	The Nexus Aurora port uses one or more lanes of low voltage differential signals to transmit Nexus trace information. When multiple lanes are used, the data is striped between the different lanes. Zero to four lanes are currently projected on future devices. The connector supports up to six lanes.
TXnN (–)	Negative polarity transmit signal	
CLKP (+)	Positive polarity clock signal	The Nexus Aurora physical interface on the MCU requires a differential clock from the tool for formatting the Nexus trace information. The clock frequency should be the same as the transmit data speed.
CLKN (–)	Negative polarity clock signal	
$\overline{\text{EVTI}}$ ($\overline{\text{EVTI0}}$)	Nexus Event Input	After reset, the $\overline{\text{EVTI}}$[2] pin is used to initiate program and data trace synchronization messages or generate a breakpoint. If asserted during reset, upon negation of $\overline{\text{RESET}}$, the device will enter debug mode and not begin code execution.
$\overline{\text{EVTI1}}$[1,]	Nexus Event Input	Additional $\overline{\text{EVTI1}}$ pin for additional synchronization or break functionality.
$\overline{\text{EVTO}}$ ($\overline{\text{EVTO0}}$)[1]	Nexus Event Output	$\overline{\text{EVTO}}$ is an output that provides timing to a development tool for a single watchpoint or breakpoint occurrence. $\overline{\text{EVTI}}$ has multiple Nexus functions. In addition, the Development Semaphore Trigger module can also use the $\overline{\text{EVTO}}$ output pin.
$\overline{\text{EVTO1}}$[1,3]	Nexus Event Output	$\overline{\text{EVTO1}}$ is an additional event output signal.

1. Most of the pins on the device that support the Event signals can be defined to be either inputs ($\overline{\text{EVTIn}}$) or outputs ($\overline{\text{EVTOn}}$).
2. If no number is included, then 0 is assumed for both $\overline{\text{EVTI}}$ and $\overline{\text{EVTO}}$.
3. Not all devices will support multiple $\overline{\text{EVTI}}$ and $\overline{\text{EVTO}}$ signals.

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4.4 Nexus high speed serial connector general purpose pin definitions

The Power.org™ Standard for Physical Connection for High-Speed Serial Trace" specifies five (5) General purpose Input/ Output pins on the 34-pin Samtec connector. However, the IEEE-ISTO 5001-2012 standard defines three of these pins for Nexus functions, leaving three pins for definition for use by the MCU by the MCU manufacturer. In addition, Freescale has redefined the Nexus ClockOut pin although one is predefined to be a CLKOUT signal if needed. The following table lists the general I/O (GEN_IOx) signal definitions for the high speed Aurora interface.

Table 9. General IO definitions

Connector pin number	Power.org definition (General IO pin)	IEEE-ISTO 5001-2012 definition	MPC57xx definition	Description
14	GEN_IO0	GEN_IO0	$\overline{EVTI1}$[1]	$\overline{EVTI1}$ is the secondary input break signal on devices that support two EVTI pins.
16	GEN_IO1	$\overline{EVTI}$		The IEEE-ISTO 5001-2012 defines this as the $\overline{EVTI}$ pin.
18	GEN_IO2	$\overline{EVTO}$		The IEEE-ISTO 5001-2012 defines this as the $\overline{EVTO}$ pin
20	GEN_IO3	GEN_IO3/ CLKOUT	$\overline{RSTOUT}$ or $\overline{PORST}$[2]	GEN_IO3 is a general purpose IO pin predefined in the IEEE-ISTO 5001-2012 standard as Clock Out (if required). Otherwise it can be defined for other uses. $\overline{RSTOUT}$ or $\overline{PORST}$ allows the tool to determine if the device has been reset — not by the $\overline{PORST}$ input.
32	GEN_IO4	$\overline{RDY}$[3]		$\overline{RDY}$ is defined by the IEEE-ISTO 5001-2012 standard. For devices that do not include $\overline{RDY}$, this pin is used for $\overline{EVTO1}$ (if available).
34	GEN_IO5	34	—	Currently not defined.

1. Only available on devices with multiple $\overline{EVTO}$ signals.
2. $\overline{ext\_POR}$ on some devices.
3. Not available on all devices. Can be used for EVTO1 (if available).

Appendix A References

For more information on Nexus and the Nexus implementation on the MPC5500 and MPC5600 families of devices, see the device reference manual and the additional documents listed in the following table.

Table A-1. Nexus References

Document	Title	Location/Availability
e200z0CORERM	e200z0 Power Architecture Core Reference Manual	Freescale web site http://www.freescale.com
e200z1RM	e200z1 Power Architecture Core Reference Manual	
e200z3coreRM	e200z3 Power Architecture Core Reference Manual	

Table continues on the next page...

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Table A-1. Nexus References (continued)

Document	Title	Location/Availability
e200z4RM	e200z4 Power Architecture Core Reference Manual	
e200z6RM	e200z6 PowerPC Core Reference Manual	
e200z759N3CRM	e200z759n3 Power Architecture Core Reference Manual	
e200z760RM	e200z760 Power Architecture Core Reference Manual	
AN2614	MPC553x, MPC555x, and MPC556x Family Nexus Interface Connector	
AN3968	Nexus Interface Connector for the MPC567xF and MPC5676R Families	
AN3970	MPC5500 and MPC5600 Nexus/JTAG Client Access Overview	
AN4030	Using the Development Tool Semaphore Module on the MPC564xA	
AN4088	Nexus Overview and Nexus Support for the MPC5500 and MPC5600 Families	
IEEE-ISTO 5001-1999	The Nexus 5001 Forum™ Standard for a Global Embedded Processor Debug Interface, Version 1	IEEE-ISTO Nexus web site http://www.nexus5001.org
IEEE-ISTO 5001-2003	The Nexus 5001 Forum™ Standard for a Global Embedded Processor Debug Interface, Version 2.0	
IEEE-ISTO 5001-2012	The Nexus 5001 Forum™ Standard for a Global Embedded Processor Debug Interface, Version 3	Available only to IEEE-ISTO 5001 Consortium Members
IEEE Std 1149.1-1990	IEEE Standard Test Access Port and Boundary-Scan Architecture	IEEE web site http://www.ieee.org