Freescale Semiconductor
Application Note

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i.MX53 Power Consumption Measurement on MCIMX53SMD Board

by Freescale Semiconductor, Inc.

This application note is a report that helps the customer to design power management systems. By running several use cases, this report illustrates current drain measurements of the i.MX53 system-on-chip (SoC), taken on the MCIMX53SMD (SMD refers to Smart Mobile Design) board. Therefore, this report enables the customer to choose the appropriate power supply domains for the i.MX53 SoC.

NOTE

The numbers presented in this report are empirical numbers, based on a small sample size. Hence, the numbers are not guaranteed.

Contents

1 Overview of i.MX53 Voltage Supply Rails

The i.MX53 SoC has many power supply domains (voltage supply rails). Figure 1 shows an overview of each of these supply rails.

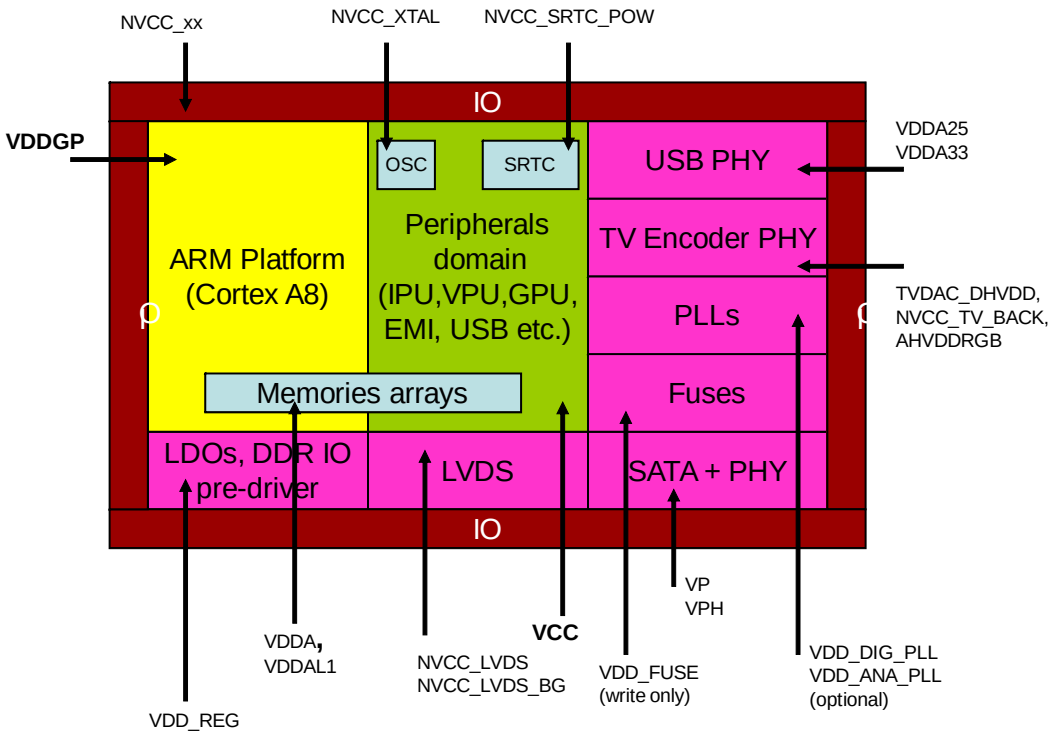

Figure 1. i.MX53 Power Rails

NOTE

See *i.MX53 Applications Processors for Consumer Products* (IMX53CEC), for the recommended operating conditions of each supply rail and for a detailed description of the groups of I/Os (pins) each I/O voltage supply powers.

2 Internal Power Measurement of the i.MX53 Processor

Several use cases (described in Section 3, "Use Cases and Measurement Results,") are run on the MCIMX53SMD board. The measurements are taken mainly for the two power supply domains: VDDGP, which is the ARM core supply, and VCC, which is the peripheral supply. These two supply domains consume the majority of the internal power of the processor. For relevant use cases, the power of additional supply domains is added. However, the power of these supply domains does not depend on specific use cases, but whether these modules are used or not. The power consumption of SRTC is comparatively negligible in most of the modes, except in low power and audio playback modes.

The power of NVCC_XTAL and PLL is described in Section 2.1, "On-Chip Oscillator Power," and Section 2.2, "PLL Power," respectively.

The NVCC_* power consumption mainly depends on the board level configuration and the components.

Therefore, it is not included in the i.MX53 internal power analysis. The power of NVCC_EMI_DRAM is added for reference.

The power consumption for these supplies, in different use cases, is provided in Table 1 through Table 7.

NOTE

Unless mentioned differently, all the measurements are done on typical process silicon, at room temperature (25 °C approximately).

2.1 On-Chip Oscillator Power

The 24 MHz on-chip oscillator amplifier that uses an external crystal is powered from the NVCC_XTAL supply domain. Its voltage on the MCIMX53SMD board is 2.5 V and it consumes ~0.7 mA (1.8 mW). It is enabled in all cases, except for Stop mode (if SBYOS bit is set in the CCM (Clock Controller Module)). This power should be added to each of the relevant use cases below as part of the total power.

2.2 PLL Power

The i.MX53 SoC has four PLLs. Each PLL is powered from the following two power supplies:

- Digital supply: Its nominal voltage is 1.3 V. By default, it is driven by the on-chip LDO, but can also be sourced from NVCC_DIG_PLL supply pin.
- Analog supply: Its nominal voltage is 1.8 V. By default, it is driven by the on-chip LDO, but can also be sourced from NVCC_ANA_PLL supply pin.

The power consumed by a PLL (from both supplies) depends upon the frequency at which the PLL is running. For example, the power consumed by a PLL at 800 MHz is almost twice the power it would consume at 400 MHz. The power consumed by a PLL at 400 MHz is between 1.5 mW and 2 mW.

The nominal frequencies for the four PLLs are as follows:

- 1 GHz for PLL1
- 400 MHz for PLL2
- 432 MHz for PLL3 (divided-by-2 clock output is used)
- 595 MHz for PLL4

The total power consumed by the four PLLs at their nominal frequencies is ~9 mW. This power is included in VDD_REG power, since the internal LDOs are powered from VDD_REG.

NOTE

In audio playback and low power modes, the number of enabled PLLs can be reduced through optimization.

2.3 DDR I/O Power

The DDR I/O is supplied from the following two power supply domains:

- VDD_REG: Provides the power for pre-drivers of the DDR pads. The target voltage for this supply is 2.5 V.

NOTE

This supply also provides power to the on-chip LDOs (PLL power).

- NVCC_EMI_DRAM: Provides the power for the DDR I/O pads. The target voltage for this supply depends on the DDR interface being used. The target voltages for the different DDR interfaces are as follows:
  - 1.8 V for DDR2
  - 1.5 V for DDR3
  - 1.2 V for LPDDR2

The power consumption for the NVCC_EMI_DRAM supply is affected by various factors, including:

- Amount of activity of the DDR interface
- Termination (enabled/disabled, which termination resistors are used)
- Configuration of the DDR pads (such as, drive strength)
- Board layout
- Load of the DDR memory devices

Therefore, the measurement values provided in the below tables cannot be guaranteed; they should be used only as estimated values.

NOTE

The measured current also includes the I/O current of the onboard DDR3 devices, and in some cases, also the current of the core of the DDR3 devices. The MCIMX53SMD board (on which measurements were taken) includes four DDR3 devices, each having width of 16 bits and capacity of 2 Gbits. For power optimized systems that use LPDDR2 memories, the power consumed by the DDR I/O and DDR memories would be significantly lower.

2.4 Voltage Levels and DVFS Usage in Measurement Process

The voltage levels of all the supplies, except for VDDGP and VCC, are set to the typical voltage levels as defined in *i.MX53 Applications Processors for Consumer Products* (IMX53CEC).

The VDDGP and VCC supplies require special explanations. To save power, VDDGP voltage are changed using DVFS (dynamic voltage and frequency scaling), during the run time of the use cases. The voltage levels of these supplies can be changed to standby voltage levels during low power modes.

2.4.1 VDDGP Voltage Levels

The target voltage levels for VDDGP are as follows (see IMX53CEC for the official operating points):

- 0.9 V for 160 MHz setpoint
  - 160 MHz is achieved by dividing 800 MHz by 5, although frequency can go up till 167 MHz according to IMX53CEC at this lowest setpoint.

  - For Ubuntu and Android, 160 MHz setpoint was removed. The impact on power is not clear as it may reduce power in some use-cases, as CPU is idle for longer period. However, it requires slightly higher voltage.
- 0.95 V for 400 MHz setpoint
- 1.1 V for 800 MHz setpoint
- 1.25 V for 1 GHz setpoint

Most of the measurements are done using these voltage levels and the power data that appears in this document is according to these values. In case the measurement is done at different voltage levels, the results are scaled accordingly. In real applications when DVFS is applied, the frequency and voltage values are automatically adjusted according to the use case requirements. In Stop mode, VDDGP can be lowered to 0.85 V.

In normal operation mode, core frequency is set to 1 GHz during measurements. In DVFS mode, it can be scaled down to 800 MHz, 400 MHz, or 160 MHz.

The voltage used for power calculation is the average voltage between those setpoints. It depends on the amount of time spent at each setpoint.

2.4.2 VCC Voltage Levels

The target voltage level for VCC is 1.3 V (up to 200 MHz for AXI bus frequency, 133 MHz for AHB bus frequency, and 400 MHz for DDR frequency).

In Stop mode, VCC can be lowered to 0.95 V.

2.5 Hardware and Software Used

The software versions used for the measurement are as follows:

- Ubuntu 10.04 (Linux BSP version: L2.6.35_11.05.01_ER_RC3_Update_
- Android R10.3.1-RC1
- Windows CE 7 (Linux BSP version: BSP WCE700_11.05.03_ER)

The board used for Ubuntu, Android, and WinCE measurements is MCIMX53SMD Rev B board (SCH-26876 REV B). The measurements were done using Agilent 34401A 6 ½ Digit Multimeter.

2.6 Measuring Points on MCIMX53SMD Board

The measurements are done by measuring the average voltage drop over the measurement points, and dividing it by the resistor value to get the average current. The measuring points for the various supply domains are as follows:

- VCC: The VCC current is measured on SH13 and the recommended resistance value for this measurement is 0.02 Ω.
- VDDGP: The VDDGP current is measured on SH11 and the recommended resistance value for this measurement is 0.02 Ω.

- VDD_REG: The VDD_REG current is measured on SH10 and the recommended resistance value for this measurement is 0.2 Ω.
- DDR3 I/O: The current in this domain includes the NVCC_EMI_DRAM current and the I/O current of the onboard DDR3 devices. The current in this domain is measured on SH4 and the recommended resistance value for this measurement is 0.02 Ω.
- DDR3 I/O + Memories: The current in this domain includes the NVCC_EMI_DRAM current and the overall current of the onboard DDR3 devices. The current in this domain is measured on SH26 and the recommended resistance value for this measurement is 0.02 Ω.
- NVCC_XTAL: The NVCC_XTAL current is measured on SH5 and the recommended resistance value for this measurement is 10 Ω.
- NVCC_SRTC_POW: The NVCC_SRTC_POW current is measured on SH9 and the recommended resistance value for this measurement is 100 Ω.

3 Use Cases and Measurement Results

3.1 Use Cases

The main use cases and subtypes, which form the benchmarks for i.MX53 internal power measurements, are as follows:

- Low power mode
  - Stop mode
  - System Idle mode
  - User Idle mode
- Audio playback
  - MP3 Audio Playback
- Video playback
  - H.264 Video Playback, 720p at 9 Mbps on XGA LCD
  - H.264 Video Playback, 1080p at 10 Mbps on XGA LCD
- Web Browsing
  - 720p Flash Video Playback by Web Browsing on XGA LCD

3.2 Low Power Mode Use Cases

For all low power mode use cases, perform the following two steps:

1. Disable the Ethernet and USB.
2. Enable DVFS-CORE and bus frequency scaling.
   - For System Idle mode, frequencies of AHB bus and peripheral (IP) bus are scaled from 133 MHz to 50 MHz and 66.5 MHz to 25 MHz, respectively.
   - For User Idle mode, frequencies of AHB bus and peripheral (IP) bus are scaled from 133 MHz to 80 MHz and 66.5 MHz to 40 MHz, respectively.

To obtain the results for low power mode use cases in case of Ubuntu measurements, perform the following steps:

- Boot up the board by using the image with USB built-out and the command-line statement: exec -c "noinitrd console=ttymxc0,115200 root=/dev/mmcblk0p1 rw rootwait ip=dhcp di1_primary video=mxcdi1fb:RGB666,XGA ldb jtag=off debug_uart=on no_console_suspend usbcore.autosuspend=2 splash text", and disable USB devices
- Make sure that no USB device is currently active (lsmod and check no ehci_hcd)
- Run the following command to disable the Ethernet:
  ifconfig eth0 down
- Run the following command to enable DVFS-CORE:
  echo 1 > /sys/devices/platform/mxc_dvfs_core.0/enable
- Run the following command to enable bus frequency scaling:
  echo 1 > /sys/devices/platform/busfreq.0/enable
- Run the following command to make sure that all the USB clock usage is 0:
  cat /proc/cpu/clocks | grep usb

3.2.1 Use Case 1—Stop Mode

The use case is as follows:

- ARM CORE is in the SRPG (state retention power gating) mode
- All PLLs (phase locked loop) and CCM (clock controller module) generated clocks are OFF
- USB PHY PLL is OFF
- SATA PHY is suspended (kept in the PDDQ mode)
- CKIL (32 kHz) input is ON
- All the modules are disabled
- External high frequency crystal and on chip oscillator are powered down (by asserting SBYOS bit in CCM)
- Standby voltages are applied to VDDGP and VCC

In this mode, no current flow is caused by external resistive loads. This use case simulates the situation when the device is in standby mode (commonly called suspend mode in OS).

Table 1 shows the measurement results when this use case is applied on the i.MX53 processor.

Table 1. Stop Mode Measurement Results

Supply Domain	Voltage (V)	Android		Ubuntu[1]		WinCE[1]	
		P (mW)	I (mA)	P (mW)	I (mA)	P (mW)	I (mA)
VDDGP	0.85	0.085	0.1	0.2	0.25	0.04	0.05
VCC	0.95	3	3.15	2.8	2.95	2.53	2.65
VDD_REG	2.5	1.12	0.45	1.5	0.6	4.3	1.75

Table 1. Stop Mode Measurement Results (continued)

Supply Domain	Voltage (V)	Android		Ubuntu[1]		WinCE[1]	
		P (mW)	I (mA)	P (mW)	I (mA)	P (mW)	I (mA)
Total Power (without DDR3 I/O + Memories)		**4.2**		**4.5**		**6.87**	
DDR3 I/O + Memories[2]	1.5	31.4	20.8	32	21.3	32	21.3
Total Power		35.6		36.5		38.87	

1 USB is used for wakeup; hence, the VCC current is high to enable this option. When USB wakeup is disabled, the VCC current is below 1 mA for this mode.

2 The current in this domain includes the NVCC_EMI_DRAM current and I/O and memories current of the onboard DDR3 devices. The current for the NVCC_EMI_DRAM supply is high due to the onboard resistors used for impedance matching. In case of LPDDR2 memories, the expected current of DDR I/O + Memories for Stop mode is few milliamps and the current of the MX53 DDR I/O is nearly zero.

3.2.2 Use Case 2—System Idle Mode

The use case is as follows:

- ARM is in SRPG mode most of the time; this significantly minimizes the current
- PLLs are always ON
- Operating system is ON
- LCD is turned OFF
- Screen is not refreshed

This use cases simulates the situation when the device is left idle for some time and the display is turned OFF after the timer expires.

Table 2 shows the measurement results when this use case is applied on the i.MX53 processor.

Table 2. System Idle Mode Measurement Results

Supply Domain	Ubuntu			WinCE		
	Voltage (V)	P (mW)	I (mA)	Voltage (V)	P (mW)	I (mA)
VDDGP	0.96	0.33	0.35	0.96	0.19	0.2
VCC	1.3	39.5	30.2	1.3	19.7	15.1
VDD_REG	2.52	32.5	12.9	2.48	10.3	4.15
Total Power (without DDR3 I/O + Memories)		**72.33**			**30.19**	
DDR3 I/O + Memories	1.55	51.9	33.5	1.5	32	21.3
Total Power		124.23			62.19	

3.2.3 Use Case 3—User Idle Mode

The use case is as follows:

- ARM is in SRPG mode most of the time; this significantly minimizes the current
- PLLs are always ON
- Operating system and LCD are ON, but not in operation
- The XGA screen refresh is done by IPU through LVDS

The use case simulates the situation when the device is left idle and no application is performed on the screen (like reading from the screen).

Table 3 shows the measurement results when this use case is applied on the i.MX53 processor.

Table 3. User Idle Mode Measurement Results

Supply Domain	Android			Ubuntu[1]			WinCE		
	Voltage (V)	P (mW)	I (mA)	Voltage (V)	P (mW)	I (mA)	Voltage (V)	P (mW)	I (mA)
VDDGP	0.96	2.1	2.2	0.96	0.96	1	1.1	0.39	0.35
VCC	1	153.14	116.9	1.3	160.1	122.4	1.3	155.1	118.8
VDD_REG	2.5	57.5	22.9	2.52	34.5	13.7	2.48	60	24.25
Total Power (without DDR3 I/O + Memories)		**212.74**			**195.56**			**215.49**	
DDR3 I/O + Memories	1.53	218.5	142.6	1.55	251	162.2	1.5	282	187.8
Total Power		431.24			446.56			497.49	

1 Numbers are taken using the Text mode.

3.3 Audio Playback Use Cases

3.3.1 Use Case 1—MP3 Audio Playback

The use case procedure is as follows:

1. MP3 (MPEG-1 audio layer 3) decoding is done by Cortex™-A8.
2. Audio playback is run through SSI (serial synchronous interface).
3. The stream 128 Kbps_44 kHz_s_mp3.mp3 is taken from the SD (secure digital) card.

The LCD is turned OFF after the timer expires.

Table 4 shows the measurement results when this use case is applied on the i.MX53 processor.

Table 4. MP3 Audio Playback Measurement Results

Supply Domain	Android			Ubuntu[1]			WinCE		
	Voltage (V)	P (mW)	I (mA)	Voltage (V)	P (mW)	I (mA)	Voltage (V)	P (mW)	I (mA)
VDDGP	0.96	18.45	17.6	0.96	14.1	14.7	0.96	9.4	9.8
VCC	1.3	38.5	29.55	1.3	36.1	27.8	1.3	27.1	20.8
VDD_REG	2.5	12.5	5	2.51	29.3	11.7	2.48	14.1	5.7
Total Power (without DDR3 I/O + Memories)		**69.45**			**79.5**			**50.6**	
DDR3 I/O + Memories	1.54	55	36.4	1.54	75.8	49.2	1.5	50.6	33.6
Total Power		124.45			155.3			101.2	

1 Numbers are taken using the Text mode.

Frequencies of AHB bus and peripheral (IP) bus are scaled from 133 MHz to 50 MHz and 66.5 MHz to 25 MHz, respectively. To achieve these numbers, disable the Ethernet and USB.
Both DVFS-CORE and bus frequency scaling enabled.

To enable DVFS-CORE, use the following command:
echo 1 > /sys/devices/platform/mxc_dvfs_core.0/enable

To enable bus frequency scaling, use the following command:

echo 1 > /sys/devices/platform/busfreq.0/enable

3.4 Video Playback Use Cases

3.4.1 Use Case 1—H.264 Video Playback, 720p at 9 Mbps on XGA LCD

This use case has the following features:

- The video source is H.264, 720p resolution, 30 fps, 9 Mbps bitrate

- The audio source is AAC, 48 kHz, 64 Kbps stereo
- The display is of XGA resolution using LVDS

The video/audio stream is loaded from the SD card into the DDR (double data rate) memory and then demuxed by Cortex-A8. The demuxed video signal is decoded by the VPU. It is then resized to XGA in IPU and displayed on the LCD display (through LVDS) with a refresh rate of 60 Hz. In parallel, the demuxed audio signal is decoded using Cortex-A8 and is played back through the SSI.

Table 5 shows the measurement results when this use case is applied on the i.MX53 processor.

Table 5. 720P Video Playback Measurement Results[1]

Supply Domain	Voltage (V)	Ubuntu[2]	
		P (mW)	I (mA)
VDDGP	0.9	45.72	50.8
VCC	1.3	271.3	207.75
VDD_REG	2.5	69	27.6
DDR3 I/O	1.5	274	182.4
Total Power		**660.02**	

1 Measurement results are based on the previous Linux BSP release.
2 Numbers are taken using gst-player running from GUI.

Frequencies of AHB bus and peripheral (IP) bus are scaled from 133 MHz to 80 MHz and 66.5 MHz to 40 MHz, respectively. To achieve these numbers, disable the Ethernet and USB.
Both DVFS-CORE and Bus frequency scaling enabled.

To enable DVFS-CORE, use the following command:
echo 1 > /sys/devices/platform/mxc_dvfs_core.0/enable

To enable bus frequency scaling, use the following command:

echo 1 > /sys/devices/platform/busfreq.0/enable

3.4.2 Use Case 2—H.264 Video Playback, 1080p at 10 Mbps on XGA LCD

This use case has the following features:

- The video source is H.264, 1080p resolution, 24 fps, 10 Mbps bitrate
- The audio source is AAC, 48 kHz, 192 Kbps stereo
- The display is of XGA resolution using LVDS

The video/audio stream is loaded from the SD card into the DDR (double data rate) memory and then demuxed by Cortex-A8. The demuxed video signal is decoded by the VPU. It is then taken by IPU, resized to XGA, and displayed on the LCD display (through LVDS) with a refresh rate of 60 Hz. In parallel, the demuxed audio signal is decoded using Cortex-A8 and is played back through the SSI.

Table 6 shows the measurement results when this use case is applied on the i.MX53 processor.

Table 6. 1080P Video Playback Measurement Results

Supply Domain	Android			Ubuntu[1]			WinCE		
	Voltage (V)	P (mW)	I (mA)	Voltage (V)	P (mW)	I (mA)	Voltage (V)	P (mW)	I (mA)
VDDGP	0.96	42.54	44.55	0.96	41.4	43.1	1.1	74.2	66.8
VCC	1.3	282.6	216.9	1.3	308.8	237	1.3	268.9	206.2
VDD_REG	2.5	74.5	29.8	2.5	74.3	29.7	2.51	74.8	29.8
Total Power (without DDR3 I/O + Memories)		**399.64**			**424.5**			**417.9**	
DDR3 I/O + Memories	1.5	549.9	359.4	1.52	577.1	379.7	1.53	614.9	402.4
Total Power		949.54			1001.6			1032.8	

1 Numbers are taken using gst-player running from GUI.

Frequencies of AHB bus and peripheral (IP) bus are scaled from 133 MHz to 80 MHz and 66.5 MHz to 40 MHz, respectively. To achieve these numbers, disable the Ethernet and USB.
Both DVFS-CORE and Bus frequency scaling enabled.

To enable DVFS-CORE, use the following command:
echo 1 > /sys/devices/platform/mxc_dvfs_core.0/enable

To enable bus frequency scaling, use the following command:

echo 1 > /sys/devices/platform/busfreq.0/enable

3.5 Web Browsing Use Cases

3.5.1 Use Case 1—720p Flash Video Playback by Web Browsing on XGA LCD

This use case has the following features:

- The video source is of 720p resolution, 30 fps, 2040 Mbps bitrate
- The audio source is AAC, 44.1 kHz, 125 Kbps stereo
- The display is of XGA resolution using LVDS

The video/audio stream is loaded through the Ethernet controller into the DDR (double data rate) memory and then demuxed by Cortex-A8. The demuxed video signal is decoded by the VPU. It is then resized to XGA in IPU and displayed on the LCD display (through LVDS) with a refresh rate of 60 Hz. In parallel, the demuxed audio signal is decoded using Cortex-A8 and is played back through the SSI.

The browser used is Firefox, and video is played from a local server. The video stream is Toy Story 3 trailer 2 (official trailer), select 720p, full screen size. Measurements are taken during playback (from DDR), in

parallel to reading video data through the Ethernet controller into DDR. Table 7 shows the measurement results when this use case is applied on the i.MX53 processor.

Table 7. 720p Flash Video Playback Measurement Results [1]

Supply Domain	Voltage (V)	Ubuntu	
		P (mW)	I (mA)
VDDGP	0.95	130	138
VCC	1.3	248	191
VDD_REG	2.5	76.5	30.6
DDR3 I/O	1.5	225.5	150.3
Total Power		**680**	

[1] Measurement results are based on the previous Linux BSP release.

4 Reducing Power Consumption

The overall system power consumption greatly depends on software optimization and how system hardware is implemented. Below is a list of suggestions which may help to reduce system power. Part of this is already implemented in Linux BSP and WinCE. Further optimizations can be done on individual customer's system.

- Apply clock gating whenever clocks or modules are not used, by configuring CCGR registers in the CCM (Clock Controller Module).
- Reduce the number of operating PLLs: Applicable mainly in Audio Playback mode or Idle modes.
- Core DVFS and system bus scaling: Applying DVFS for ARM and scaling the frequencies of the AXI, AHB, and IPG bus clocks can significantly reduce the power consumption of VDDGP domain and VCC domain, respectively. However, due to the reduced operation frequency, the accesses to the DDR take longer which increases the power consumption of the DDR I/O and memories. This tradeoff needs to be taken into account for each mode, to quantify the overall affect on system power.
- Put MX53 into low power modes (Wait, Stop) whenever possible. See the CCM chapter of i.MX53 reference manual for details.
- DDR interface optimization:
  - Use careful board routing of the DDR memories, maintaining lines as short as possible.
  - If possible (depends on board routing), do not enable ODT (On Die Termination). This greatly influences the power consumption of the DDR interface pins.
  - Use proper output driver impedance for DDR interface pins which provides good impedance matching. Select the lowest possible drive strength which still provides the required performance, in order to save current through DDR I/O pins.
  - Carefully choose onboard resistors so the least amount of current is wasted, for example, when selecting impedance matching resistors between CLK and CLK_B (when using DDR2/DDR3 memories).

— Float MX53 DDR interface pins (set to high Z) when DDR memory is in self refresh mode.

The various steps involved in floating of MX53 DDR interface pins are given below.

NOTE

All these steps are performed when the code is running from the internal RAM rather than from the DDR memory.

Steps to be performed before entering suspend (Stop mode):

1. Set the memory to self refresh mode manually, by asserting a software DVFS request in M4IF. Wait for an acknowledge from the M4IF.
2. Set the DSE (drive strength selection, in IOMUXC) for all DDR IF I/O to 0 (High Z), except for CKE0 and CKE1.
3. Get into the Stop mode.

Steps to be performed after exiting suspend:

1. Set the DSE for all I/O to the required value.
2. De-assert the SW DVFS request. Wait for an acknowledge from the M4IF.

DDR pins can be floated in the same manner, even when suspend is not entered and DDR can be put into self refresh, to save power. This happens when CPU is not running, or it is running from the internal RAM.

5 Revision History

Table 8 provides a revision history for this application note.

Table 8. Document Revision History

Rev. Number	Date	Substantive Change(s)
Rev 1	02/2012	• In Section 2.5, “Hardware and Software Used,” replaced the second bullet item “Android 10.2” with “Android R10.3.1-RC1.” • In Table 1, updated Android results based on Anrdoid R10.3.1-RC1 release. • In Table 3, updated Android results based on Anrdoid R10.3.1-RC1 release. • In Table 4, updated Android results based on Anrdoid R10.3.1-RC1 release. • In Table 6, updated Android results based on Anrdoid R10.3.1-RC1 release.
Rev 0	07/2011	Initial release.

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