Cookbook for SAR ADC Measurements
ADC measurements done properly

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1   Introduction

An analog-to-digital converter (ADC) cannot ensure ideal accuracy by itself. A number of parameters can affect the achievable accuracy of an ADC in an application.

For example:
- ADC timing (that is, acquisition time, conversion time, sampling time, sampling jitter, and so on)
- Power supply characteristics (noise and internal impedance)
- Isolation between digital and analog portions of the data acquisition system
- Internal and external impedance matching
- Input/output switching
- PCB layout

To achieve optimal performance, it is necessary to consider the application note provides comprehensive guidelines on the procedure. This document gives comprehensive guidelines on how to correctly select and design the required external RC components for a SAR ADC input based upon a selected acquisition time and other converter parameters that can be found in the controller documentation.

This application note is developed to address a number of similar requests from several customers. One customer reported having performed an investigation of the influence of the ADC during sampling, and also the influence of different values of external RC components on performance. They

Contents

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observed serious voltage disturbances (voltage drops/peaks) at the ADC input (see Figure 1). This disturbance was even worse in the case of sequential sampling, when the previously measured signal was grounded. The disturbance at the ADC input in this case results from the basic principle of operation of the sample and hold (S/H) circuit inherent in a SAR ADC. These disturbances do not have to introduce a loss of conversion accuracy as long as the ADC timing is set correctly. If appropriate precautions are not taken, a significant reduction in the accuracy of the digital result can occur during the conversion. This application note clearly shows how to avoid this situation by choosing the correct conversion time and external RC components. The examples of correct external RC component design are presented at the end of the application note. The examples clearly demonstrate proper selection of external components for the cyclic and SAR ADC used in Freescale devices and also mention common mistakes related to incorrect selection of external resistance.
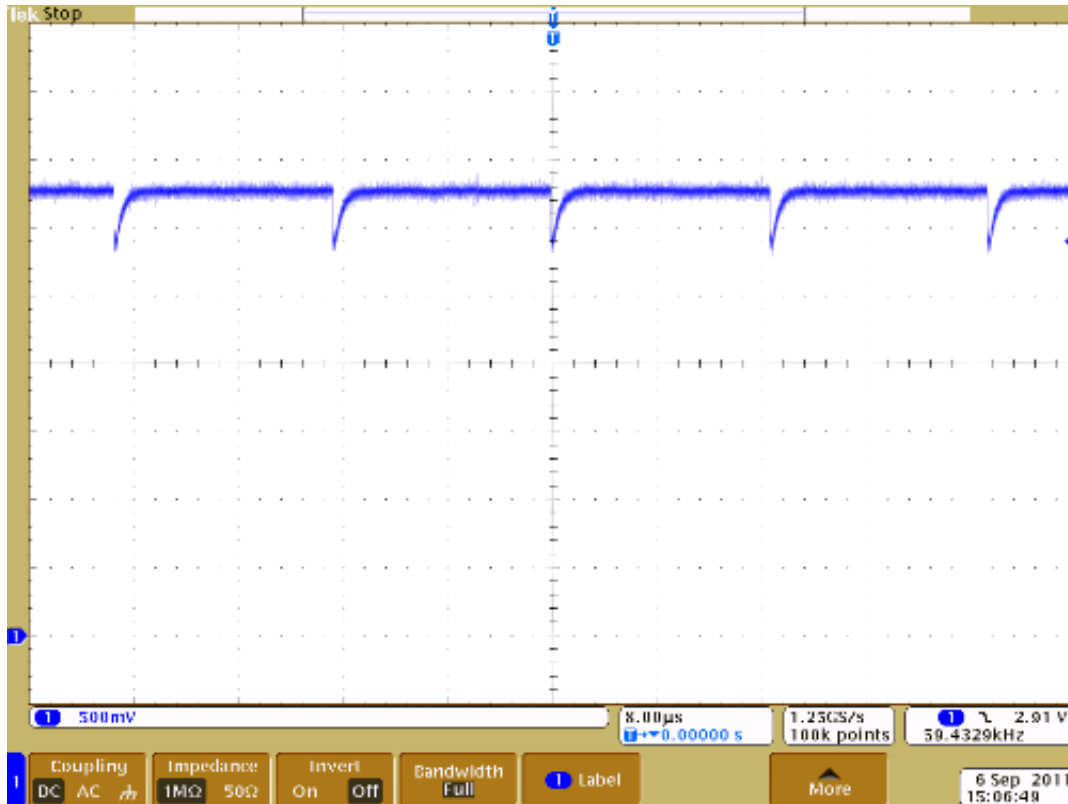
Figure 1. Voltage drops at ADC input during sampling process

2 Theoretical background

To achieve the best performance from an ADC, the overall system must be designed and configured correctly.

The hardware setup must carefully follow data sheet recommendations, for example:

- Place 0.1 µF capacitor positioned as near as possible to the package power pins (one capacitor for each power pins pairs)
- Place approximately 100 µF capacitor to power pins
- PCB trace lengths should be minimal
- It is necessary to consider all parasitic passive components due to PCB traces in your application
- Special care must be taken to minimize noise levels on the analog power and reference pins
- Use separate power and ground planes for digital and analog supply pins

- If the analog and digital circuits are connected to the same power supply a small inductor (or ferrite) should be connected between digital and analog pins
- Separate analog components from noisy digital components by ground planes (not in parallel), and place the analog ground trace around the analog signal trace

In addition the aforementioned recommendations, special attention must be paid to the design and selection of the external RC components. Minimum values for the external RC components must be considered in final calculations. See *MC56F825x/ MC56F824x Digital Signal Controller* (document MC56F825X)

In the text below, the basic principle of the sample and hold circuit (S/H) that is inherently part of an ADC is described in detail. An equivalent sampling circuit considered to present the required background theory is shown in Figure 2. To simplify the sampling process all parasitic components are neglected.

NOTE

It is desirable to mention that the equivalent sampling circuit in Figure 2 represents simplified form of ADC used in Freescale devices. The equivalent sampling resistance R_{SH} is represented by total serial resistance connected between sampling capacitance and analog input pin (sampling switch, multiplexor switches etc.). The sampling capacitance C_{SH} is represented by total parallel capacitance. For example in a case of Freescale SAR ADC equivalent sampling capacitance contains bank of capacitances. Each capacitance in the bank should be charged by the measured input pin voltage during sampling time (later as acquisition time). During the rest hold and successive approximation time (conversion steps) the energy stored in each capacitance is charged/discharged to V_{REFH} accordingly to the particular sequence of binary weighted principle. In general, both equivalent sampling resistance R_{SH} and equivalent sampling capacitance C_{SH} can be found in datasheet (usually hidden under different names).
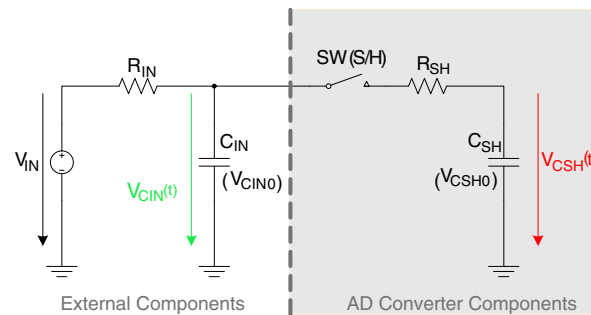

Figure 2. Equivalent sampling circuit

Considering the correct sampling process (including *Nyquist-Shannon* sampling theorem), it is possible to replace a measured input signal with a constant DC voltage source during the ADC time. If the signal source is assumed to have a large input impedance ($R_{IN} \gg R_{SH}$), two essentially different time intervals of sampling capacitance charging appears. This is not a common case, but a lot of designers use it (usually $R_{IN} \leq R_{SH}$). Time waveforms for the voltage across the sampling capacitor C_{SH} (red) and the voltage across the input capacitor C_{IN} (green) are shown in Figure 3.

NOTE

Figure 3 assumes that the initial voltage across the input capacitor C_{IN} is greater than the initial voltage across the sampling capacitor C_{SH} ($V_{CIN0} > V_{CSH0}$). In such a case, the voltage drop across the input capacitor appears (see Figure 3). In some cases this condition is not satisfied, that is $V_{CIN0} < V_{CSH0}$. In this case, a voltage peak across the input capacitor appears. The magnitude of the voltage drop/peak is defined by Eqn.6.

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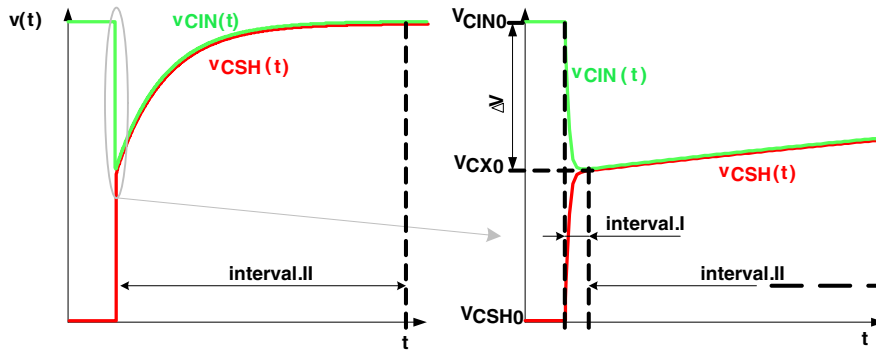
Figure 3. Example of time waveforms of voltage across sampling capacitor and voltage across input capacitor (b. in detail)

In Figure 3, the charging of the sampling capacitor C_{SH} should be divided into two time intervals (see Figure 2). In the case of high input impedance, the second interval is much slower than the first one. Taking these facts into account, the equivalent circuit from Figure 2 can be divided into two separate equivalent circuits as shown in Figure 4. The first (shorter) interval is represented by the circuit shown in fig. 4a. Solving a system of differential equations, it is possible to achieve mathematical representation of voltage time waveforms. The voltage across sampling capacitance is defined as:

$$V_{CSH}(t) = (V_{CIN0} - V_{CSH0})\frac{\alpha}{\alpha+1}\left(1 - e^{-\frac{t}{\tau_I}}\right) + V_{CSH0}$$

Equation 1

and the voltage across input capacitance as:

$$V_{CIN}(t) = (V_{CIN0} - V_{CSH0})\left(\frac{\alpha}{\alpha+1} - \frac{1}{\alpha+1}e^{-\frac{t}{\tau_I}}\right) + V_{CSH0}$$

Equation 2

Where V_{CIN0} represents the initial voltage across input capacitance (this voltage is equal to the measured input voltage), V_{CSH0} represents initial voltage across input capacitance C_{IN}. The value of initial voltage across the sampling capacitor C_{SH} depends on the specific ADC input architecture. In a case of redistribution charging architecture of SAR ADC or if a presampling circuit is used, then the initial voltage can be equal to V_{REFL} or V_{REFH}. In some special cases, this value can be set to (V_{REFH} - V_{REFL})/2 in order to ensure lower voltage stress of capacitor. Usually when sequential sampling is used, then the initial voltage V_{CSH0} is equal to the previous channel voltage conversion.

The τ_I in Eqn. 2 represents time constant of the equivalent circuit, that is:
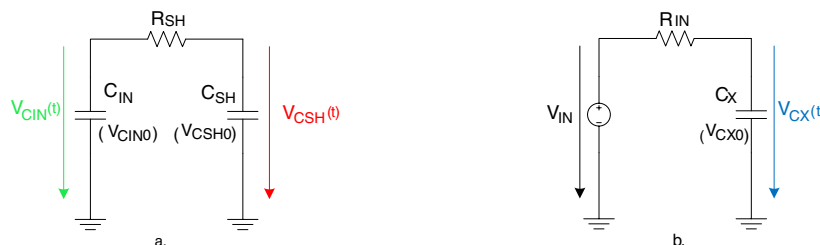
$$\tau_I = R_{SH}\frac{C_{IN} * C_{SH}}{C_{IN} + C_{SH}}$$

Equation 3

and symbol α represents:

$$\alpha = \frac{C_{IN}}{C_{SH}}$$

Equation 4

Figure 4. Equivalent circuits a.Interval I, b. Interval II

Cookbook for SAR ADC Measurements , Rev 1, 04/2014

The voltage waveforms for the first interval are shown in Figure 5. The gray dashed line represents the real waveform of voltage across the input capacitor C_{IN}. This interval represents the charging of sampling capacitor C_{SH} by energy accumulated in the input capacitor (usually $V_{CIN0} = V_{IN}$). In a steady state, no energy is transferring; the current is zero, and voltages across both capacitors are equal. A mathematical expression of steady state voltage is defined using substitution $t \rightarrow \infty$ intoEqn.1 and 2:

$$v_{CX0} = (t) = (V_{CIN0} - V_{CSH0})\frac{\alpha}{\alpha+1} + V_{CSH0} = \frac{\alpha}{\alpha+1}V_{CIN0} + \frac{1}{\alpha+1}V_{CSH0}$$
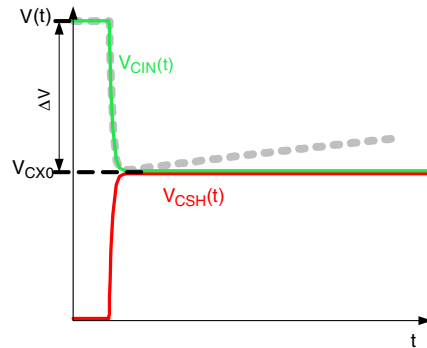
Equation 5

From Eqn. 5 and Figure 5 it is possible to derive a magnitude of voltage drop (or peak) across the input capacitor during the first interval.

$$\Delta V = V_{CIN0} - v_{CX0} = \frac{1}{\alpha+1}(V_{CIN0} - V_{CSH0})$$
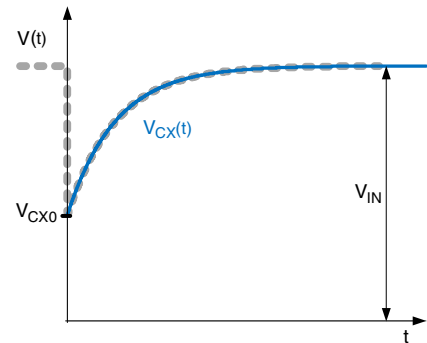
Equation 6

Referring to Eqn.4, it can be seen that a higher ratio between input and sampling capacitance will produce a smaller voltage drop (or peak).

Figure 5. Time waveforms of voltages for interval I. of sampling capacitor charging

The equivalent circuit shown in fig. 4b represents the second interval of the sampling capacitor charging. Again, considering the case of a high input impedance ($R_{IN} \gg R_{SH}$), and also assuming that the interval I voltage across the sampling capacitance V_{CSH} is equal to the voltage across input capacitance V_{CIN} during this time interval; the parallel connection of the input capacitor and sampling capacitor can be represented by the equivalent capacitance C_X. The initial voltage across C_X is given by the steady state voltage of the first interval, see Eqn. 5 . The time-domain waveform of the voltage across the equivalent capacitor $v_X(t)$ is shown in Figure 6 . The gray dashed line represents the real waveform of the input voltage.

Figure 6. Time waveforms of voltage for interval II of sampling capacitor charging

A mathematical expression for the voltage across the equivalent capacitance $v_{CX}(t)$ (7) was derived by solving a system of differential equations (resulting from equivalent circuit).

$$v_{CX}(t) = (V_{IN} - V_{CX0})\left(1 - e^{-\frac{t}{\tau_{II}}}\right) + V_{CX0}$$

Equation 7

where V_{CX0} represents the initial voltage across the equivalent capacitance, and τ_{II} represents time constant for second interval, that is:

Eqn. 8

$$\tau_{II} = R_{IN}(C_{IN} + C_{SH})$$

The basic requirement for the level of voltage across the sampling capacitance C_{SH} at the end of the sampling period (acquisition time) must be defined by following condition:

$$V_{IN} - v_{CX}(T_{AQ}) \le \frac{V_{FSR}}{2^{(N+1)}}$$

Equation 8

Where T_{AQ} is an acquisition time, V_{FSR} is ADC full scale range voltage and N is the ADC resolution in number of bits. The expression on the right side of Eqn.9 represents the voltage error caused by ½ LSB of the ADC.
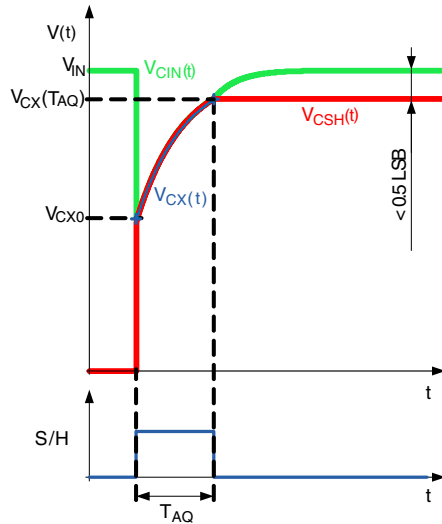
Figure 7. Voltage waveforms during acquisition time

To achieve an acceptable level of voltage across the sampling capacitance (loss of ½ LSB) the S/H switch must be switched on during acquisition time T_{AQ} given by the following equation (see also Figure 7):

$$T_{AQ} \ge \tau_{11} \cdot \ln\left(\frac{(V_{IN} - V_{CSH0})}{(1+\alpha).V_{FSR}}.2^{(N+1)}\right)$$

Equation 9

On the other hand, when the value of input resistance is required and acquisition time is known:

$$R_{IN} \le \frac{T_{AQ}}{(C_{IN} + C_{SH})\ln\left(\frac{(V_{IN} - V_{CSH0})}{(1+\alpha).V_{FSR}}.2^{(N+1)}\right)}$$

Equation 10

3   Example

The examples provided in this section demonstrate the procedure to design external RC components of ADC. Proper external RC components design is shown on two different ADC modules widely used in Freescale devices, especially DSCs and Kinetis devices.

Freescale DSC devices use 12-bit cyclic ADC with multiple analog inputs. Each ADC contains one sample and hold circuit (in some special cases each input can have its own sample and hold circuit). This ADC also includes PGA with selectable gain. Depending on the device it can be switch-capacitance gain amplifier or linear resistive operation amplifier (see reference manual for more details). The acquisition time in these devices is directly dependent on ADC clock (1 ADC clock time). If it is required to increase acquisition time it is necessary to increase ADC clock. This will significantly increase total conversion time.

Freescale Kinetis devices use 16-bit SAR ADC with multiplexed analog inputs. Each ADC contains one sample and hold circuit. Kinetis K devices also include PGA (linear resistive operation amplifier) with selectable gain. The acquisition time is not dependent just on ADC clock. User can select from various options dependent on ADLSMP bit in ADCx_CFG1 register and ADLSTS bits in ADCx_CFG2 register. In such case, the total conversion time is not significantly affected by increased acquisition time. This feature is particularly useful in case of higher input impedance used.

NOTE
It is important to mention the difference between PGA used in Freescale DSCs and Kinetis devices. If PGA is used it can have significant influence on external RC component selection. Some of DSCs use PGA with switch capacitance gain amplifier which can have even higher demands on external RC components. The main reason is the PGA input capacitance which increases with the gain. On the other hand, the Kinetis devices use PGA based on linear resistive operation amplifier. This variant is less effective (higher silicon die) and has higher power consumption. However, it can help as impedance isolation between external RC components and sample/hold circuit. Sample and hold capacitance is charged by lower PGA output impedance and the external RC components are connected to PGA higher input impedance (from 32 K up to 128 K dependent on selected PGA gain). This can rapidly decrease demand on external RC components (higher impedance can be used).

3.1   Example 1 - DSC MC86F8257 with 12-bit cyclic ADC

In this example, the Freescale daughter board with the MC86F8257 was used and primarily intended for motor control applications. This example was set up to demonstrate proper selection and design of the external RC components required for ADC inputs.

The daughter board power was supplied from a battery source. The analog and digital circuits were powered by the same power supply. Most of the recommendations are satisfied except for the inductor (or ferrite) connected between the digital and analog power pins.

NOTE
It will be necessary to allow some margin in the experimental results due to the tolerances of the passive components that were used with the neglected parasitic components.

For this example, three single-ended channels with sequential sampling mode were used. The first and the third channel inputs were grounded and the second channel was connected to 3.3 V. The PGA gain was set to 1. The conversion time was set to 2.05 us, this means that the core frequency = 60 MHz which then requires a divisor of 6 which makes an ADC clock = 10 MHz (0.1 us), that is conversion time is equal to 8.5*0.1μs+6*0.1 us+6*0.1 μs = 2.05 μs.

The conversion is initialized by a sync pulse originating from the timer every 16.67 us (sampling frequency is 60 kHz). According to the ADC timing block diagram. See, *MC56F825x/4x Reference Manual* (document number MC56F825XRM), the acquisition time of the sample and hold circuit is half of the ADC clock, that is $T_{AQ} = 50$ ns. The ADC resolution in number of bits is 12. Considering the worst case (the second channel), the measured input voltage V_{IN} is set to V_{REFH}, that is $V_{IN} = 3.3$ V and initial voltage across sampling capacitance is V_{REFL}, that is $V_{CSH0} = 0$V (from the previous measurement). The full scale range is equal to 3.3 V, that is $V_{FSR} = 3.3$ V. With respect to the data sheet *MC56F825x/MC56F824x Digital Signal Controller* (document MC56F825X) the capacitance of the sampling capacitor for 1x gain of PGA is 1.4 pF. Capacitance is directly proportional to the PGA gain. All other parasitic capacitances were neglected. Following the recommendation for correct operation of the controller, no less than 33 p capacitor must be connected at each of the used ADC inputs. In a calculation minimum recommended resistance 10Ω is considered.

In the aggregate:
- $T_{AQ} = 50$ ns
- $C_{IN} = 33$ pF (minimum)
- $C_{SH} = 1.4$ pF
- $V_{IN} = 3.3$ V
- $V_{CSH0} = 0$ V
- $V_{FSR} = 3.3$ V
- N = 12

Using Eqn.10 for this example input resistance R_{IN} must not exceed the value given by:

$$R_{IN} \leq \frac{50 \text{nf}}{(33 \text{pF} - 1.4 \text{pF}) \ln\left(\frac{1}{1+\alpha} 2^{13}\right)} = 250\Omega$$

Equation 11

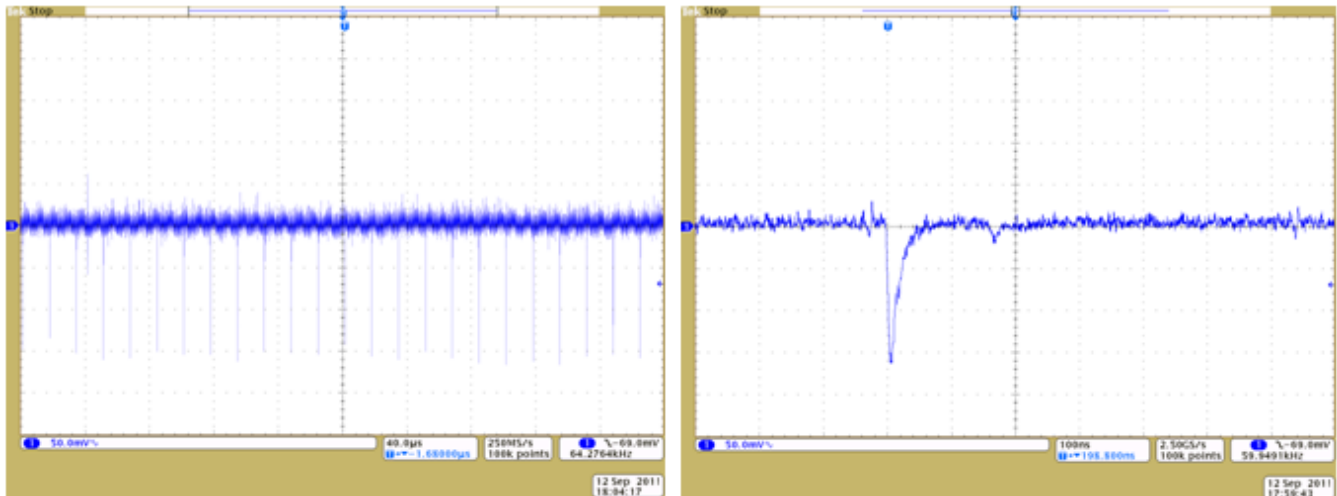The minimum recommended value of input resistance (10Ω) is satisfied. The value of α is given by Eqn. 4, That is:

$$\alpha = \frac{C_{IN}}{C_{SH}} = \frac{33}{1.4} = 23.6$$

Equation 12

The magnitude of the voltage drop (peak) across the input capacitor during sampling is defined by Eqn. 6 and in this case it is:

$$\Delta V = \frac{1}{\alpha+1}\left(V_{CIN0} - V_{CSH0}\right) = \frac{1}{\alpha+1}(3.3 - 0) = 134 \text{mV}$$

Equation 13

Figure 8. Correct acquisition time setting – digital result 4087 (time scale: left side 40 μs, right side 100 ns)

In Figure 8 the voltage drop across the input capacitor (taking into account the S/H circuit simplifications and all component tolerances) is big but does not cause any error in the digital output of the ADC. The digital result for the second channel measured by FreeMASTER is 4087.

A common mistake related to external RC component design is to increase input impedance by R_{IN} to reduce current or to make impedance isolation between the measured source and ADC. Now the same case is considered, except that the input resistance R_{IN} will be increased to10kΩ to demonstrate insufficient charging of sampling capacitor C_{SH} during the acquisition time. As can be seen in detail in Figure 9, the acquisition time of 50 ns is not sufficient to enable the sampling capacitance to charge correctly. The condition defined in Eqn. 9 is not satisfied and consequently, a big error in the second channel ADC digital output should be expected. The digital result for the second channel measured by FreeMASTER in this case was 3780. The result represents significant inaccuracy in the measurement. To get correct results, it is necessary to follow Eqn.10 and set the acquisition time higher than:

$$T_{AQ} \geq t_{II} \bullet \ln\left(\frac{(V_{IN} - V_{CSH0})}{(1+\alpha).V_{FSR}} . 2^{(N+1)}\right) \geq 2\mu s$$
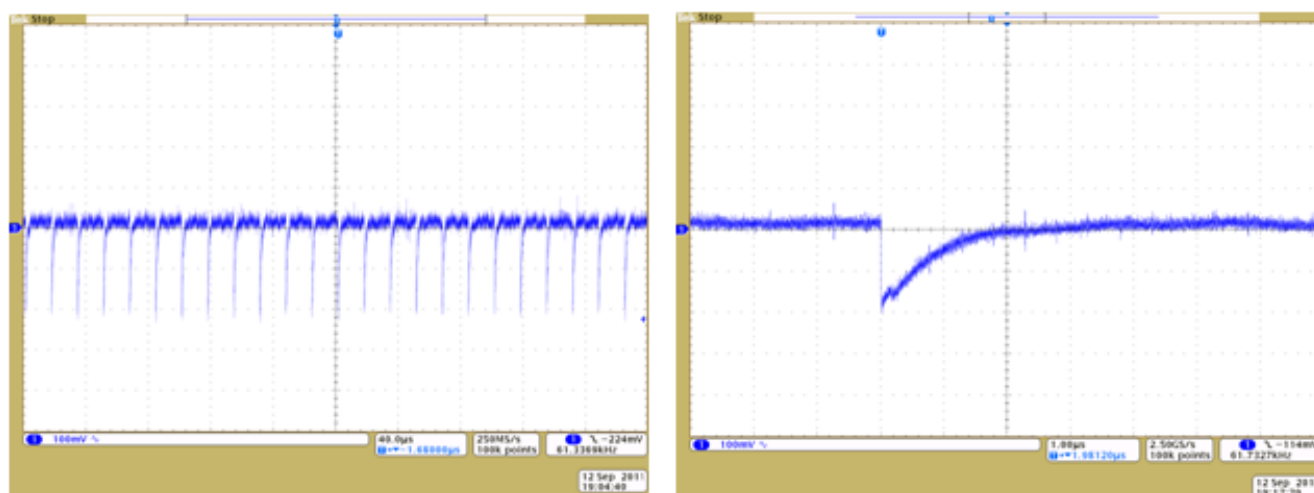
Equation 14

Figure 9. Incorrect acquisition time setting – digital result 3780 (time scale: left side 40 µs, right side 1 µs)

3.2   Example 2 - Kinetis K K70FN1M with 16-bit SAR ADC

In this example, the Freescale TWR-K70FN1M board is used. Similarly to the previous example, this example should provide proper selection and design of the external RC components required by SAR ADC used in Kinetis devices. The board is supplied from battery source to avoid any disturbances. TWR board uses linear voltage regulator to get 3.3V supply. Opto-isolation is used for communication with PC. The analog power part (V_{DDA}, V_{SSA} as well as V_{REFH}, V_{REFL}) is separated from digital part (V_{DD} and V_{SS}) using ferrite beads (100Ω@100MHz). This can significantly reduce high-frequency components coming from digital part. Hence, most of the recommendations mentioned in theoretical background are satisfied.

NOTE
It is necessary to consider that Freescale tower system boards are targeted to general usage. So, some deficiency related to PCB design of analog signals tracing can be expected.

Example

The analog signal measurement is performed by one ADC (ADC0). The ADC0 converter converts two single-ended channels in sequence. The PDB module is configured in back-to-back mode to proceed two conversions in sequence (it means PDB_CH0 pretrigger 0 starts conversion of ADC0_CHA and conversion complete flag of that channel acknowledges PDB_CH0 pretrigger 1 to start conversion of ADC0_CHB directly in sequence). The ADC0_CHA is connected to channel AD30 which represents V_{REFL}. The ADC0_CHB is connected to channel DAD0 (single-ended ADC0_DP0). The input pin of the channel ADC0_DP0 is connected to V_{DDA} through external RC components (see in Figure 10).

NOTE

Some of the parameters names presented in this document differs from the datasheet parameters names. For example: $R_{IN} = R_{AS}$ (as analog source resistance), $C_{IN} = C_{AS}$ (analog source capacitance), $R_{SH} = R_{ADIN}$ (as input resistance) and C_{ADIN} (as input capacitance).
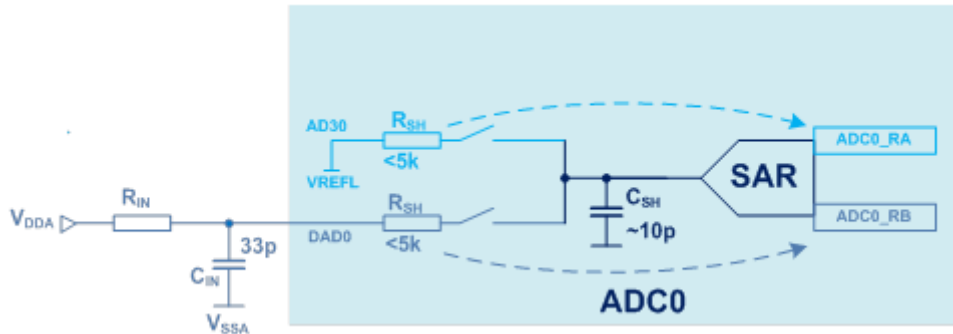
Figure 10. Block diagram of the circuit

The ADC module in this example is configured for the fastest conversion in 16-bit mode. The fastest conversion means that the ADC clock is set to 12 MHz, the acquisition time (or sample time) is set shortest as possible (ADLSMP = 0, ADLSTS = 3, ADHSC = 1) and hardware averaging is disabled. It is necessary to configure BUS clock to 48 MHz to achieve maximum ADC clock 12 MHz for 16-bit mode. The PGA module is disabled in this example. The total conversion time in such case is ~2.7μs (see also [5]).

The conversion start is triggered by a PDB channel 0 pretrigger 0 pulse every 25 μs (sampling frequency is set to 40 kHz). Considering ADC configuration mentioned before the acquisition time is set to T_{AQ} = 6xADCK cycles = 500ns (see chapter Sample time and total conversion time in [4]). The worst case of sampling is considered, it means the second measured channel (ADC0_DP1) is connected to the V_{DDA}, the measured input voltage V_{IN} = 3.3 V. The initial voltage across sampling capacitance is V_{REFL} that is, VCSH0 = 0V (from previous measurement). The full scale range is equal to 3.3V that is, V_{FSR} = 3.3V. The maximum capacitance of sampling capacitor is 10pF (see C_{ADIN} in [6]).

NOTE

The sampling capacitance defined in datasheet [6] as input capacitance C_{ADIN} represents total capacitance of the bank of capacitances implemented in SAR ADCs with redistribution charging. Each capacitor in the bank should be charged by the measured input pin voltage during acquisition time. During the rest hold and successive approximation time (conversion steps) the energy stored in each capacitance is charged/discharged to V_{REFH} accordingly to the particular sequence of binary weighted principle.

There is no restriction for the input capacitance C_{IN} (or as in datasheet C_{AS}) value provided in datasheet [6]. Hence, the same value as in previous example is used C_{IN} = 33p. All other parasitic capacitances were neglected. Now all parameters required for proper external RC components calculation are known.

In the aggregate:
- T_{AQ} = 500 ns
- C_{IN} = 33 pF
- C_{SH} = 10 pF
- V_{IN} = 3.3 V
- V_{CSH0} = 0 V

- $V_{FSR} = 3.3$ V
- $N = 16$

Using Eqn.10 for this example input resistance R_{IN} must not exceed the value given by:

$$R_{IN} \leqslant \frac{500\text{ns}}{(33\text{pF}+10\text{pF})\ln\left(\frac{1}{1+\alpha}2^{17}\right)} = 1126\,\Omega$$

Equation 15

The calculated resistance represents the maximum resistance which can be applied to the analog input pin without losing any digital result accuracy by sampling. Using higher value of resistance will result in incorrect data conversion. The datasheet provided the maximum value of 5kΩ but for the different case (12/13-bit resolution mode, lower ADC clock). Using equation (4) the value of α is calculated as:

$$\alpha = \frac{C_{IN}}{C_{SH}} = \frac{33}{10} = 3.3$$

Equation 16

Estimated magnitude of voltage drop (peak) across input capacitor during sampling is defined by equation (6) and in this case it is:

$$\Delta V = \frac{1}{\alpha+1}(V_{CIN0} - V_{CSH0}) = \frac{1}{3.3+1}(3.3 - 0) = 767\text{mV}$$

Equation 17

In Figure 11 is shown the waveform of the voltage across the input capacitance for currently calculated parameters.

NOTE
The waveforms obtained by oscilloscope shows just AC component of the analog pin voltage and should have only informative character considering oscilloscope probe influence, especially the probe capacitance which is around 8 pF.

As can be assumed from the Figure 11, the sampling capacitance charging process is finished in 500 ns of acquisition time. Hence, the accurate digital data should be expected in result register. The digital result of ADC0 channel DAD0 is stable at **65535 (this represents 0 digits of deviation from ideal case – no error)**.
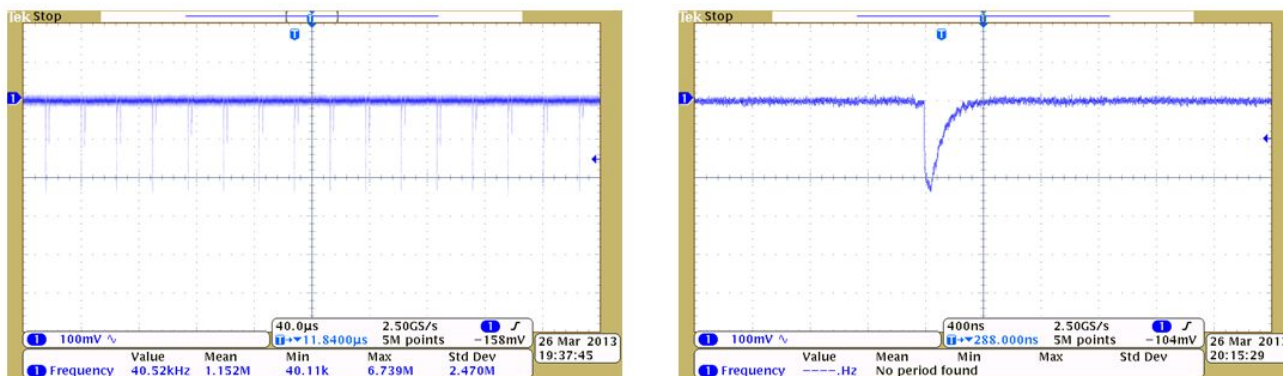
Figure 11. Correct acquisition time setting – digital result 65535

As mentioned in the previous example, the common mistake is to increase input resistance R_{IN} in order to reduce current or to make impedance isolation etc. The Figure 12 shows waveforms when input resistance is increased from 1.1 kΩ to 5.1 kΩ. It is clear from the Figure 12 that the process of charging of sampling capacitance is not accomplished in 500 ns of acquisition (sample) time. Hence, the digital data stored in result register cannot be correct. The digital result of ADC0 channel DAD0 obtained from is unstable around 64750, which represents very high deviation from expected digital result of **65535 (this represents 785 digits of deviation from ideal case – 1.2% error)**. This result can in some cases lead in fatal application failure. In order to get correct results, it is necessary to follow equation (9):

Cookbook for SAR ADC Measurements , Rev 1, 04/2014

$$T_{AQ} \geq \tau_{11}.\ln\left(\frac{(V_{IN}-V_{CSH0})}{(1+\alpha).V_{FSR}}.2^{(N+1)}\right) \geq 2,2\,\mu s$$
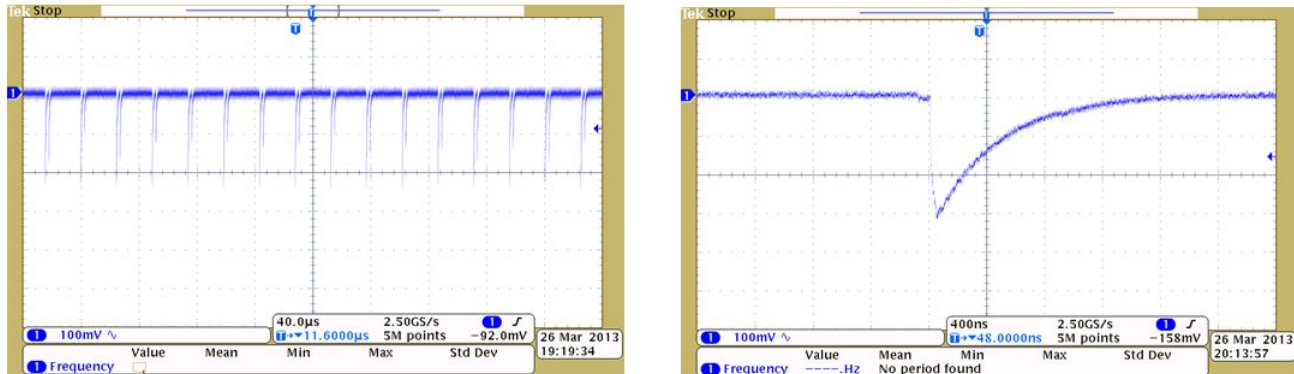
Equation 18

Figure 12. Incorrect acquisition time setting – digital result ~64750

4 Conclusion

During the acquisition time (T_{AQ}), the sampling capacitor (C_{SH}) must be charged to an acceptable minimal portion of the voltage level of the measured input voltage. In general, the deviation from the measured input voltage at the end of acquisition time must not exceed 0.5 LSB of the full scale range. If higher input impedance R_{IN} is used (high external component time constant), then the sampling capacitor (C_{SH}) is quickly charged at first by the energy of the external input capacitor (C_{IN}) (much lower input components time constant). The process of charging the sampling capacitance causes a voltage drop (or peak) across external input capacitor C_{IN}. The subsequent process of charging the sampling capacitor is much slower due to this higher input impedance. The acquisition time must be properly set while considering the time constant of the sampling capacitor charging. Hence, the external RC components essentially affect the AD conversion accuracy. To achieve optimal performance from an ADC, special care must be taken to select and design appropriate external RC components, in addition to meeting all other requirements, see *MC56F825x/4x Reference Manual* (document number MC56F825XRM) and *MC56F825x/MC56F824xDigital Signal Controller* (document MC56F825X).

5 References

Following documents are available on freescale.com :
- *MC56F825x/4x Reference Manual*, Rev. 2, 10/2010 (document MC56F825XRM)
- *K70 Sub-Family Reference Manual*, Rev. 2, Dec 2011 (document K70P256M150SF3RM)
- *MC56F825x/MC56F824x Digital Signal Controller*, Rev. 3 (document MC56F825X)
- *Data Sheet K70 Sub-Family*, Rev. 3, 3/2012 (document K70P256M150SF3)
- *Nyquist–Shannon sampling theorem*, wikipedia.org
- *ADC calculator for Kinetis devices*, freescale.com

6 Revision history

Revision number	Date	Substantial changes
Rev 0	11/2011	Initial release

Table continues on the next page...

Cookbook for SAR ADC Measurements , Rev 1, 04/2014

Revision number	Date	Substantial changes
Rev 1	04/2014	Added section Example 2 - Kinetis K K70FN1M with 16-bit SAR ADC

Document Number: AN4373
Rev. 1, April 2014