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EMC Design Considerations for MC9S08PT60

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Contents

1 Introduction

There is an increase in the use of electronic and programmable electronic devices such as the microcontroller. Therefore, paying more attention to the Electromagnetic Compatibility (EMC) of a full system at the beginning of a design phase is becoming one of the major technical issues. If it is ignored early in the design cycle, fixes become very expensive. EMC problems on a printed circuit board (PCB) can be solved at the layout stage and at a relatively lower cost. The EMC is now considered at the beginning of the design cycle. Figure 1-1 shows the cost for the EMC fix after the production phase which is high and a lot of time is spent on engineering fixes.

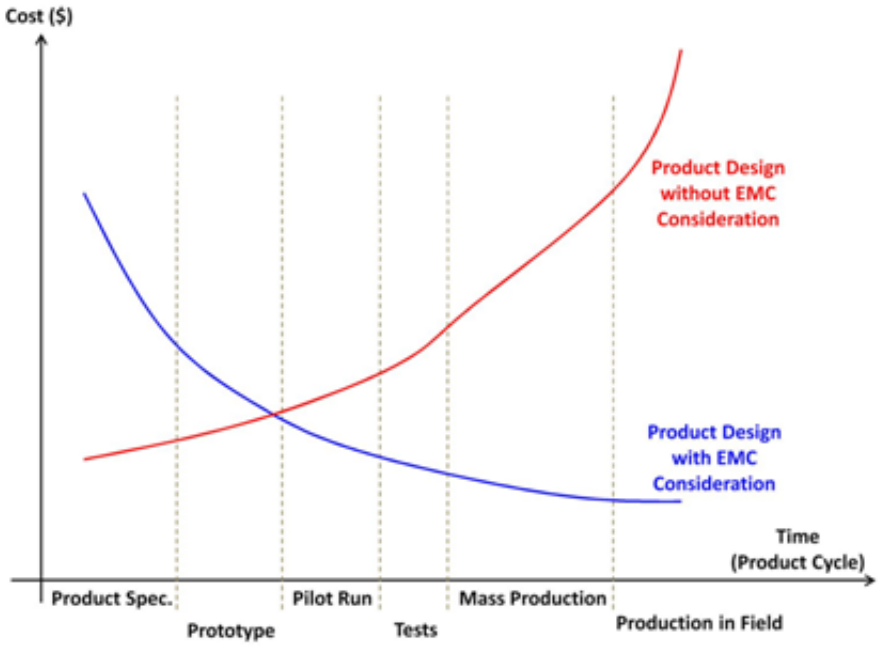

Figure 1. Cost of EMC fixing

Good practice of EMC consideration such as component selection, circuit design, PCB layout, and system and product design can provide inherent EMC performance. This document introduces some EMC basic concepts in section B and the use of a real case PCB layout example to explain how to achieve good EMC performance during the design phase.

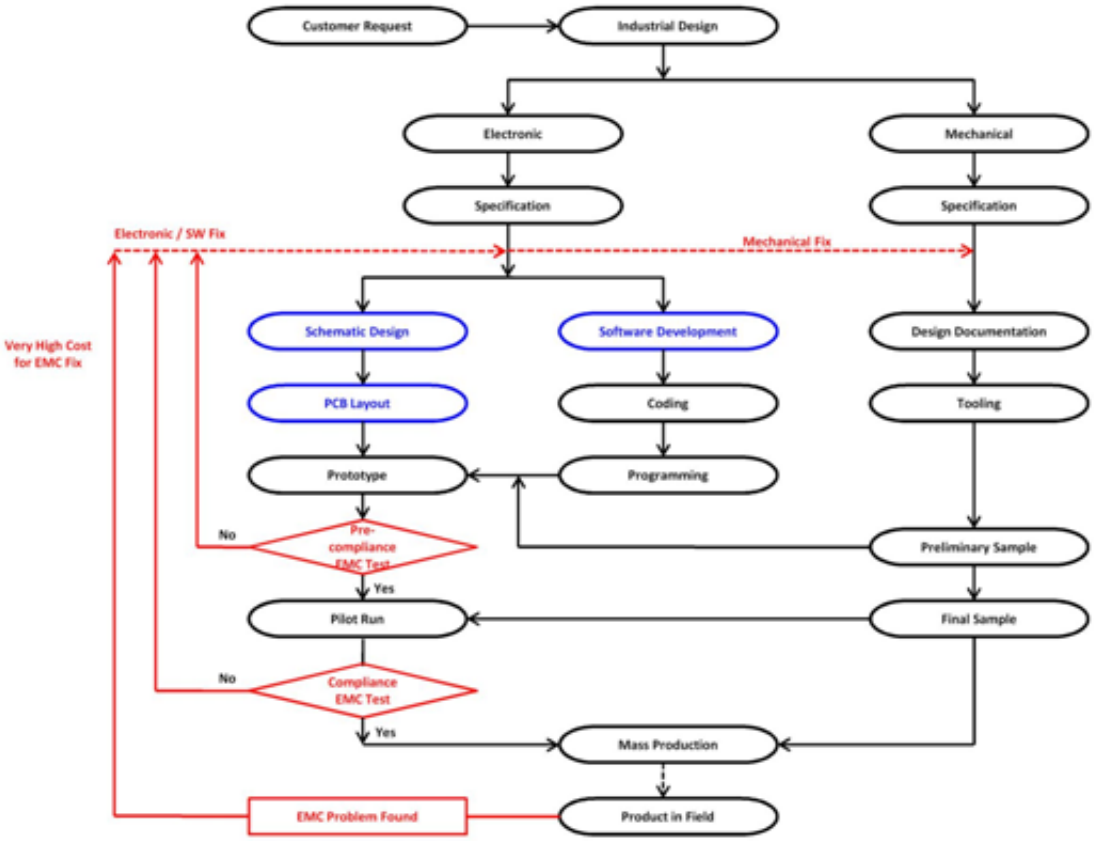

Figure 2. Product design flow

Figure 2 shows the typical product design flow. The cost of the EMC is high if attention is not given at the beginning of the schematic design, software development, and PCB layout. In a worst case scenario, the mechanical casing design is changed to let the product pass the EMC compliance test particularly for the air discharge ESD test.

2 Basic Concept

This section introduces the most important concept related to the EMC PCB board design .

2.1 EMI model

One of the basic concepts in EMC consideration is explained by the EMI model.

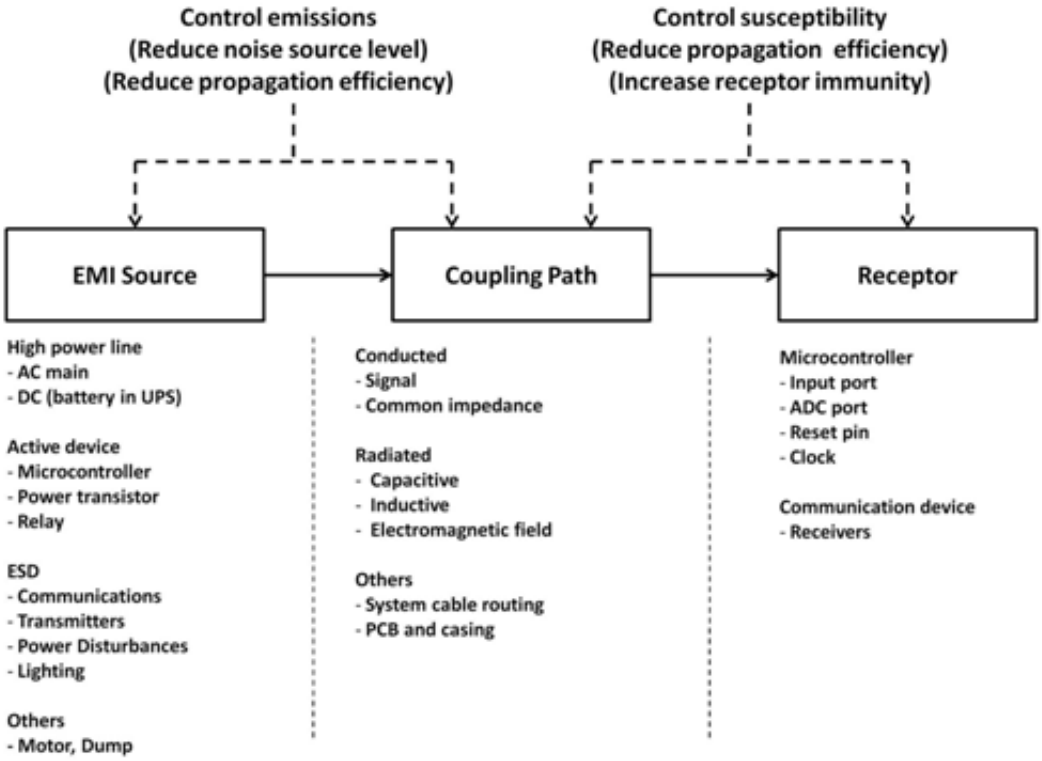

Figure 3. EMI model

Based on this model, there are three ways to fix the EMC problem —

- Reduce the noise from the EMI source
- Minimize the coupling effectiveness in any coupling path (conducted or radiated)
- Increase the immunity of the receptor

In board level consideration, MCU acts as the receptor. Traces in the PCB layout provide the coupling paths, and internal or external noises act as the EMI sources. Using a good immunity performance MCU, designing a good PCB layout to reduce the level of coupling, and preventing any internal or external noise that affects the system are helpful actions that increase the overall system EMC performance.

In system level consideration, the board acts as the receptor. The board and cable placement act as the coupling paths. The motor, pump, and high-current device (load) act as the EMI sources. A good PCB layout can help to increase the immunity of the receptor, a proper board and cable placement reduce the coupling effectiveness, and the use of the lower noisy load minimize the noise source. All of these affect the EMC.

2.2 Passive component in EMC

Understanding the characteristic of a passive component in high frequencies and its frequency response can help a hardware circuit designer, PCB layout designer, and software engineer to avoid or minimize a potential EMC problem.

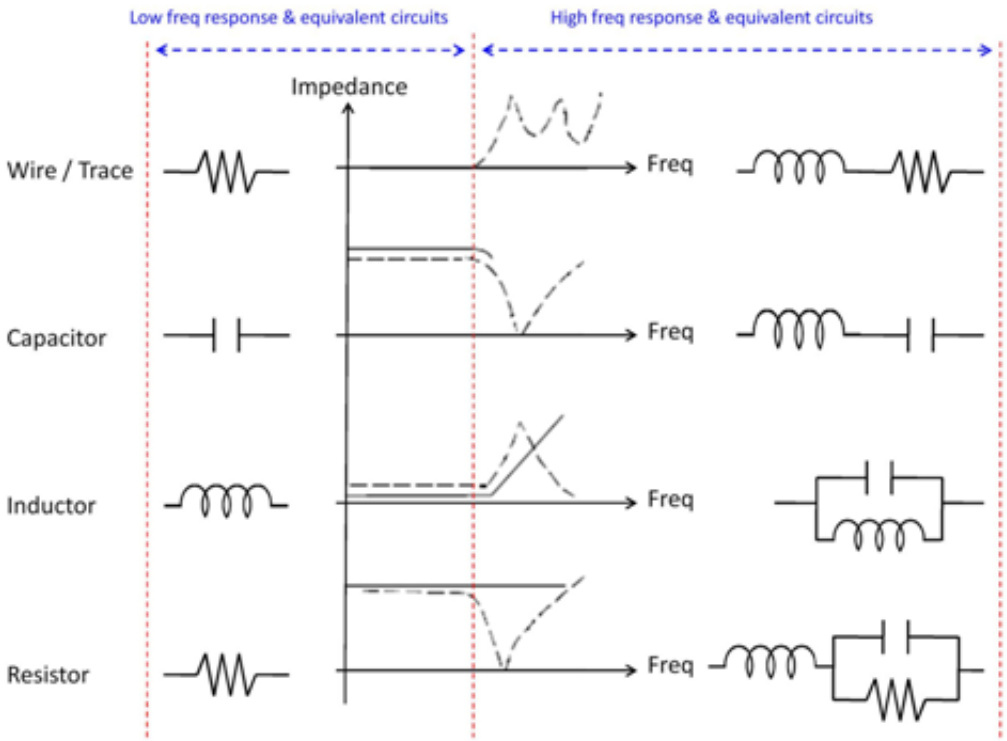

Figure 4. Passive components non-ideal behavior in high frequencies

2.3 Ground system

The ground system is one of the important elements for board and system level EMC consideration. Providing a low inductance ground system is the target to improve immunity of the PCB or system.

In the PCB layout, there are three types of ground layout structures:

- In the PCB layout, there are three types of the ground layout structures:
  - Minimal ground—Minimal ground connects the ground points on the PCB randomly. In this case, high inductance of the ground points are created under high-frequency operation.
  - Grid ground—Grid ground is achieved by connecting vertical and horizontal ground traces on both sides of PCB through the via. It provides related lower inductance ground (between minimal ground and ground plane) paths for current to return to its source
  - Ground plane—Ground plane is the best ground layout technique to provide the lowest inductance ground. Maximizing the ground plane reduces the inductance, improves the immunity, and also provides shielding of the PCB.

For a double or multi layer PCB, a ground plane technique is recommended. It provides the lowest impedance conductor and paths for current return to its source.

For a single or high density double layer PCB, it is impossible to use ground plane, consider use of the grid ground. In a single-layer board, the grid is formed by jumper wires.

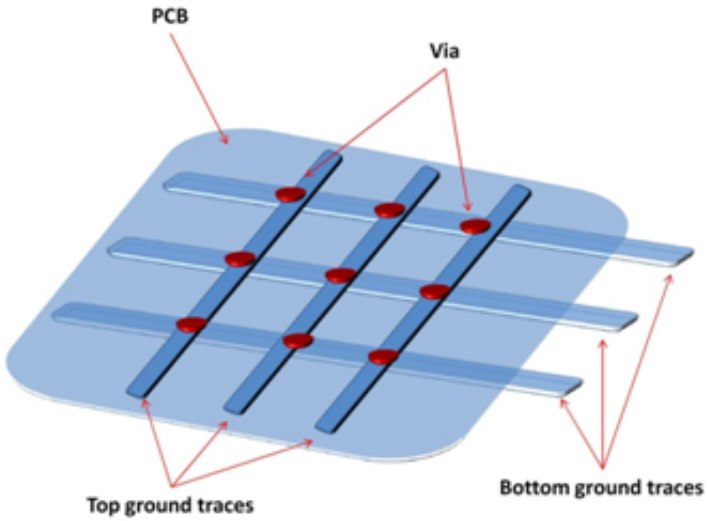

Figure 5. Grid ground structure

To control the inductance of the ground, the grid spacing must be smaller than 500 mils (1 inch = 1000 mils); the width of the ground traces should be greater than 40 mils. The thickness of the PCB trace also needs to be considered (that is, a 1 oz. copper PCB is around 1.4 mils thick). Inductance is proportional to frequency. This means that the higher the ground impedance is off the ground the higher the frequency is.

As mentioned before, ground inductance generates ground noise. This is why the ground plane is recommended instead of the minimal ground structure. When high frequencies pass through the large inductance conductor/trace in minimal ground system, they generate voltage drops and radiated emission will be occurred from the PCB and those ground noise voltage not only to force EMI current to flow out of the PCB but also affect other device on the PCB.

Besides the minimal ground, grid ground and ground plane structures. There are three different signal ground methods for PCB layout. Single-point ground, multi-point ground and hybrid ground.

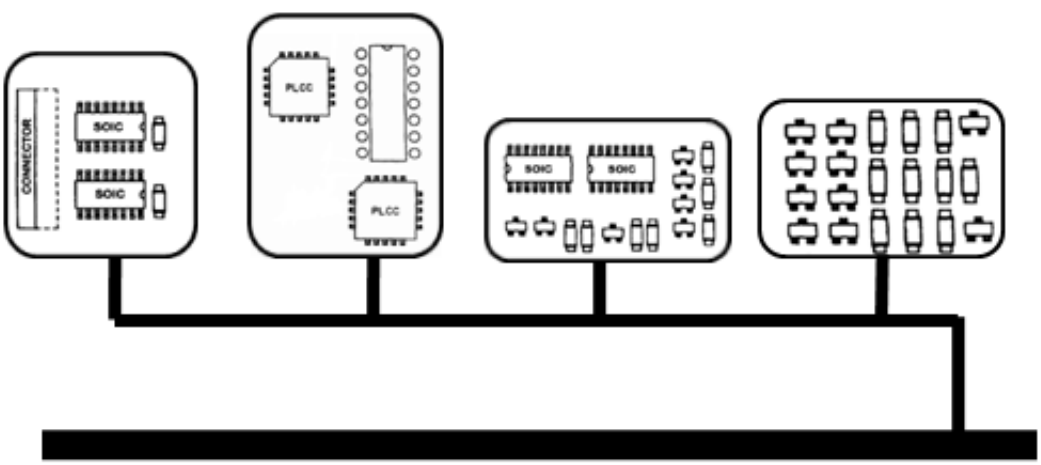

Figure 6. Single-point grounding connections

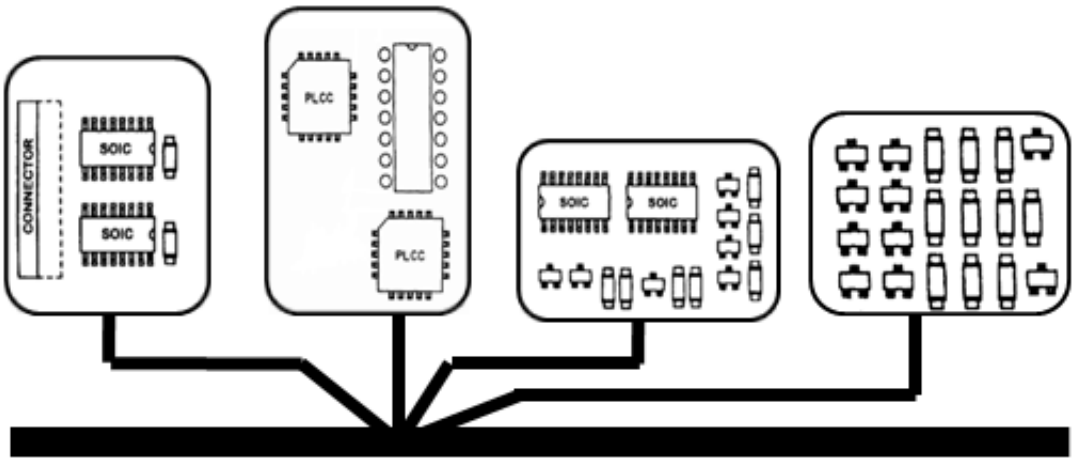

Figure 7. Multi-point grounding connections

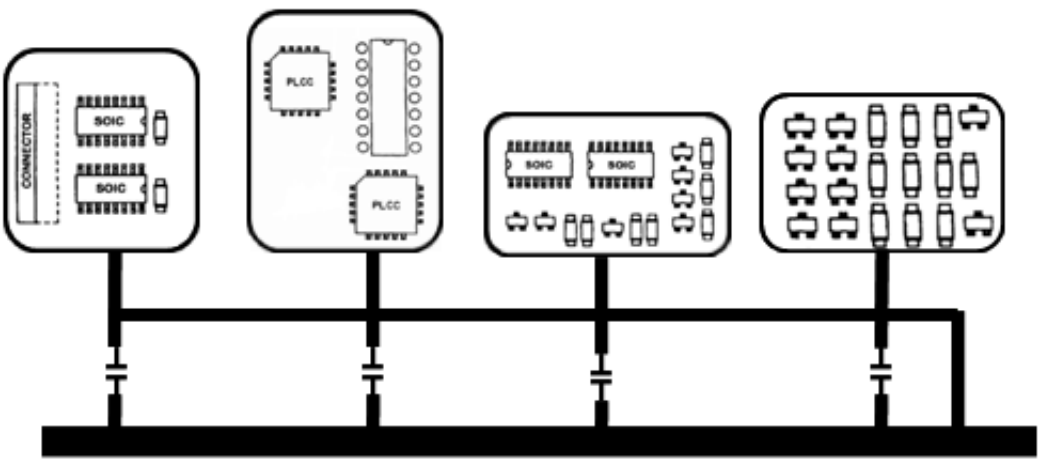

Figure 8. Hybrid grounding connections

In general, single-point ground is suitable for 1–10 MHz circuitry to minimize the impedance, the length of the ground trace is suggested to be less than 1/12 wavelength. For high speed circuitry, a multi-point ground is more suitable. It provides very low ground impedance, but avoid using it in low frequency. To archive different circuitries in the same board the hybrid ground provides a single-point ground at a low frequency while a multi-point ground provides it at high frequencies.

2.4 Characteristic of digital signal

Although digital circuits provide a high noise margin they also generate many EMC/EMI problems due to its high bandwidth, high speed clock, and edge rates. Digital signal behavior is needed to design a good EMC performance PCB board in the digital system.

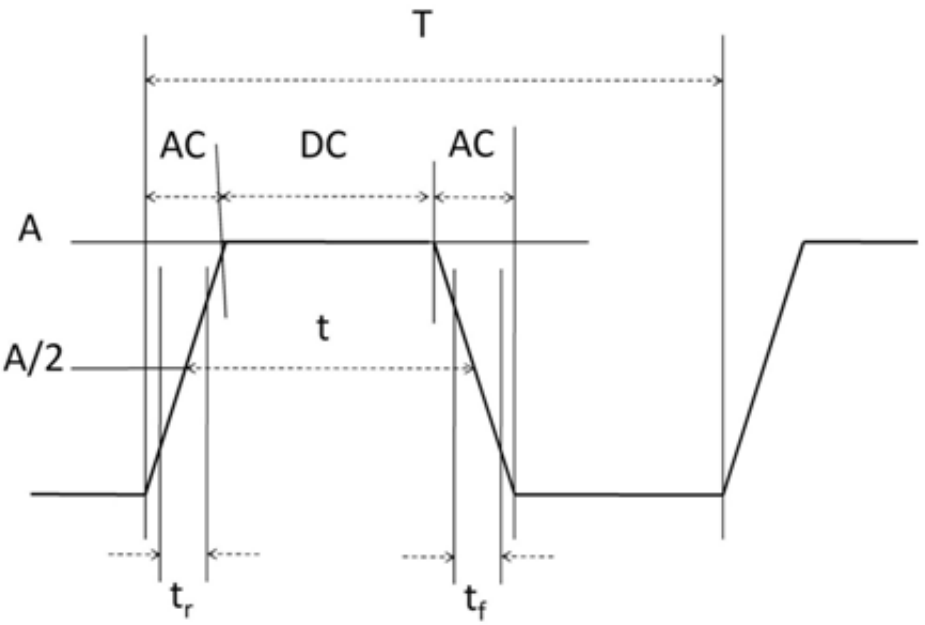

Figure 9. Time dominant characteristics of digital signal

Figure 9 shows the digital signal square waveform. There are AC components during the transition and DC components during the steady state. The AC current contains all frequency components (fundamental and harmonic frequencies). This means that the digital signal with a fundamental frequency of 8 MHz has harmonic frequency components of 16, 24, 32, 40 MHz, and so on. The corresponding signal spectrum is shown in Figure 10. In the diagram over 90% of the spectral energy of the signal is contained within the bandwidth (BW).

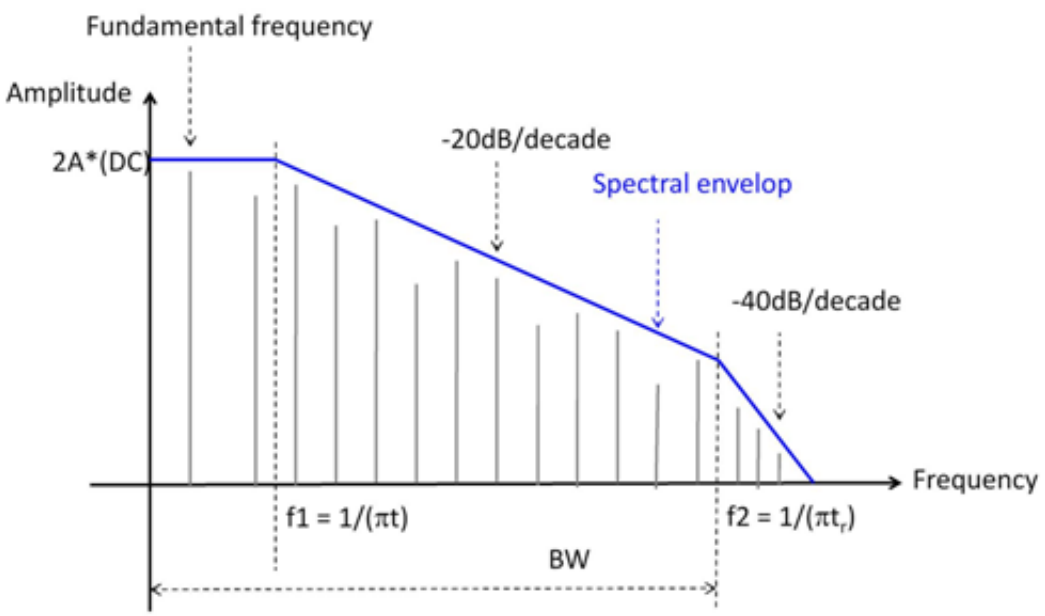

Figure 10. Frequency dominant characteristics of digital signal

The relationship between the time and the dominant frequency of the digital signal shown in Figure 9 and Figure 10 can be considered below equation 1 if $t_r = t_f$.

Eqn.1

$$BW = 1/(\pi t_r)$$

Where BW is the bandwidth of the digital signal shown in Figure 10 and t_r is the rise time of the digital signal shown inFigure 9.

In this equation, an increase in the rise time (t_r) of the digital signal reduces the bandwidth (BW). As a result, reduce the spectral energy of the signal or reduce the sum of the harmonic current of the signal (that is reduce the noise source).

2.5 Interference coupling

There are three different types of coupling between circuits:

- Common impedance coupling
- Capacitive coupling
- Inductive coupling

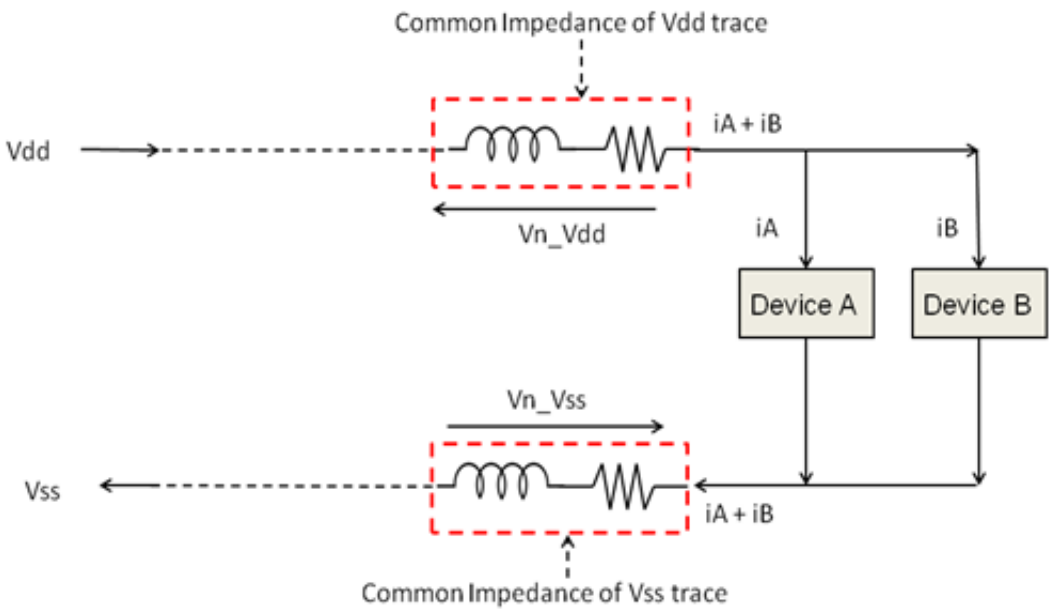

Figure 11. Common impedance coupling model

In Figure 11, two devices or circuits connected with the same V_{dd} and V_{ss} traces. The common impedance coupling means two or more circuits share a common trace to source or sink current. The problem is it creates a path of interference between those circuits. Any change in the current of device A causes the potential change on both common impedance ends (V_{dd} and V_{ss}) and it will affect device B. This is the same case when there is any current change in device B. Many EMC problems in the PCB and MCU are caused by this type of coupling. Reduce the inductance of power and ground traces, isolate devices A and B by decoupling, bypassing and layout technique can eliminate this type of coupling.

Localized the pull-up and pull-down resistors and filtering capacitors for a different device (MCU) is one method to minimize this type of coupling effectively. Reduce the common mode impedance (enlarge the trace width and use of the ground plane) can also minimize this type of coupling.

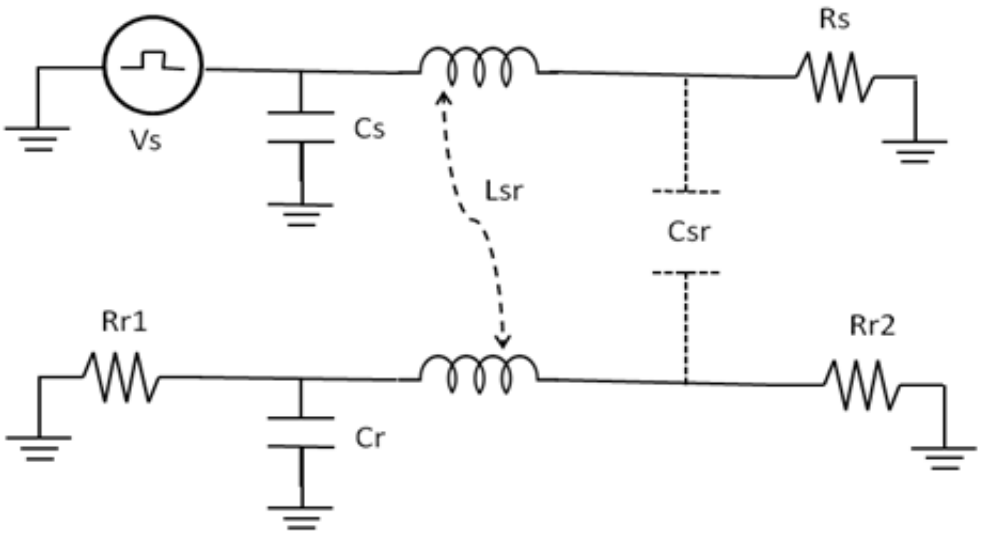

Figure 12. Inductive and capacitive coupling model

Figure 12 shows the inductive and capacitive coupling between two circuits. Both capacitive and inductive coupling are due to mutual capacitance (Csr) and inductance (Lsr) between the circuits (generator and receptor).

On the generator side, the signal voltage passes through the PCB trace to its load. The electric field is also generated along with the PCB trace. This time-varying electric field is be coupled to the PCB trace in the receptor side through the mutual capacitance between them. It induces the noise voltage in the receptor circuit. The noise voltage due to the capacitive coupling is shown as in:

Eqn2.

$$Vn = j\omega RrCsrVwhereRr \ll 1/\ j\omega(Csr + Cr)$$

and

Eqn3.

$$Vn = (Csr/Csr + Cr)\ Vs \text{ where } Rr \gg 1/\ j\omega(CSR + CR)$$

Where Rr = (Rr1 // Rr2)

Based on equation 3, minimize the capacitive coupling by following these recommendations:

- Reduce the generator frequency (lower clock frequency)
- Reduce the length of parallel traces for a sensitive circuit and noisy circuit
- Increase the physical separation between those circuits
- Place both traces with orthogonal basis
- Increase Cr and reduce Rr
- Apply shielding between two circuits
- Place the traces over the ground plane (mutual capacitance is reduced significantly if the traces are placed over the ground plane)

In inductive coupling, the circuit is considered the transformer. The generator circuit is primary while the receptor circuit is the secondary.

On the generator side, the signal voltage passes through the PCB trace to its load and the magnetic field is generated along with the PCB trace. This time-varying magnetic field is coupled to the PCB trace on the receptor side through the mutual inductance between them and induces the noise voltage on the receptor circuit. Unlike the capacitance coupling (high frequency only), both low and high frequencies are coupled into the receptor. High and fast transient current must be avoided in inductive coupling circuits particularly in low impedance circuits.

The noise voltage due to the inductive coupling is:

Eqn4.

$$Vn = j\omega BA\cos\theta$$

Where B is the magnetic flux density (Weber/cm2)

A is the receptor circuit area (cm2)

θ is the angle between the generator and receptor circuit

Based on equation 4 minimize the inductive coupling by following these recommendations.

- Reduce the generator operating frequency and rate of change of its current (that is di/dt)
- Reduce the area (ground return path) in generator and receptor circuits
- Reduce the parallel length between generator and receptor circuits
- Increase the physical separation between those circuits
- Place both traces with orthogonal basis
- Twist the generator return path loop
- Apply shielding between two circuits
- Place the traces over the ground plane (current return path)

2.6 Decoupling bypassing

Better understanding of decoupling and bypassing is needed to avoid wrong implementation for EMC problems.

Bypassing is to reduce the high frequency current flows in an impedance path by shunting that path with a bypass capacitor. Decoupling is to isolate noise between circuits on its common line.

The common line such as the power trace is the connection from a voltage regulator to the load (MCU). When the MCU is operating, the time varying current demand creates a noise voltage across the power trace inductor. To reduce the noise, reduce either the inductance of the power trace or the rate of the current change (di/dt). Therefore, the use of the power and ground planes to reduce the inductance and the use of the bypass capacitor to reduce the rate of change of the current are critical to avoid the noise propagate along the common line.

To ensure the proper use of the bypassing technique to provide the high frequency low impedance path of varying currents from the load that shares as little inductance as possible with power supply lines, it is important is to ensure the flow current from a load to the supply (that is a return path) that cannot be shared with any other circuit. It is also important to reduce noise coupling into the circuit particular in the circuit with the MCU to minimize the area of the return path loop.

The bypass capacitor can reduce the rate of the current change (di/dt), and mutual couplings (in Figure 12) can cancel the inductance between the forward and return paths, for example signal and power traces, signal and ground traces, and power and ground traces. When two traces are placed closely, the coupling between forward and return paths cause the voltage generated in the self-inductance of one path to be cancelled by the voltage induced from the coupling of the other path.

To prevent noise from one circuit propagate to other circuits through the power trace, place a decoupling capacitor it reduces the amount of shared supply currents between them. This is to avoid the common impedance coupling between two circuits already mentioned before.

3 PCB Layout Guideline for the MC9S08PT60

The need of a PCB layout consideration at the beginning of the product design phase and some fundamental concepts related to the PCB layout design for EMC / EMI compliance has already been introduced. The microwave oven control board is the use case to show how to implement the board design with EMC / EMI good practice, this explains the layout concept for EMC / EMI compliance.

3.1 Single layer double side loading PCB

For cost consideration, most of the home appliance (HA) manufacturers use the single-layer double-side loading control board for their products.

Although a single-layer double-side loading PCB can reduce the cost of the control board, it is more challenging than a double-layer and multi-layer PCB because of its design flexibility.

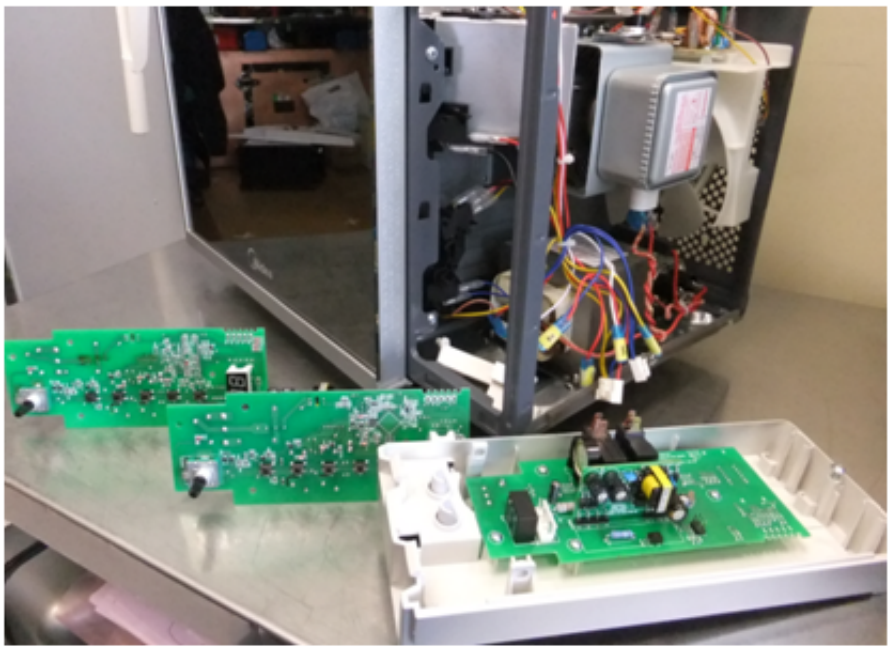

Figure 13. PT60 Control board for microwave system

Figure 13 shows the MC9S08PT60 (PT60) control board and the microwave oven. During the mechanical product design, the board size is fixed. The control board is implemented by a single-layer, and double-side loading with a separate switch mode power supply daughter board mounted vertically.

There are many constraints in the board design such as the size limitation, low cost concern, fixed position of push buttons location, LED 7-segment display and rotary encoder. The following sections show you how to implement the PCB layout for good EMC practice under such bounded conditions.

3.2 Placement methods

Figure 14 shows the control board placement. Since it is a single-layer, double-sided loading board, and needs to fulfill the product design requirements. Here is the list of mechanical constraints.

- Screw hole position is fixed
- Vertical mounted separated SMPS board
- Separated high-power AC main circuitry and low power DC circuitry.
- Placement of the push buttons, LED 7-segment display and rotary encoder are fixed.
- Except the SMD, push buttons, LED 7-segment display, and rotary encoder, all others components must be placed on the TOP side.

By fulfilling all of the above constraints, the components placement on the board is shown in Figure 14 which requires a lot of effort to finalize the acceptable version.

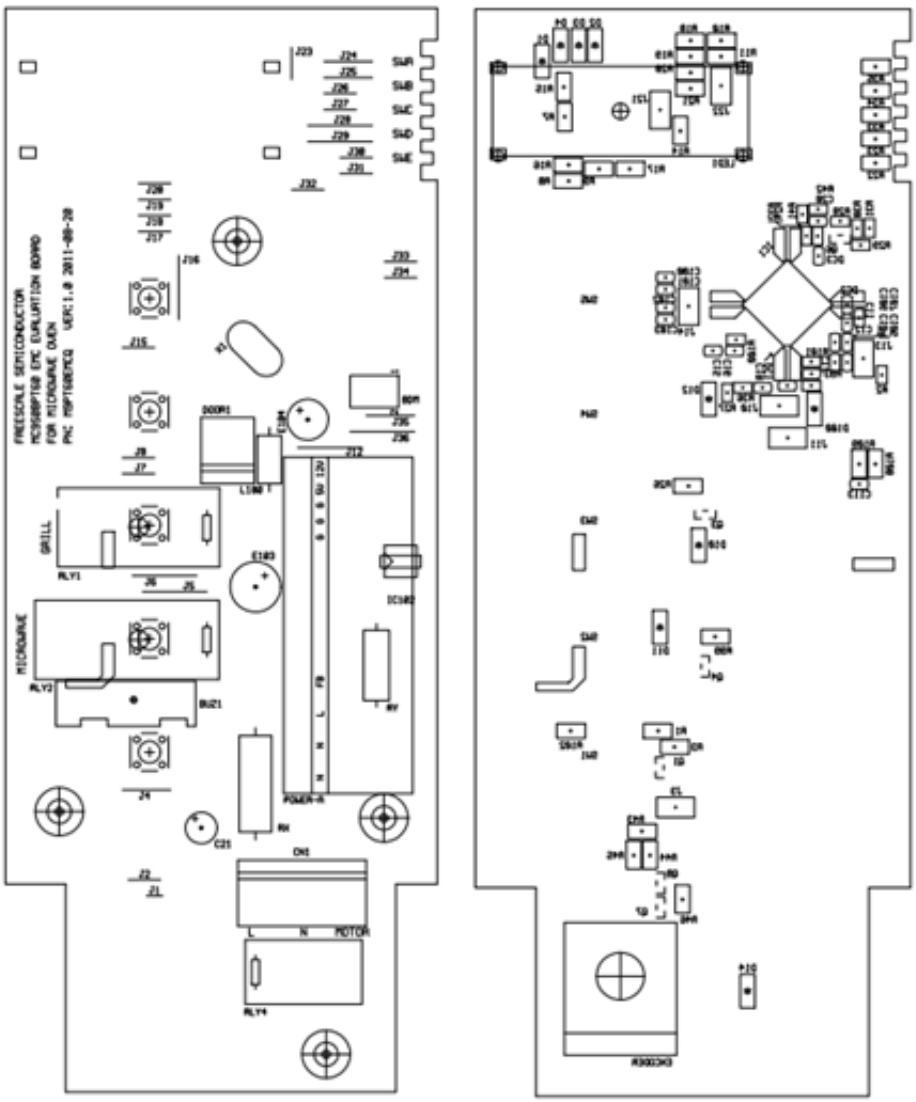

Figure 14. Component placement

The first EMC technique is how to select the critical components that need to be placed near the MCU. To consider the ground system, common impedance coupling and input port of the MCU is more sensitive with external noise, you need to minimize the ground and power loops area as well as the impedance of the power and ground. Therefore, the first step is to identify all components that connect to the MCU input ports which are also connected to power or ground. Those critical components are shown in Figure 15.

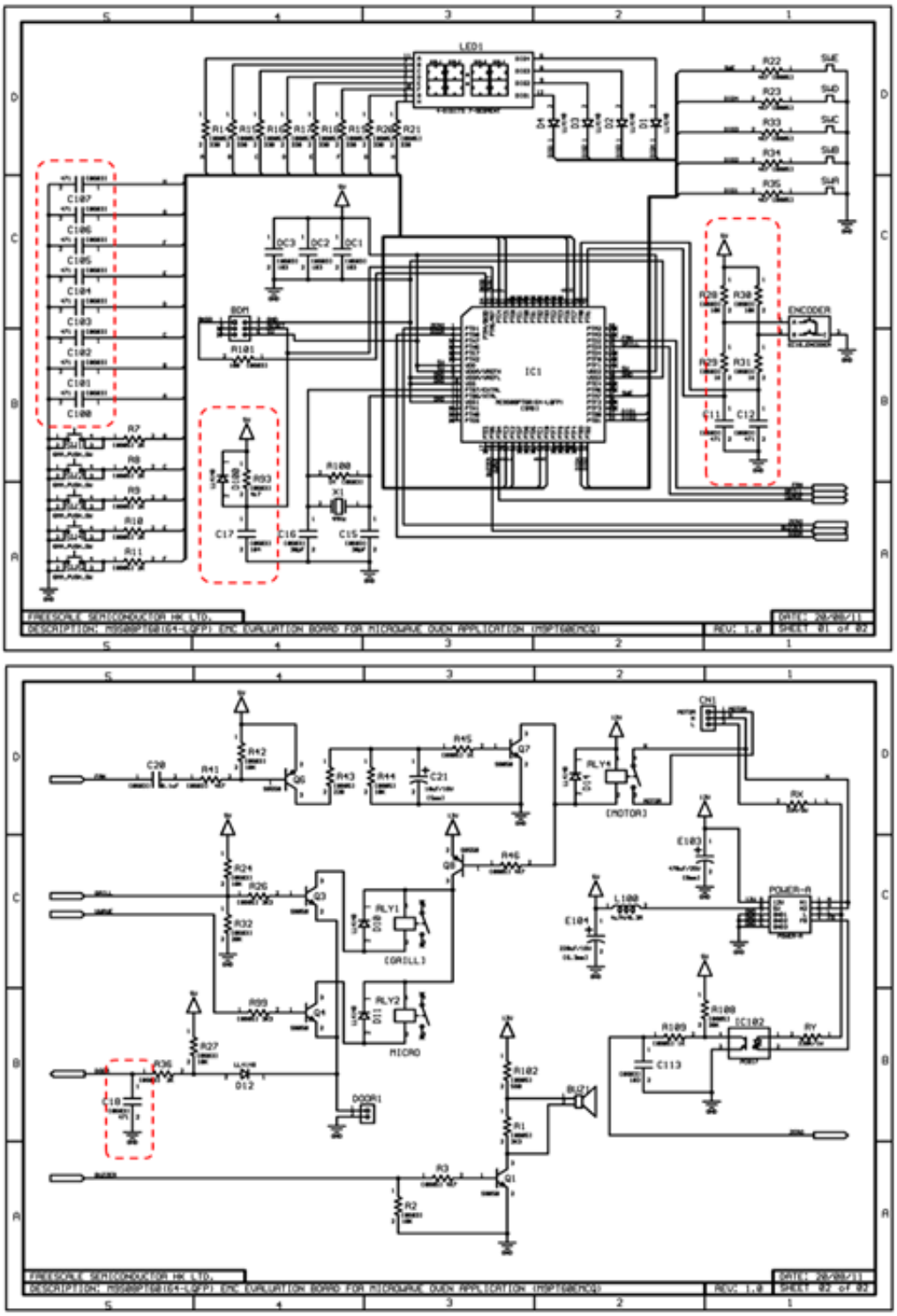

Figure 15. Critical component selections for placement

As a result those critical components are placed near the MCU as in Figure 16. The advantage of such placement can minimize both power and ground loop areas and reduce common impedance coupling such as power and ground. This thoroughly studied placement increases the EMC performance of the board and the system.

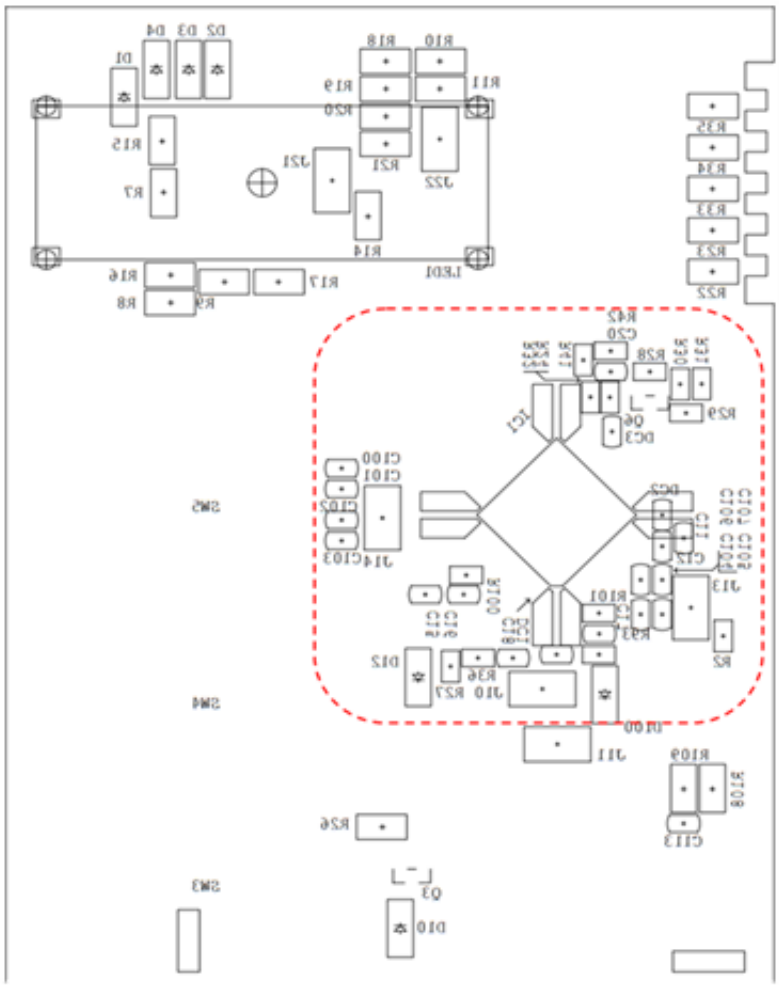

Figure 16. Selected critical component and place them near the MCU

3.3 Power supply board

Section B discussed the reason to reduce the loops area of the return path. In the power supply board, the current is large compared with the other circuit so more attention in the PCB layout is needed to minimize the noise generated from the board. Figure 17 shows the loops consideration and Figure 18 shows the PCB layout implementation. This is not only to minimize the loops but also to consider the isolation between AC and DC portion of the switch mode power supply.

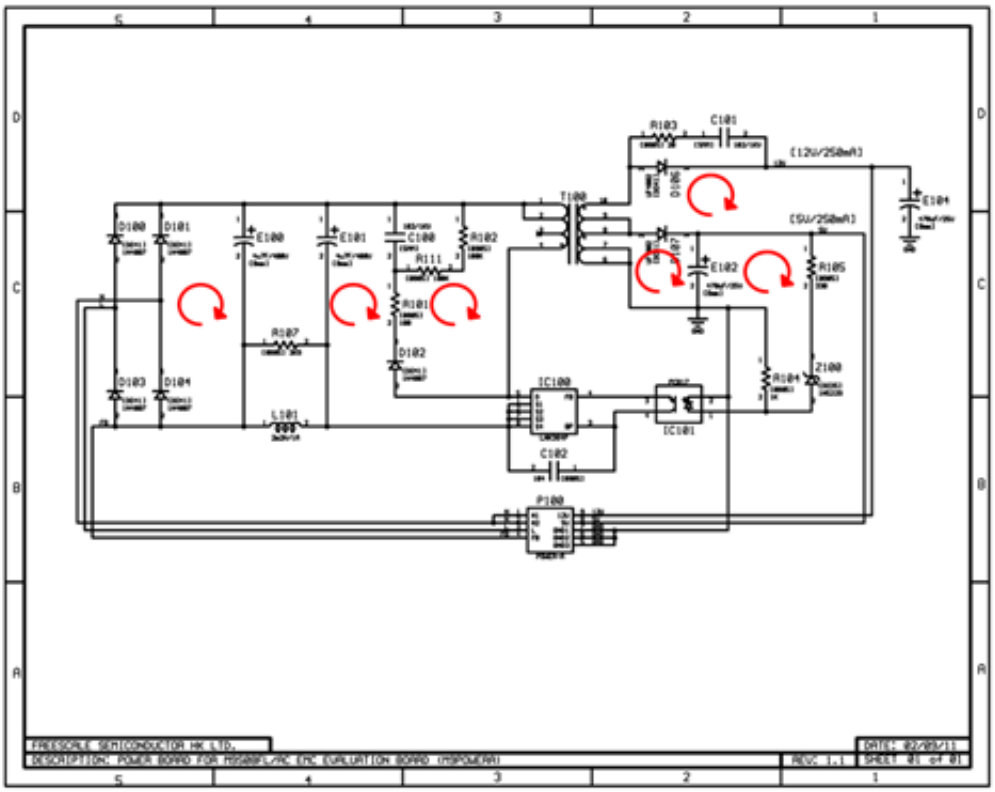

Figure 17. Loop consideration in SMPS circuit

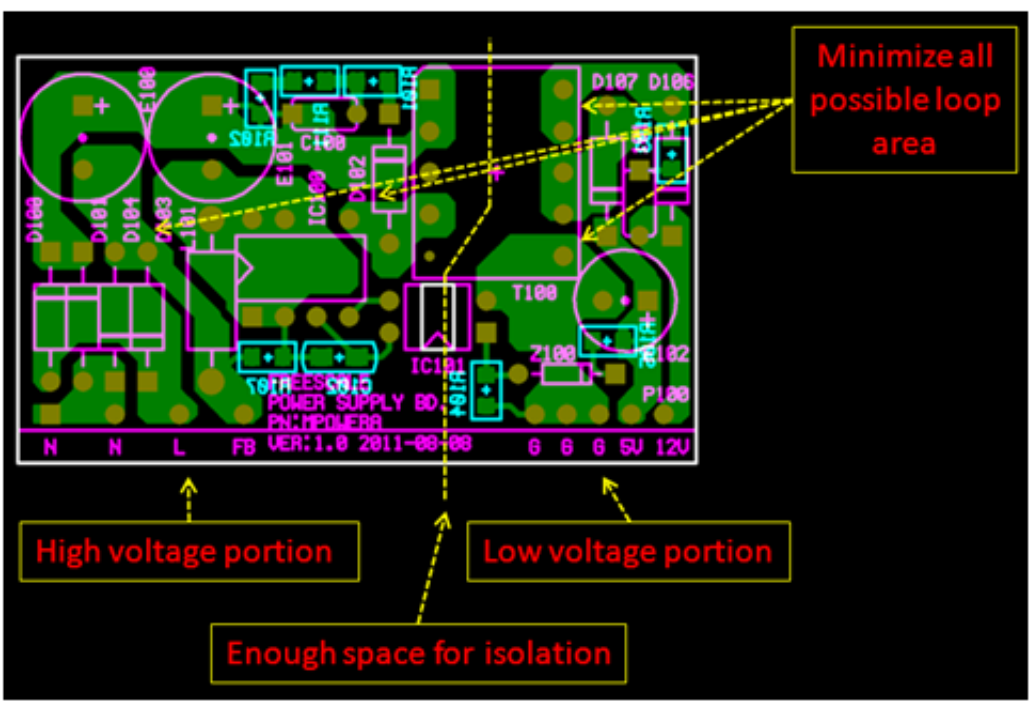

Figure 18. PCB layout implementation to minimize the return path loops

3.4 Main control board

Due to the space limitation, the AC to DC supply board is separated from the main control board which is mounted to the main board vertically. Important points to take care:

- Space to isolate the AC high-voltage portion and DC low voltage portion circuitry
- In some cases, adding a slot in the PCB is needed to provide higher isolation between them

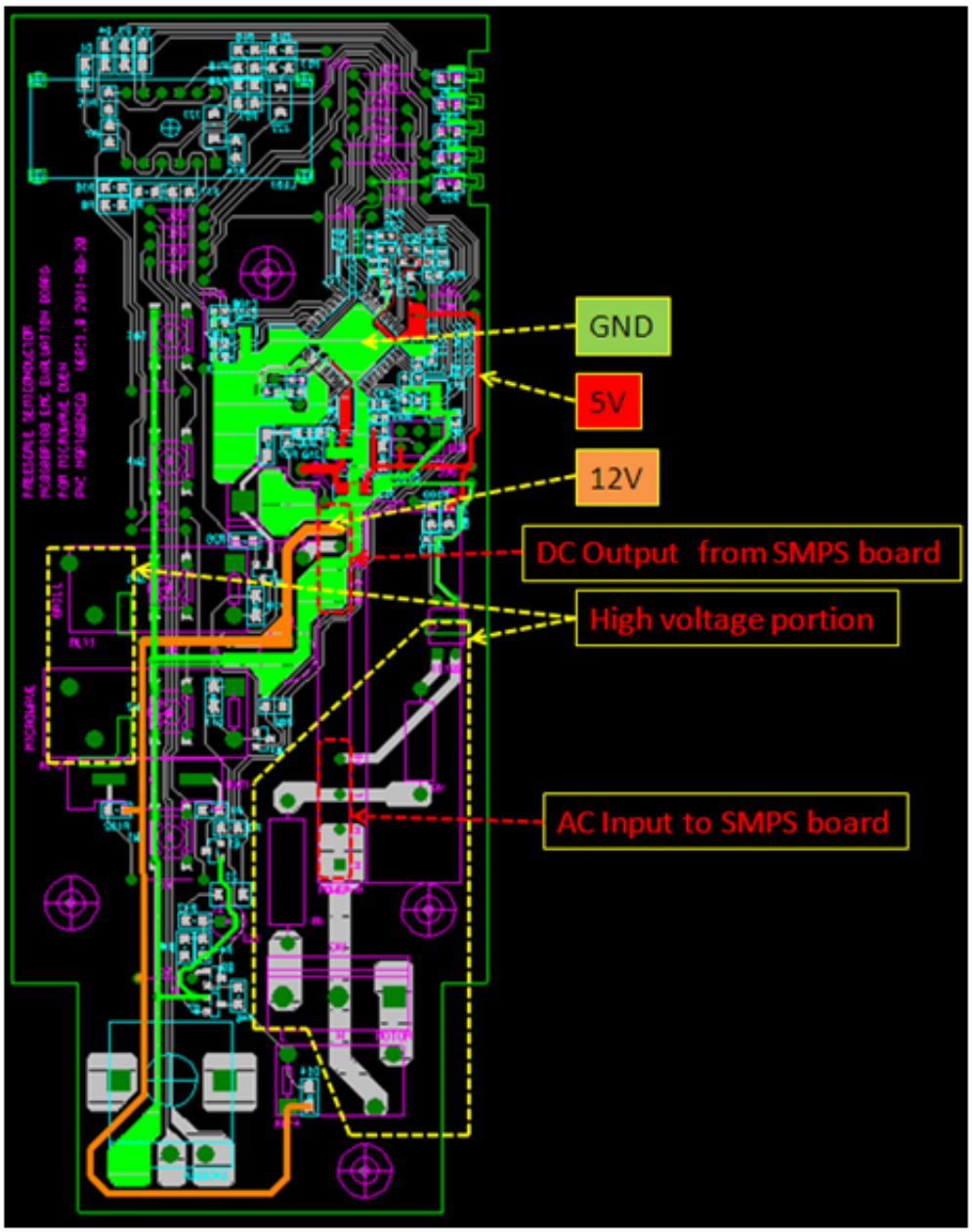

Figure 19. Overall placement and layout

3.5 Power supply routing and grounding

Figure 19 shows the DC supply comes from the vertical mounted SMPS board. In the output header of the SMPS board, the PCB layout technique is used to separate the ground into two portions. Figure 20, shows the ground form SMPS is divided into two sides by the PCB layout technique. One side acts as the 12 V ground return path except for the switches and encoder. The other side acts as the 5 V ground return path for the MCU and critical components. Therefore, the noise from the 12 V ground will not be coupled to the 5 V ground through the ground traces.

The reason to connect the 12 V ground to push buttons SW1–5 is to prevent that the ESD discharge energy couples to the 5 V GND directly. In some improper PCB layouts with good enough ESD energy passing through the MCU may cause the MCU to reset, or enter a hang-up state.

In the microwave oven, there is high noise energy in the DOOR1 header ground during the door open and close operation. It is highly recommended to connect it near the DC output from the SMPS board. See Figure 18.

In the MCU, building the ground plane on the bottom and connecting all V_{ss} pins together is good practice for EMC consideration. This ensures all MCU V_{ss} pins are at the same potential level and provide a good high frequency current return path (low inductance) back to the bypass capacitor. On the other hand, using three corners to connect the ground from the ground plane to the external circuitry can reduce the ground loop for those critical components near the MCU.

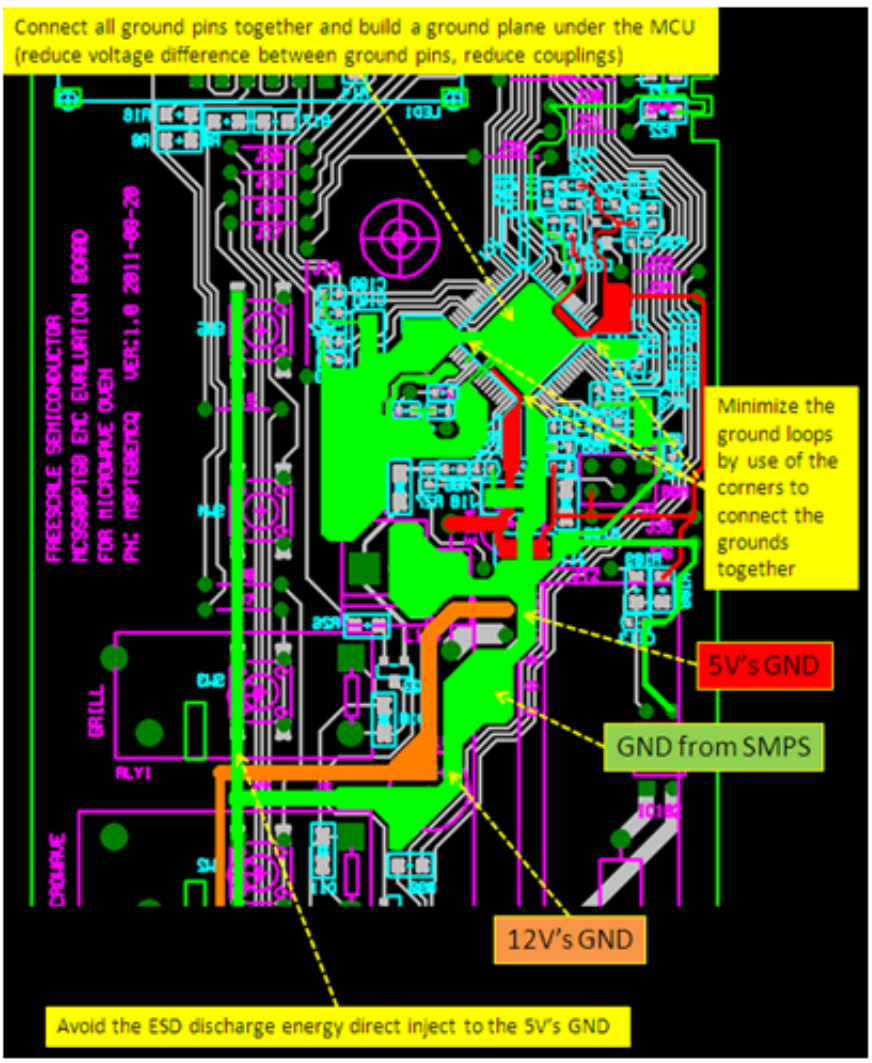

Figure 20. Power and ground routing

3.6 Bypass and decoupling

Two electrolytic capacitors E103 and E104 provide the decoupling of the 12 V and 5 V supplies. This helps minimize the common impedance coupling between 12 V and 5 V circuitries.

In a 5 V supply, adding the inductor L100 and associating it with decoupling capacitor E104 can eliminate the noise from other circuitries.

In the PT60 MCU, three bypass capacitors where added near its V*dd* and V*ss* pairs. The PCB layout designer needs to be aware of the the guidelines below during the layout.

- Connect V*dd* and V*ss* traces from power source to the decoupling capacitor E104 first and then connect them to the bypass capacitor before going to MCU
- Place V*dd* and V*ss* in parallel to minimize the loop area.
- Place the bypass capacitor to the V*dd* and V*ss* as close as possible

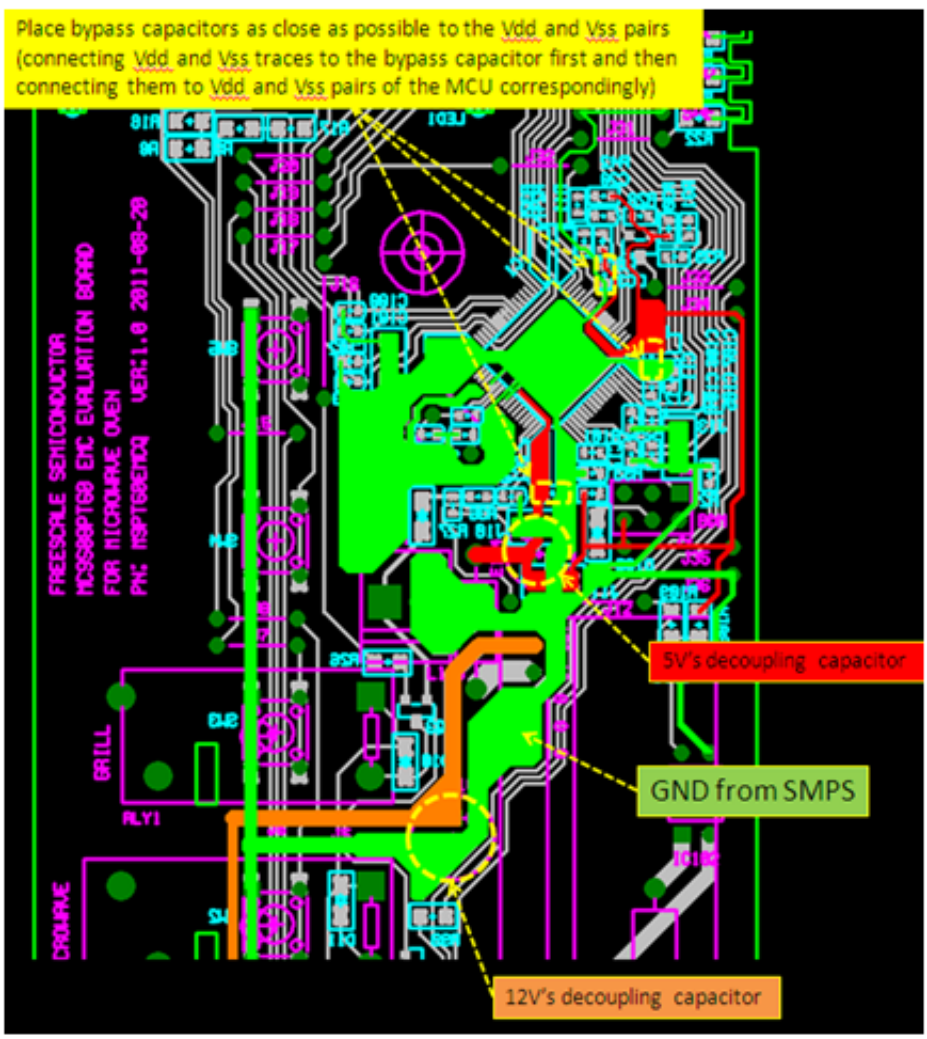

Figure 21. Bypass and decoupling

3.7 Crystal oscillator circuit

The crystal is easily affected by external noise, you need to take special attention in the layout. The MCU EXTAL and XTAL pins are also very sensitive to external noise, placing the ground and guard ring (no current ground) along with the trace connecting to the EXTAL and XTAL pin can minimize the noise coupling to the crystal circuit. The guidelines are listed below:

- Don not place any trace except ground near the crystal circuit including the bottom of the crystal circuit.
- Place oscillator circuit to the EXTAL and XTAL pin as close as possible. In this case is the crystal, feedback resistor and loading capacitors.
- Use the internal oscillator to have better EMC performance
- In double-layer or multi-layer PCB, connect the ground of the loading capacitor to the ground plane
- Use the minimum bus frequency to fill system requirements
- Apply the minimum trace length to the oscillator circuit
- Use suitable value of the feedback resistor and loading capacitors

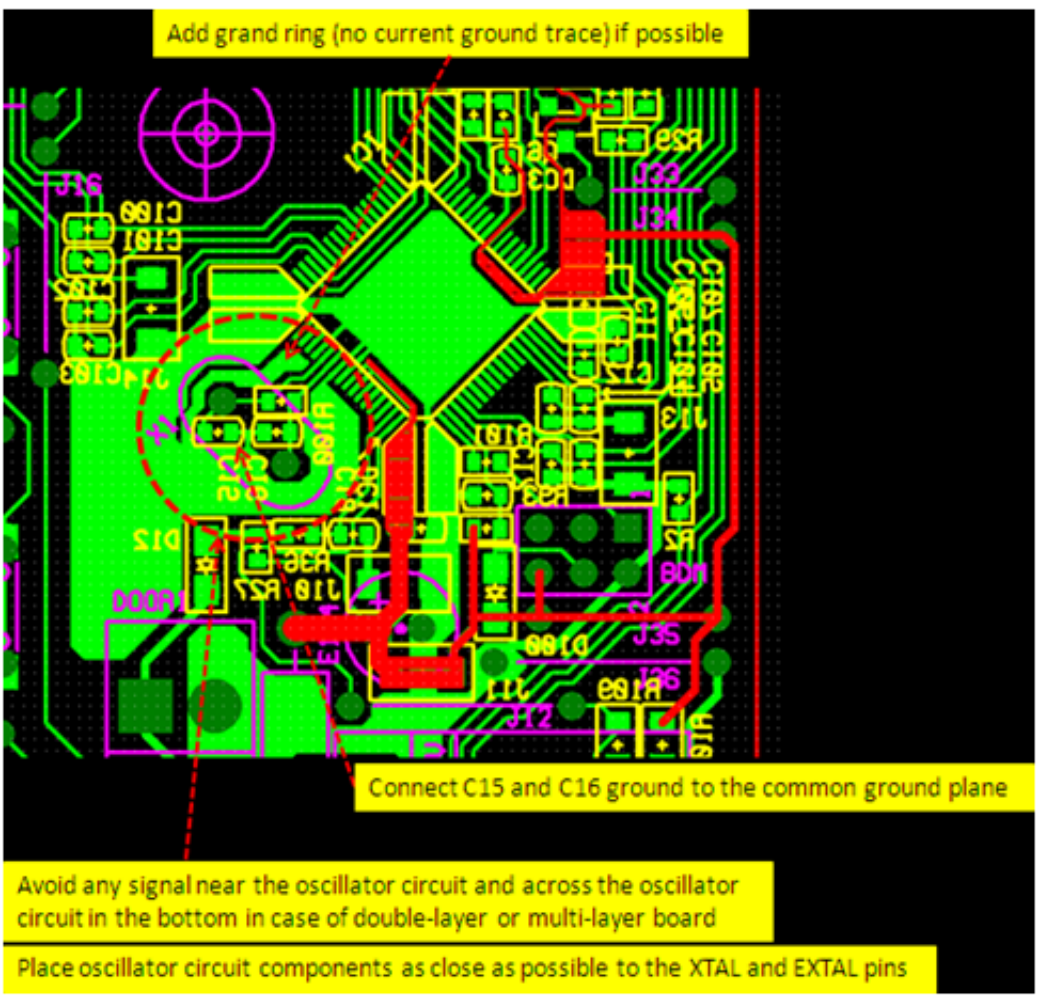

Figure 22. Oscillator circuit and layout

3.8 Spacing and isolation

Figure 19 shows the AC high-power region and DC low-power region, provide enough isolation space between them. In some cases, you need to add a slot for better isolation. Similarly, apply enough isolation space between the trace and screw holes or the trace and the board edge for ESD consideration.

3.9 Input Output (I/O)

In the MCU, the input port is also sensitive to noise. In most cases, an RC filter for the input port is added. The value of the RC filter is dependant on the input signal and its characteristic (digital or analogue, and rate of change). The typical value of the series resistor is in the range of 100 Ω to 1K Ω while the value of filtering the capacitor is in the range of 1000 pF to 0.1 uF. As mentioned in Section 3.2 Placement methods, the RC filter should be placed as near as possible to the input port. See Figure 16.

RESET, IRQ, and BKGD/MS are special pins in the PT60 MCU. The typical circuits of RESET, BKGD, and the BDM header are shown in Figure 15. The corresponding layout is shown in Figure 14. The key concept is to place them near the MCU and to minimize the loop area of traces (V*dd* , V*ss*) reducing the noise coupling off those pins.

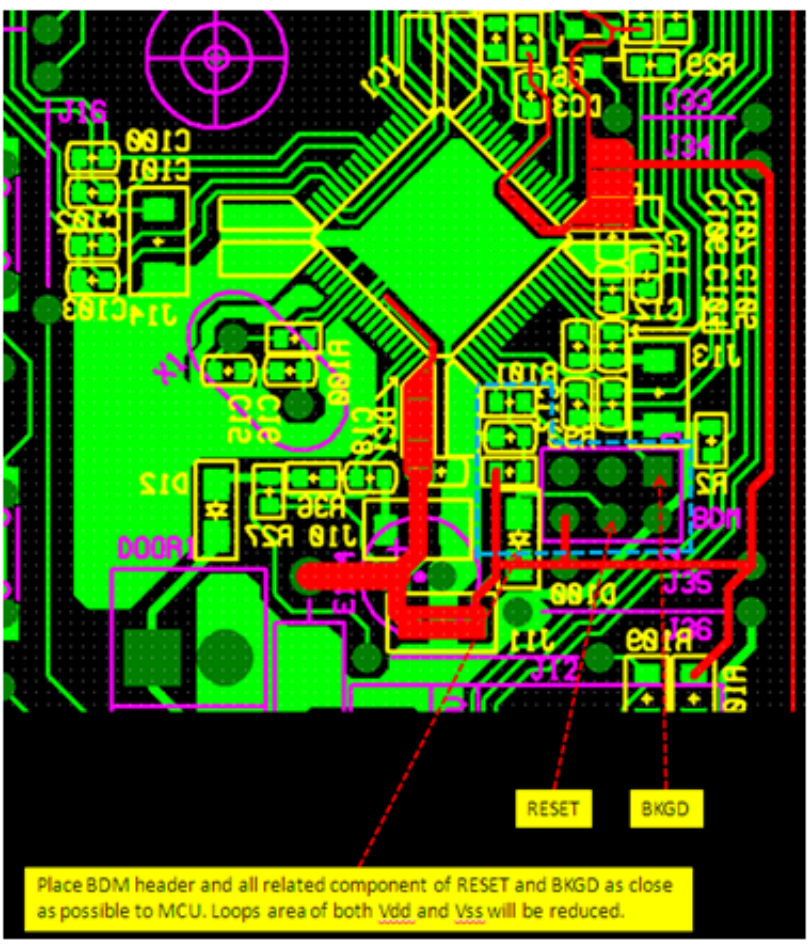

Figure 23. RESET, BKGD, BDM header, and layout

Unused I/O pins do not need to connect anything (that is, float) and set it as output logic low. The Direction Data Register (DDR) must be used to refresh periodically to avoid being changed with noise. The floating port pins are not allowed in some applications. Add the 10K Ω pull-down resistor and connect to the unused pin. Do not try to connect any unused I/O pins to power or ground directly.

3.10 Software techniques

In many cases, when the noise is coupled into the MCU, the system response is also dependant on the software implementation. Good defensive software design can protect the system during the noise injection. Below are some important techniques.

- Refresh data direction register periodically
- Enable Watchdog to avoid code runaway
- Use of the slew rate to increase the rise edge of the digital signal
- Fill unused memory to avoid code runaway
- Define all interrupt vectors even those not used
- Enable input glitch filter (PT60 build-in feature)

There is a new feature in the PT60 MCU, the input glitch filter provides a simple low-pass filter for the I/O pins. The glitch width threshold can be programmable from 1 to 128 ms.

4 Conclusion

There is always a challenge to build a low-cost PCB solution like a single-layer, double-sided loading, with limited size that needs to pass EMC compliance tests. Good planning to minimize the EMC risk at the beginning of the project is necessary to avoid the cost of the EMC fix.

Although most of the MCU manufacturers spend a lot of time improving their chip EMC performance, a good PCB layout, hardware design, software design, and good product designs are needed to minimize coupling paths from the noise source to the receptor.

5 References

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