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Application Note

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Using the High Resolution Timer and PWM in the S12ZVC

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1 Introduction

The S12ZVC family is a member of the S12 MagniV product line integrating a battery level (12 V) voltage regulator, supply voltage monitoring, high voltage inputs and a Controller Area Network (CAN) physical interface. These and other features make this device ideal for CAN node applications such as sensors, switch panels, or small actuators.

This document intends to explain the functions and advantages of the special high resolution timers and PWM available in the MC9S12VC devices and their role in advanced timing applications.

2 High resolution timer

The TIM16B8CV3 module consists of a 16-bit software programmable counter driven by a flexible programmable prescaler.

This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output waveform. Pulse widths can vary from microseconds to many seconds.

2.1 Features

The following features are found in the TIM16B8CV3 module:

- 16-bit counter
- Up to 8 input capture/output compare channels
- 16-bit pulse accumulator available on channel 7
- Selectable trigger transition edge for captures
- Clock prescaling

2.2 Initialization

To use the timer module the application can follow the steps shown below:

- Configure the prescaler (TSCR2[PR]).
- Configure needed channels as Input Capture (TIOS[IOSx]=0) or Output Compare (TIOS[IOSx]=1).
- Enable interrupts if needed in the timer interrupt enable register (TIE).
- Set the timer enable bit (TSCR1[TEN]).

3 High resolution PWM

The S12PWM8B8CV2 module is a channel scalable PWM with the flexibility to select one of four clock sources per channel.

3.1 Features

The S12PWM8B8CV2 module has the following distinctive features:

- Up to eight 8-bit or four 16-bit independent PWM channels
- Programmable period and duty cycle for each channel
- Dedicated counter for each channel
- Programmable PWM enable/disable for each channel
- Selectable pulse polarity for each channel
- Double buffered period and duty cycle registers
- Left or center aligned output configurable independently on each channel
- Four clock sources

3.2 Initialization

To configure PWM the application can follow the steps shown below:

1. Select 8 bit (CONxx=0) or 16 bit (CONxx=1) operation.
2. Select the clock source (PWMCLK register).
3. Configure prescaler (PWMPRCLK register).
4. Configure duty (PWMDTYx) and period (PWMPERx).
5. Select the PWM polarity (PWMPOL).
6. Select left aligned (CAEx=0) or center aligned (CAEx=1) output.
7. Enable the needed channels (PWMEx=1).
8. Change the duty cycle and period of a given channel at any time by writing to the desired channel period and duty registers (Period and duty cycle registers are double buffered. Change takes place when the end of the effective period is reached or when the channel is disabled).

4 Use case examples

The following use cases illustrate how to take advantage of the advanced features of the S12ZVC in two example automotive applications.

4.1 Ultrasonic level sensor

In this application the signal runtime of ultrasonic response has to be measured. Sensor output can be connected to any ADC channel. The analog comparator is then used to compare the sensor output voltage with a reference voltage provided by the DAC module. The output of the analog comparator is finally connected to the high resolution timer to measure the signal runtime.

4.2 Waveform measurement and generation

The 16-bit counter of the timer module together with the 7 input capture or output compare channels can be configured to measure a waveform while simultaneously generating an output waveform.

Configuring a channel to function as input capture will help measure an input waveform by capturing the 16-bit value of the timer when an input event occurs. Input capture channels can be configured to detect rising edges, falling edges, or any edge. Furthermore channel 7 of the timer module has a 16-bit pulse accumulator that can count how many of these events have occurred. Software can read the capture registers and calculate input waveform features such as low time, high time, period, etc.

Using the timer channels as output compare can help generate an output waveform by changing the state of a pin when the timer counter reaches the value programmed in the output compare register of any given channel. Channels can be configured to just trigger an interrupt on a successful output compare, toggle the output line, clear the output line to zero, or set the output line to one thus helping generate an output waveform without CPU intervention.

5 Attachments

For your reference please download companion software AN4851SW.zip from freescale.com to find the code and CodeWarrior project for configuring the timer and PWM modules in the S12ZVC device.

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