Freescale Semiconductor
Application Note

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Migrating from MPC5675K to MPC5775K

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Contents

1 Introduction

The Qorivva MPC5675K and MPC5775K are 32-bit MCUs built on Freescale's Power Architecture® technology integrating technologies that are important for present and future automotive safety applications. These MCUs are targeted at automotive applications including radar, transmission control, steering and braking, as well as high end hybrid and advanced combustion systems, electric power steering, chassis, and safety applications that require a high safety integrity level. MPC5775K is the 55 nm successor to the 90 nm MPC5675K. MPC5775K is built for RADAR applications with a set of feature modules including high fidelity and high speed analog-to-digital converters and a high performance Fast Fourier Transform (FFT) unit. For the signal processing the device targets an ISO26262 ASIL-B integrity level in combination with an ISO26262 ASIL-D integrity level compute system based on delayed lock-step. Its peripheral set is compatible with MPC5675K to allow a high degree of re-use. This application note provides a summary of the significant differences between MPC5675K and MPC5775K devices, and may be used as a reference for planning a migration to MPC5775K. This application note covers the architectural differences between the two devices and highlights the software and hardware considerations for migrating from an existing MPC5675K-based design to MPC5775K.

2 Overview

The following table summarizes the key feature differences between MPC5675K and MPC5775K.

Table 1. MPC5675K and MPC5775K comparisons

Feature	MPC5675K	MPC5775K
Process	C90	C55
Core • Lock-Step mode • Decoupled Parallel mode • Execution speed • SPE2 • EFPU2 • MMU • MPU • Instruction set PPC Book E • Instruction set VLE • Instruction cache • Data cache • Data local memory	Dual-Core e200z760n3 • Yes • Yes • Yes (up to 180 MHz) • Yes • Scalar/Vector • 64 entries • 16 regions • Yes • Yes • 16 KB • 16 KB • No	Dual-Core e200z726 + e200z420 • Yes (delayed lock-step z4) • Yes (decoupled core z7) • Yes (up to 266 MHz (133 MHz ,z4)) • Yes (z7 only) • Scalar/Vector (z4 only scalar) • No • 24 regions • No • Yes • z7 16 KB (z4 8 KB) • z7 16 KB (z4 4 KB) • 64 KB on e200z4
Core bus	AHB 32-bit address, 64-bit data	AHB 32-bit address, 64-bit data e2eECC
Internal Periphery bus	32-bit address, 32-bit data	32-bit address, 32-bit data
Master x Slave ports	• 4 x 3 in Lock-Step mode • 6 x 3 in Decoupled Parallel mode	• 7 x 8 XBAR_0 • 4 x 4 XBAR_1
Code/Data flash memory	2 MB	4 MB
SRAM	512 KB	1.5 MB (8 banks)
System MPU	No	16 regions
Error Correction Status module	Yes	No
Memory Error Management Unit	No	Yes
Fault Control and Collection Unit	Yes	Yes
Interrupt controller • Priority levels • Software settable interrupts • Latency monitor	Yes • 16 • 8 • No	Yes • 32 • 16 • Yes
Periodic Interrupt Timer	1 module x 4 channels	2 module x 4 channels
System Timer Module	1 module x 4 channels	3 module x 4 channels
eTimer	• eTimer_0: 6 channels • eTimer_1: 6 channels • eTimer_2: 6 channels	• eTimer_0: 6 channels • eTimer_1: 6 channels • eTimer_2: 6 channels
Enhanced DMA	32 channels, replicated module	32 channels
DMA Channel Mux	• 2 module (32 channels) • 46 peripheral sources	• 1 modules (32 channels) • 37 peripheral sources on DMAMUX_0 • 37 peripheral sources on DMAMUX_1
FlexRay	1 module x 64 message buffers, dual channel	1 module x 64 message buffers, dual-channel

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Table 1. MPC5675K and MPC5775K comparisons (continued)

Feature	MPC5675K	MPC5775K
FlexCAN	4 modules x 32 message buffers	4 modules x 64 message buffers error detection/correction
MCAN	No	Yes
LINFlexD	4 modules	4 modules
FlexPWM	2 modules x 4 channels	2 modules x 4 channels
Analog-to-digital converters	• 4 x SAR ADC • 12-bit (1 MSample/sec) • Up to 34 analog pads	• 4 x SAR ADC (12-bit) • 1 MSample/sec • 8 x SD ADC (12-bit) • 10 MSamples/sec • 8 converters
Cross Triggering Unit	• 2 modules	• 2 modules • Dual conversion mode • Interleaved triggering
Sine-Wave Generator	No	Yes
Deserial Serial Peripheral interface	3 modules	4 modules
Cyclic Redundancy Checker	2 modules	2 modules
External bus interface	Yes	No
DRAM Controller	Yes	No
IIC	2 modules	3 modules
Parallel Data Interface	Yes	Yes
Ethenet	FEC	ENET (Time stamp)
Signal Processing Toolbox	No	Yes
Analogue Front End	No	Yes
Peripheral Register Protection	Yes	Yes
Interprocessor Serial Link interface	No	Yes
Device power supply	• 3.3 V I/O • 1.2 V with internal switched regulator or external supply	• 3.3 V I/O • 3.3 V High fidelity analog • 1.25 V with internal switched regulator or external supply
Analog reference voltage	3.3 to 5.5 V	3.3 to 5.5 V
Phase-locked loop	2 Frequency-modulated phase-locked loop (FMPLL)	1 PLL and 1 Frequency-modulated phase-locked loop (FMPLL)
Internal RC oscillator	16 MHz	16 MHz
External crystal oscillator	4–40 MHz	40 MHz
LBIST and MBIST	Available at startup	Available at startup or shutdown
Low Power modes	• HALT • STOP	• HALT • STOP
Debug/Trace • JTAG • Class • MDO • Aurora	• Yes • Level 3+ • RPM and FPM • No	• Yes • Level 3+ • - • Yes

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Table 1. MPC5675K and MPC5775K comparisons (continued)

Feature	MPC5675K	MPC5775K
Package (MAPBGA)	• 257 balls, 0.8 mm pitch, 14 mm x 14 mm outline • 473 balls, 0.8 mm pitch, 19 mm x 19 mm outline	• 356 balls, 0.8 mm pitch, 17 mm x 17 mm outline

3 Software considerations

3.1 Core complex

3.1.1 Operating modes

The MPC5675K supports both decoupled parallel mode (DPM) and lock-step mode (LSM). In DPM, each core runs independent of each other with redundancy checks disabled. In LSM, the two redundant e200z7 cores execute the same operations or transactions synchronously.

MPC5775K has four separate cores that perform various computational and safety control functions. The main computational shell consists of the following three cores, which are used for general computational functions:

- Main Core_0 is e200z4201n3 core,
- Main Core_1 is e200z7260n3 core, and
- Main Core_2 is e200z7260n3 core

The fourth core, Checker Core_0s, uses e200z419 core, which is a true subset of the e200z4201n3 core.

The Checker Core_0s operates in lock-step mode with Main Core_0 executing exactly the same instructions as Main Core_0. Checker Core_0s ensures that Main Core_0 is executing correctly. There is no lock-step function associated with Main Core_1 and Main Core_2. The e200z419 core, used as Checker Core_0s, differs in hardware from the e200z4201n3 core as it has neither of the following:

- Instruction cache,
- Data cache,
- I-memory, and
- D-memory

3.1.2 Signal processing extension unit

MPC5675K supports the Signal Processing Extension (SPE2) unit for real-time single instruction, multiple data (SIMD) fixed-point, and single-precision embedded numeric operations.

MPC5775K implements the same SPE2 unit. MPC5775K implements the SPE2 unit on e200z7 core and not on e200z4 core.

3.1.3 Floating-point instructions

MPC5675K supports the Embedded Floating Point Unit (EFPU) which implements scalar and vector single-precision floating-point instructions.

MPC5775K e200z4 core EFPU supports scalar single-precision floating-point instructions. It does not support vector single-precision floating-point instructions, therefore, the software must be updated if this feature is used on MPC5675K.

3.1.4 General-purpose registers

MPC5675K e200z7 cores implement 64-bit general-purpose registers (GPRs) to support vector instructions defined by the SPE category.

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MPC5775K e200z4 cores implement 32-bit GPRs that are accessed through instruction operands. The EFPU instructions operate on 32-bit GPRs.

3.1.5 Instruction set architecture

MPC5675K e200z7 cores use the 32-bit Power Architecture Book E instruction set architecture (ISA) as well as the variable-length encoding (VLE) which uses the 16-bit versions of the standard Book E ISA for reduced code footprint.

MPC5775K cores implement the VLE ISA only. The software must be updated to ensure that fixed-length 32-bit instruction set is not used.

3.1.6 Core memory management

The MPC5675K core Memory Management Unit (MMU) provides a 64-entry translation lookaside buffer (TLB) to define virtual to physical address translation. MPC5775K does not implement an MMU so there is no address translation.

Instead, the Core MPU (CMPU) is supported to provide access protection to specified memory regions. The software should configure the region descriptors with the address ranges, access protections, and memory attributes for each protected region. The software instructions are also implemented for reading and writing the MPU entries and special purpose registers for the MPU assist registers.

3.1.7 Local data memory

MPC5675K does not include local memory in the core complex.

MPC5775K linker file must be updated to add 64 KB of local data memory (DMEM) of the main core. The software should use DMEM for critical data to take advantage of its zero wait-state latency.

3.2 Flash memory

Both MPC5675K and MPC5775K provide an electrically programmable/erasable, non-volatile flash memory for instruction and/or data storage. However, the C55 flash memory of MPC5775K has different electrical characteristics as compared to the C90 flash memory of MPC5675K. For optimum performance, the software must configure the correct number of wait states and address pipeline control in the flash memory controller.

The linker file must be updated to reflect the increased flash memory size and different flash memory partitioning.

3.3 Flash ECC testing

MPC5675K flash memory has a user-test (UTEST) mode ECC logic check feature that can be utilized for ECC logic testing. The software test applies walking 0 patterns to data and ECC parity bits to perform the ECC logic check.

In MPC5775K, the flash ECC is supervised by hardware. MPC5775K implements end-to-end ECC (e2eECC) error detection and correction in hardware for improved fault tolerance and detection. While traditional ECC-protected memories generate the ECC checkbits and store the data and checkbits in the memory, with e2eECC all bus masters generate the Single Error Correcting and Double Error Detecting (SECDED) code for every bus transaction. ECC is stored in memories on write operations and validated by the master on read operations.

The flash ECC testing in software is no longer required on MPC5775K.

3.4 RAM memory

Both MPC5675K and MPC5775K provide an on-chip SRAM with ECC. The linker file must be updated to reflect MPC5775K's increased SRAM size.

ECC protection in MPC5775K is extended for all memories, including the FlexRay, FlexCAN, and DMA RAM arrays. The software must take into consideration the changes in the mapping of the FCCU fault sources related to the system RAM and peripheral RAM ECC errors.

On MPC5775K, the SRAM is organized in to eight banks so that the different masters can access different banks simultaneously, thereby increasing the performance.

3.5 System memory protection

MPC5675K Memory Protection Unit (MPU) supports 16 memory region descriptors. Each crossbar master can be assigned different access rights to each region. The optional process identifier (ID) from the current bus master is checked against the descriptor's attributes for region hit determination.

In addition to the MPC5775K core MPU, the System MPU (SMPU) provides another layer of memory protection. The SMPU splits the physical memory map into 16 different regions. Unlike the MPC5675K MPU which is process ID-aware, the MPC5775K SMPU uses the master ID, privilege level, and access type to determine whether an access violated the protected region. The SMPU also uses the memory region's cacheability attributes to determine whether references to a region can be cached.

The software must be updated to define the memory spaces and configure each crossbar master's access rights to each region.

3.6 Peripheral bridges

The peripheral bridge (PBRIDGE) is the interface between the system bus and the on-chip peripherals. Accesses that fall within the address space of the PBRIDGE are decoded to provide individual module selects for the peripherals.

In MPC5675K and MPC5775K one set of peripherals is controlled by AIPS_0 and the other set of peripherals is controlled by AIPS_1. On-Platform peripherals are controlled by AIPS_0. On and Off-Platform peripherals are controlled by AIPS_0 or AIPS_1.

The MPC5775K header file must be updated to reflect the new memory mapping of the peripherals. Peripheral access control to restrict read and write accesses to individual peripherals must be updated to reflect changes in the implemented peripherals.

3.7 Direct Memory Access

MPC5675K and MPC5775K Enhanced Direct Memory Access (eDMA) allows complex data transfers with minimal intervention from the core processor. MPC5675K implements a replicated 32-channel eDMA controller. MPC5675K eDMA Channel Mux (DMAMUX) allows 46 DMA peripheral sources to be routed to 32 DMA channels.

MPC5675K implements one 32-channel eDMA controllers and MPC5775K implements two DMAMUX modules:

- DMAMUX_0 connects 1-37 peripheral sources to channel 0 through 15
- DMAMUX_1 connects 1-37 peripheral sources to channels 16 through 31.

The software should be updated to take advantage of the additional DMA channels and the split of the DMA channel muxes.

3.8 Clock architecture

MPC5675K implements two independent frequency-modulated phase-locked loop (FMPLL) modules to generate the system and peripheral clocks.

MPC5775K C55 dual-PLL architecture drives the peripherals from the PLL0 output while the core and platform clocks are driven by the PLL1 frequency-modulated output. The software must update the drivers for MPC5775K PLLs which require a different programming model from the MPC5675K PLLs.

The clock distribution on MPC5775K is also different from MPC5675K. The software must update the assignment of clock sources as well as the system and auxiliary clock dividers. It must also take into account the frequency limits of these clocks. Refer to the MPC5775K Reference Manual for the clock assignments and maximum frequencies for each module, available at freescale.com

MPC5775K has an improved progressive clock switching which allows for linear ramp up ramp down of the system clock.

On MPC5775K the oscillator is part of Analogue Frond End (AFE) block which results in a different memory space compared with MPC5675K.

3.9 Interrupt Controller

MPC5675K Interrupt Controller (INTC) provides 16 interrupt priority levels and eight software settable interrupt sources. MPC5775K increases the number of interrupt priority levels to 64 and the number of software settable interrupt sources to 16. The software should take these enhancements into consideration.

Differences in implemented peripherals between MPC5675K and MPC5775K affect the interrupt vector assignments. The software must update the interrupt vector table to define the implemented interrupt sources on the MPC5775K.

MPC5775K adds Interrupt Controller Monitor (INTCM) to provide a safety mechanism to monitor the latency of maximum four interrupt sources to ensure that these interrupts execute within the expected window of time. Safety-critical applications should use INTCM select IRQs to monitor and to set the maximum interrupt latency for the selected IRQs.

3.10 Pad control and I/O multiplexing

The System Integration Unit Lite (SIUL) provides control over the electrical configuration of the pads, general-purpose functionality, external interrupts, and I/O multiplexing. Although a similar I/O multiplexing between MPC5675K and MPC5775K is maintained, the C55 devices implement a different SIUL programming model. The software must take into consideration the new SIUL memory map and updated pad control capabilities of MPC5775K.

MPC5775K SIUL also adds a DMA request interface. The REQ input pins are the sources of interrupt or DMA requests. Four DMA request channels are available on MPC5775K.

3.11 ECC error reporting

MPC5675K Error Correction Status Module (ECSM) provides information about the platform configuration and revision. It also provides registers for capturing information on memory errors. ECSM is not supported on MPC5775K. The software must be updated to remove ECC error reporting and error injection functions using ECSM. Instead, the software should check the reported ECC errors in SRAM, flash, and peripheral RAM in the Memory Error Management Unit (MEMU).

Additionally, the software should configure the reaction to the ECC error events in the Fault Collection and Control Unit (FCCU).

3.12 Failure handling

MPC5675K and MPC5775K implement the Fault Collection and Control Unit (FCCU) which offers a hardware channel to collect errors and to place the device into a safe state when a failure is detected. MPC5675K classifies faults as either critical or non-critical based on the criticality and the related fault reactions, whereas MPC5775K classifies all faults as non-critical to provide maximum configurability of the fault reactions.

The software should be updated to reflect changes in fault configuration as well as the FCCU input mapping of the non-critical faults.

3.13 Low- and high-voltage detection and self-test

MPC5675K and MPC5775K have several low- and high-voltage detectors (LVD/HVD) that provide information whether the voltage is in proper range. MPC5675K provides LVDs for the 3.3 V I/O, regulator, and flash supplies as well as LVDs and HVDs for the 1.2 V core supply. MPC5775K Power Management Controller (PMC) provides LVDs for the 3.3 V oscillator, ADC, I/O, flash, and regulator supplies as well as HVD and LVD for the 1.25 V core supply.

MPC5775K PMC implements an LVD/HVD self-test mechanism which is automatically performed at power-up. The software has the option to trigger the LVD/HVD self-test. In this case, the software must configure the self-test time window before initiating the self-test.

3.14 Clock and temperature monitoring

MPC5675K and MPC5775K provide Clock Monitoring Units (CMUs) to detect missing clocks or incorrect clock frequencies. MPC5675K provides clock monitors for the system clock, XOSC clock, motor control clock, and FlexRay clock. Additional clock monitoring on MPC5775K is provided for the IRCOSC clock, checker clock, PBRIDGE clock, and ADC clock. The software should configure the clock monitoring accordingly.

MPC5675K is equipped with one Temperature Sensor (TSENS) and MPC5775K is equipped with two Temperature Sensors (TSENS). Each TSENS module provides an analog voltage that is proportional to the internal junction temperature of the device. The software should update control of MPC5775K TSENS done via the PMC register space.

3.15 Logic and memory built-in self-tests

MPC5675K performs the built-in self-test (BIST) every time a destructive or external reset occurs. The BIST is performed while the device is still under reset. MPC5675K provides memory BIST (MBIST) for all RAMs and ROMs. It also provides a logic scan-based BIST (LBIST).

MPC5775K MBIST and LBIST are performed every time the device boots. It also allows the MBIST and LBIST to be performed during shutdown. The shutdown self-test sequence is user-programmable and can be executed at less critical times in the application. A long functional reset is initiated after the self-test is executed during shutdown. The software needs to configure the Self-Test Control Unit (STCU2) to prepare the device for the shutdown self-test.

The run-time SAR-ADC BIST and run-time BIST of LVDs/HVDs are also available and require software enhancements.

3.16 Analog-to-digital converter self-test

MPC5675K and MPC5775K implement analog-to-digital converter (ADC) self-test to check the internal analog circuitry of the ADC. MPC5675K supports supply (algorithm S), resistive-capacitive (algorithm RC) and capacitive (algorithm C) self-tests. MPC5775K does not support a separate algorithm RC test. Instead, it merges the algorithm RC and algorithm C into a single algorithm.

MPC5775K also supports a high-accuracy calibration mode. In this mode, all the steps of ADC built-in-self-test (BIST) are run in succession and with averaging. ADC calibration registers get updated based on the measured values from the corresponding tests. The software should perform the ADC calibration after power-up, after an error situation or when the operating conditions change, particularly a change in the ADC reference voltage.

3.17 Low Power modes

Both MPC5675K and MPC5775K provide peripheral clock gating control during low-power modes. No dedicated low power mode or stand-by domains are implemented. The possibility to switch off clocks to reduce power and enter HALT/STOP modes is granted within a fully powered device.

3.18 Cyclic Redundancy Checker

The Cyclic Redundancy Checker (CRC) unit is a dedicated module for the computation of CRC and off-loading the CPU. MPC5675K and MPC5775K support CRC generation for CRC-16-CCITT and CRC-32 (Ethernet) polynomials.

For CRC-32, MPC5775K CRC engine expects the CRC input to be byte-swapped. For example, the software must enter 0x98EFCDAB in the input data register for a given input data of 0xABCDEF98. The BYTE_SWAP, inversion (INV), and swap (SWAP) selection bits in the Configuration register (CRC_CFG) must be set to 1.

For CRC-16, MPC5775K CRC engine expects the CRC input to be bit-reversed. For example, the software must enter 0x19F7B3D5 in the input data register for a given input data of 0xABCDEF98. The BIT_SWAP, INV, and SWAP bits in the CRC_CFG must be set to 0.

3.19 Cross-Triggering Unit

The Cross-Triggering Unit (CTU) allows automatic generation of ADC conversion requests without CPU load. MPC5675K and MPC5775K implements the following two CTU modules:

- CTU_0, that controls ADC0 and ADC1
- CTU_1, that controls ADC2 and ADC3

MPC5775K supports interleaved triggering in MPC5775K. In this mode, two ADCs control the execution of command lists with their triggers independently. The completion of one of the command lists does not require acknowledgement by both ADCs. The software can configure the CTU for interleaved triggering to improve system performance.

3.20 FlexRay

Both MPC5675K and MPC5775K support a dual channel FlexRay communication controller that implements the FlexRay Communications System Protocol Specification, Version 2.1 Rev. A. The FlexRay module implements 64 message buffers.

MPC5775K FlexRay module adds the Message Buffer Data Field Offset registers (FR_MBDOR0:67) and the Receive FIFO Start Data Offset register (FR_RFSDOR). The software must configure the data field offset values for all used message buffers. MPC5775K also adds the LRAM ECC Test Error registers (FR_LEETR0:5) which contain the LRAM ECC test data. The software must take into consideration the layout changes to the Controller Host Interface Lookup-Table Memory (CHI LRAM) which now includes the new registers.

The message buffer search engine runs on the CHI clock and evaluates one individual message buffer per CHI clock cycle. MPC5775K search duration requires an additional 27 CHI clock cycles instead of 10 CHI clock cycles for MPC5675K to ensure correct search engine operation. The application software must take into consideration the additional clock cycle requirements in the search duration.

The minimum CHI clock frequency for MPC5775K is different from the MPC5675K requirements. The timing requirements are defined in the MPC5775K Reference Manual. The minimum CHI frequency must be met, otherwise, a message buffer search error flag is set.

3.21 FlexCAN

MPC5675K and MPC5775K FlexCAN module implements the CAN protocol according to Version 2.0B specification, which supports both standard and extended message frames. The message buffers are stored in the embedded FlexCAN RAM.

MPC5675K implements four FlexCAN modules, each with 32 message buffers, while MPC5775K has four FlexCAN modules, each with 64 message buffers. The increase in message buffers requires the implementation of additional registers, thus MPC5775K FlexCAN memory map and programming model are different from MPC5675K. The software should take into account the new registers related to interrupts and masking for the additional message buffers.

MPC5775K also adds error detection and correction to the FlexCAN memory in read accesses. Each byte of FlexCAN memory is associated with five parity bits. The error correction mechanism ensures that for 13-bit word, errors in one bit can be corrected and errors in two bits can be detected but not corrected. The software should enable error correction in the Memory Error Control register (CAN_MECR) and check the error reporting registers to obtain the address, data, and syndrome of the detected error.

3.22 Periodic Interrupt Timer

MPC5675K and MPC5775K support a Periodic Interrupt Timer (PIT). PIT contains four 32-bit timer channels which can generate interrupts and trigger DMA channels.

MPC5775K adds a lifetime counter for applications that require Timer 0 and Timer 1 to be chained to build a 64-bit lifetime counter. To use this feature, the software must first read the PIT Upper Lifetime Timer register (PIT_LTMR64H) and then the PIT Lower Lifetime Timer register (PIT_LTMR64L).

3.23 Sine Wave Generator

MPC5775K supports the Sine Wave Generator (SGEN) module which generates analog sine wave signal that can range from 1 kHz to 50 kHz. The normal output of SGEN is a free running sine wave of a specified amplitude and frequency.

MPC5775K SGEN adds support for two trigger signals to enable the user to phase-align the sine wave output to the activation of the trigger input. Software can enable this feature in the SGEN Control register (SGEN_CTRL). When the sine wave is started, the trigger signal is continuously checked for a phase offset. If there is a phase offset, the SGEN re-aligns the sine wave output so that the phase difference becomes zero.

MPC5675K does not support the SGEN module

3.24 Parallel Data Interface

Both MPC5675K and MPC5775K have Parallel Data Interface (PDI) that provides an interface to high-speed external parallel devices such as external analog-to-digital converters (ADC) and image sensors. MPC5775K has an enhanced feature that allows the ADC digital interface to bypass sigma-delta ADCs enabling the ability to read RADAR data from external ADCs.

3.25 Ethernet

MPC5675K supports Fast Ethernet Controller (FEC) which is an Ethernet media access controller (MAC) designed to support both 10 and 100 Mbit/s Ethernet/IEEE 802.3 networks.

MPC5775K supports Ethernet MAC (ENET), a programmable 10/100 Ethernet MAC with IEEE 1588 integrates a standard IEEE 802.3 Ethernet MAC with a time-stamping module. The IEEE 1588 standard provides accurate clock synchronization for distributed control nodes for industrial automation applications. The driver software should be updated.

3.26 Common modules

Both MPC5675K and MPC5775K share the following modules which are similar and require little or no software alterations:

- DSPI,
- IIC,
- FlexPWM,
- eTimer, and
- LinFlex

3.27 New modules

The following modules are available only on MPC5775K and requires new software routines or drivers to be developed to support them:

- SPTB,
- WGM/DAC,
- CTE,
- SD-ADCs,
- MCAN, and
- LFAST/SIPI

4 Hardware considerations

4.1 Device packages

MPC5675K is available in 257-ball MAPBGA and 473-ball MAPBGA production packages while MPC5775K is available in 356-ball MAPBGA production packages and 473-ball MAPBGA development packages.

Table 2. Device package comparison

Package	MPC5675K	MPC5775K
257-ball MAPBGA	0.8 mm pitch 14 mm x 14 mm Outline	N/A
356-ball MAPBGA	N/A	0.8 mm pitch 17 mm x 17 mm outline
473-ball MAPBGA	0.8 mm pitch 19 mm x 19 mm outline	N/A

4.2 Pin compatibility

There is no pin compatibility between MPC5675K and MPC5775K. The new hardware should be developed to accommodate the differences.

4.3 Power supply

The power supply concept between MPC5675K and MPC5775K share several commonalities. The voltage regulator, I/O, flash, oscillator, and ADC supply voltages remain 3.3 V (nominal). However, the voltage range of MPC5675K is 3.0 V to 3.6 V, while MPC5775K requires a narrower range of 3.13 V to 3.6 V. Both devices support ADC reference voltages of either 3.3 V or 5 V and also support internal regulation mode when using external ballast transistor. The internal regulation mode allows a single 3.3 V supply to be input to MPC5775K when an external ballast transistor is present.

However, MPC5775K adds an external regulation option that allows 1.25 V ± 5% to be input to the core supply pins. This mode removes the requirement for the external ballast transistor. Both MPC5675K and MPC5775K do not support internal ballast transistor.

MPC5775K adds the Nexus Aurora and LFAST modules in the package. These blocks require 1.25 V voltage supplies. For full description please see Appendix 1.

Table 3. Device power supplies

Supply	MPC5675K	MPC5775K
Voltage regulator supply voltage	3.0 V to 3.6 V	3.13 V to 3.6 V
I/O supply voltage	3.0 V to 3.6 V	3.13 V to 3.6 V
Flash supply voltage	3.0 V to 3.6 V	3.13 V to 3.6 V
Oscillator supply voltage	3.0 V to 3.6 V	3.13 V to 3.6 V
ADC supply voltage	3.0 V to 3.6 V	3.13 V to 3.6 V
ADC reference voltage	3.3 V or 5 V	3.3 V or 5 V
Core supply	Internal regulation with external ballast transistor or Internal ballast transistor	Internal regulation with external ballast transistor or 1.25 V ± 5% external regulation
Aurora supply voltage	N/A	1.25 V
LFAST supply voltage	N/A	1.25 V

4.4 Operating temperature

MPC5775K supports an extended junction temperature of up to 150°C. The printed circuit board (PCB) and board components must meet the extended temperature requirements when MPC5775K is exposed to to high temperature.

Table 4. Device operating temperature

Feature	MPC5675K	MPC5775K
Junction temperature range	-40°C to 150°C	-40°C to 150°C
Ambient temperature range	-40°C to 125°C	-40°C to 125°C

4.5 I/O multiplexing

Hardware design must take into consideration the changes in pin multiplexing from MPC5675K to MPC5775K. Most of the functionality of port pins remains the same, however, some pins now have added alternate functions. The addition of new modules also affects supported functionality of some pins.

5 Summary

Freescale's MPC5775K offers some changes and enhancements over the MPC5675K. This document provides information on how to migrate from existing MPC5675K designs to the MPC5775K designs. The software and hardware must address the following major feature changes:

- Additional delayed lock-step cores
- VLE instruction set only
- 32-bit general-purpose core registers
- End-to-end ECC protection for all memories
- Internal/External regulation for the core supply
- Core and system-level memory protection
- Enhanced pad control capabilities
- Additional port pin functionality in I/O multiplexing
- MBIST and LBSIT at startup and shutdown
- MEMU for ECC error collection and reporting
- Increased configurability of FCCU fault reactions
- Changes in FCCU input mapping
- 55 nm-based flash memory controller
- Larger SRAM and flash memory
- Clock distribution changes
- Additional clock monitors
- Trigger signals in the SGEN
- ADC high calibration mode
- ADC self-test algorithm changes
- Dual conversion mode and interleaved triggering in the CTUs
- More DMAMUX channels
- Changes in interrupt vector assignments
- New signal processing toolbox functionality
- New AFE block with sigma-delta ADC and DAC, etc.

6 References

For additional information, refer to the following documents available at freescale.com :

- MPC5675K Reference Manual
- MPC5775K Reference Manual

7 Appendix 1 MPC5775K device supplies

Table 5. MPC5775K device supplies

Supply name	Supply description	Voltage level	Internal mode	Supply	External mode	Supply
vdd_lv_core	Core logic supply	1.25	Supplied by internal VREG	1.25 V supplied from external coil	Supplied by external supply	1.25_Switched Reg
vdd_hv_io [x]	Main GPIO supply	3.3	Supplied by external supply	3.3v_Switched Reg	Supplied by external supply	3.3v_Switched Reg
vdd_hv_adc	SAR ADC supply	3.3	Supplied by external supply	3.3v_Switched Reg	Supplied by external supply	3.3v_Switched Reg
vdd_hv_adcref0/2	SAR ADC reference supply	3.3/5 .0	Supplied by external supply	5V_Linear Reg	Supplied by external supply	5V_Linear Reg
vdd_hv_adcref1/3	SAR ADC reference supply	3.3/5.0	Supplied by external supply	5V_Linear Reg	Supplied by external supply	5V_Linear Reg
vdd_hv_fla	Flash supply	3.3	Supplied by external supply	3.3v_Switched Reg	Supplied by external supply	3.3v_Switched Reg
vdd_hv_io_pdi_0	PDI I/O supply	3.3	Supplied by external supply	3.3v_Switched Reg	Supplied by external supply	3.3v_Switched Reg
vdd_hv_io_pdi_0	PDI I/O supply	3.3	Supplied by external supply	3.3v_Switched Reg	Supplied by external supply	3.3v_Switched Reg
vdd_hv_io_pwm	PWM I/O supply (wg0, wg1, wg2)	3.3	Supplied by external supply	3.3v_Switched Reg	Supplied by external supply	3.3v_Switched Reg
vdd_hv_pmu	Supply for voltage regulator	3.3	Supplied by external supply	3.3v_Switched Reg	Supplied by external supply	3.3v_Switched Reg
vdd_hv_reg3v8	Supply for regulator switch driver	3.8	Supplied by external supply	3.8v_Switched Reg	Supplied by external supply	3.8v_Switched Reg
vdd_lv_drfpll	Supply for LFAST PLL	1.25	Supplied by internal VREG	Internal	Supplied by external supply	1.25_Switched Reg
vdd_lv_io_aurora	Supply for Aurora I/O	1.25	Supplied by internal VREG	Internal	Supplied by external supply	1.25_Switched Reg
vdd_lv_io	Supply for I/O	1.25	Supplied by internal VREG	Internal	Supplied by external supply	1.25_Switched Reg
vdd_lv_pll0	Supply for PLL	1.25	Supplied by internal VREG	Internal	Supplied by external supply	1.25_Switched Reg
vdd_hv_raw	3.0–3.6V supply	3.3	Supplied by external low noise supply	3.3v_Linear Reg	Supplied by external supply	3.3v_Linear Reg
vdd_hv_dac	3.0–3.6V supply. Connects to DAC (analog portion)	3.3	Supplied by external low noise supply	3.3V_Linear Reg	Supplied by external VREG	3.3V_Linear Reg

Table continues on the next page...

Table 5. MPC5775K device supplies (continued)

Supply name	Supply description	Voltage level	Internal mode	Supply	External mode	Supply
vdd_lv_dac_2v5	2.5 V regulated analog supply from the DAC digital 1 V Vreg	2.5	Supplied by internal VREG	Internal	Supplied by internal VREG	Internal
vdd_lv_osc	1.47–1.33 V regulated analog supply from the XOSC analog 1.4 V Vreg	1.4	Supplied by internal VREG	Internal	Supplied by internal VREG	Internal
vdd_lv_sdclk	1.47–1.33 V regulated supply from the LVDS analog 1.4 V Vreg	1.4	Supplied by internal VREG	Internal	Supplied by Internal VREG	Internal
vdd_lv_radar_dig	1.47–1.33 V regulated digital supply from the ADC digital 1.4 V Vreg	1.4	Supplied by internal VREG	Internal	Supplied by internal VREG	Internal
vdd_lv_sdadc	1.47–1.33 V regulated analog supply from the ADC analog 1.4 V Vreg	1.4	Supplied by internal VREG	Internal	Supplied by internal VREG	Internal
vdd_lv_sdpll	1.47–1.33 V regulated analog supply from the PLL analog 1.4 V Vreg	1.4	Supplied by internal VREG	Internal	Supplied by Internal VREG	Internal
vdd_lv_radar_ref	1.25 V reference voltage from the VREF	1.25	Supplied by internal VREG	Internal	Supplied by internal VREG	Internal

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