Freescale Semiconductor
Application Note

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Hardware Design Considerations for MKW2x IEEE® 802.15.4 Devices

1 Introduction

This application note describe Printed Circuit Board (PCB) design considerations for the MKW2x LGA63 package. Included are layouts of the component copper layer, solder mask, and solder paste stencil. These recommendations are guidelines only and may need to be modified depending on the assembly house used and the other components on the board.

Contents

2 63-Pin LGA Component Copper Layer

Figure 1 shows a recommended component copper layer. This layer is also referred to as the top metal layer and is the layer to which the components are soldered. The footprint for the LGA-63 package consists of 56 IC contact pads, six internal pads and a centered ground pad. The centered ground pad is partitioned into four pads. the copper pattern as shown in Figure 1. Use 0.25 mm via holes to connect to the ground plane layers. These are required for RF grounding and help prevent solder float.

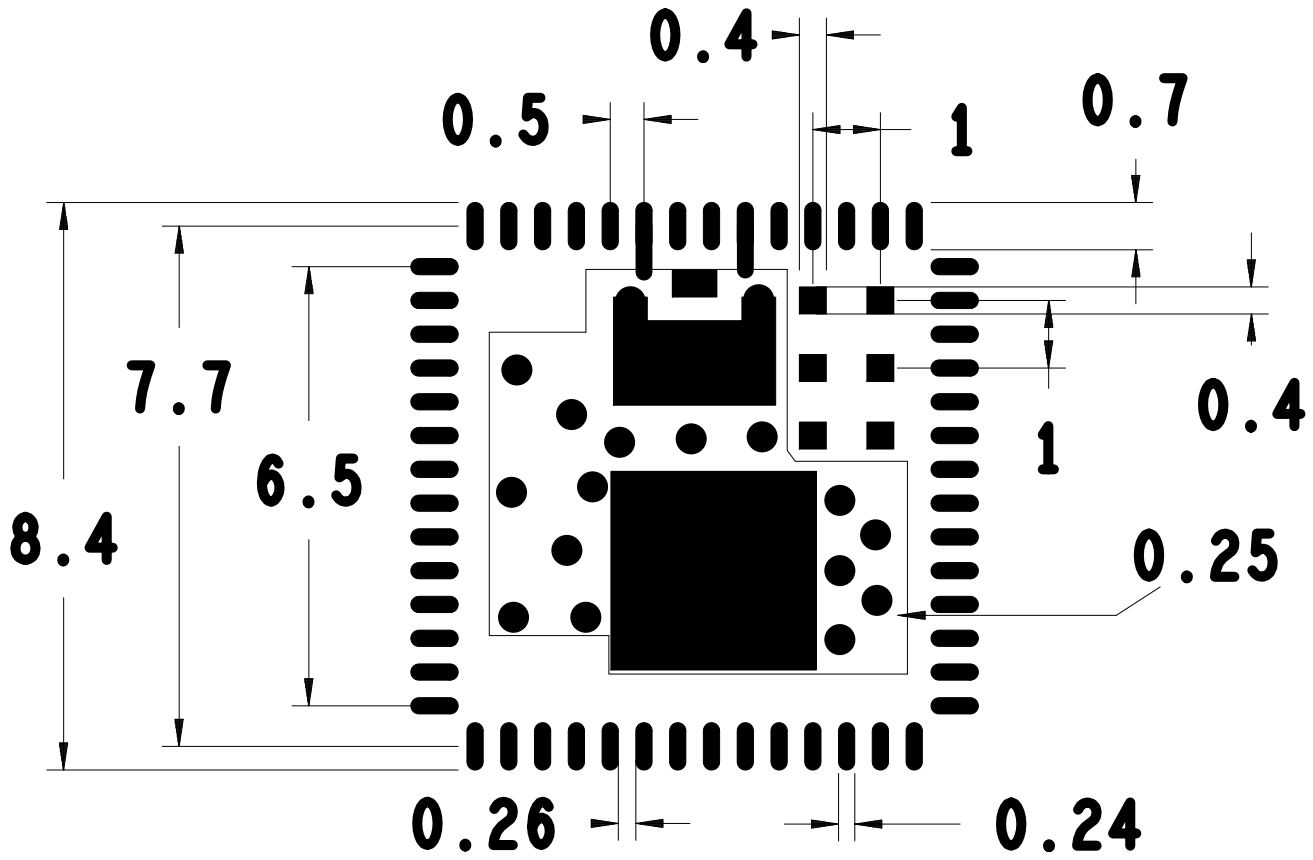

Figure 1. LGA Component Copper Layer

2.1 63-Pin LGA Solder Mask

The solder mask limits the flow of the solder paste during the reflow process. Figure 2 shows a recommended solder mask pattern. The pattern represents openings in the solder mask.

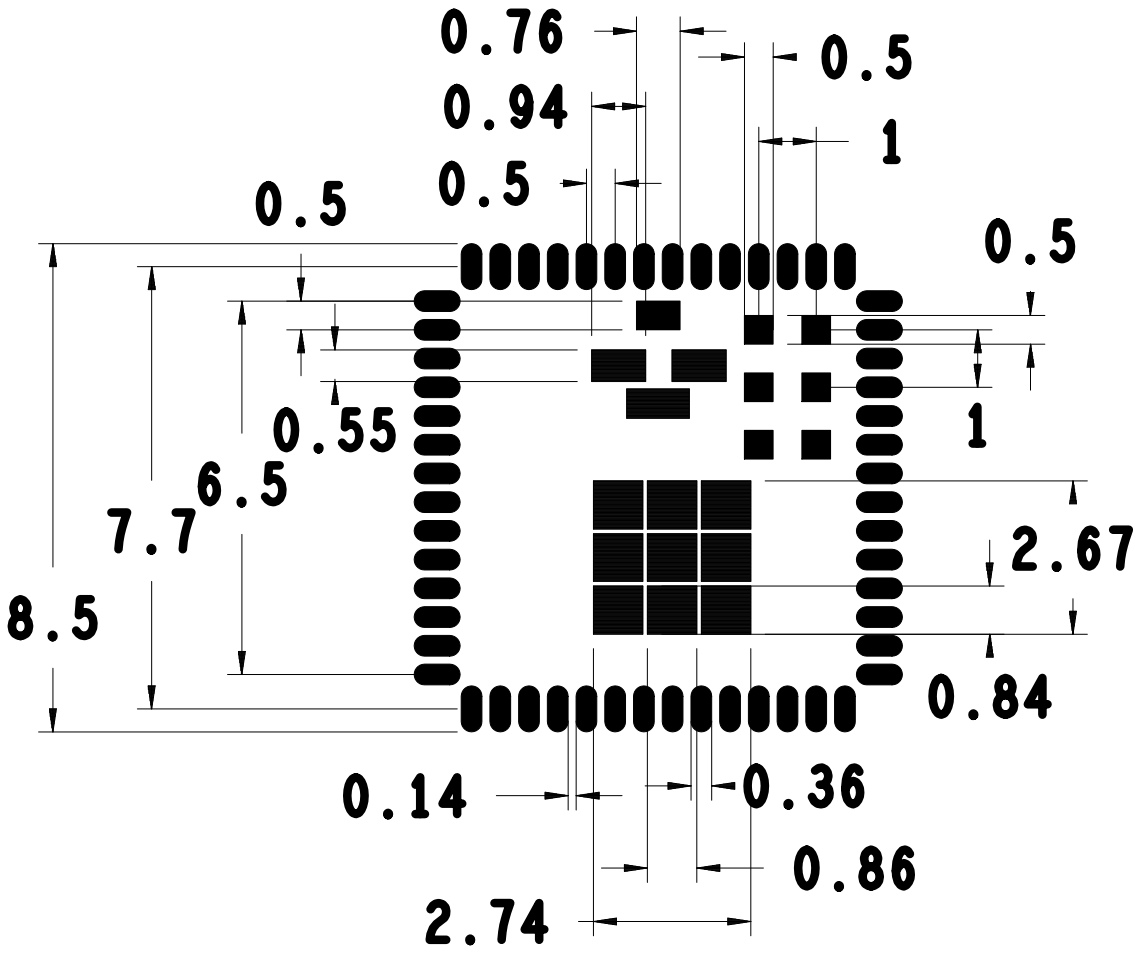

Figure 2. 63-Pin LGA Solder Mask Pattern

2.2 63-Pin LGA Solder Paste Stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. Figure 3 shows a recommended solder stencil pattern. Stencil thickness should be approximately 0.1 mm.

Other patterns and opening sizes can be used if too much solder is being applied. See Section 2.2.1, “LGA Problems with Excess Solder for more information.

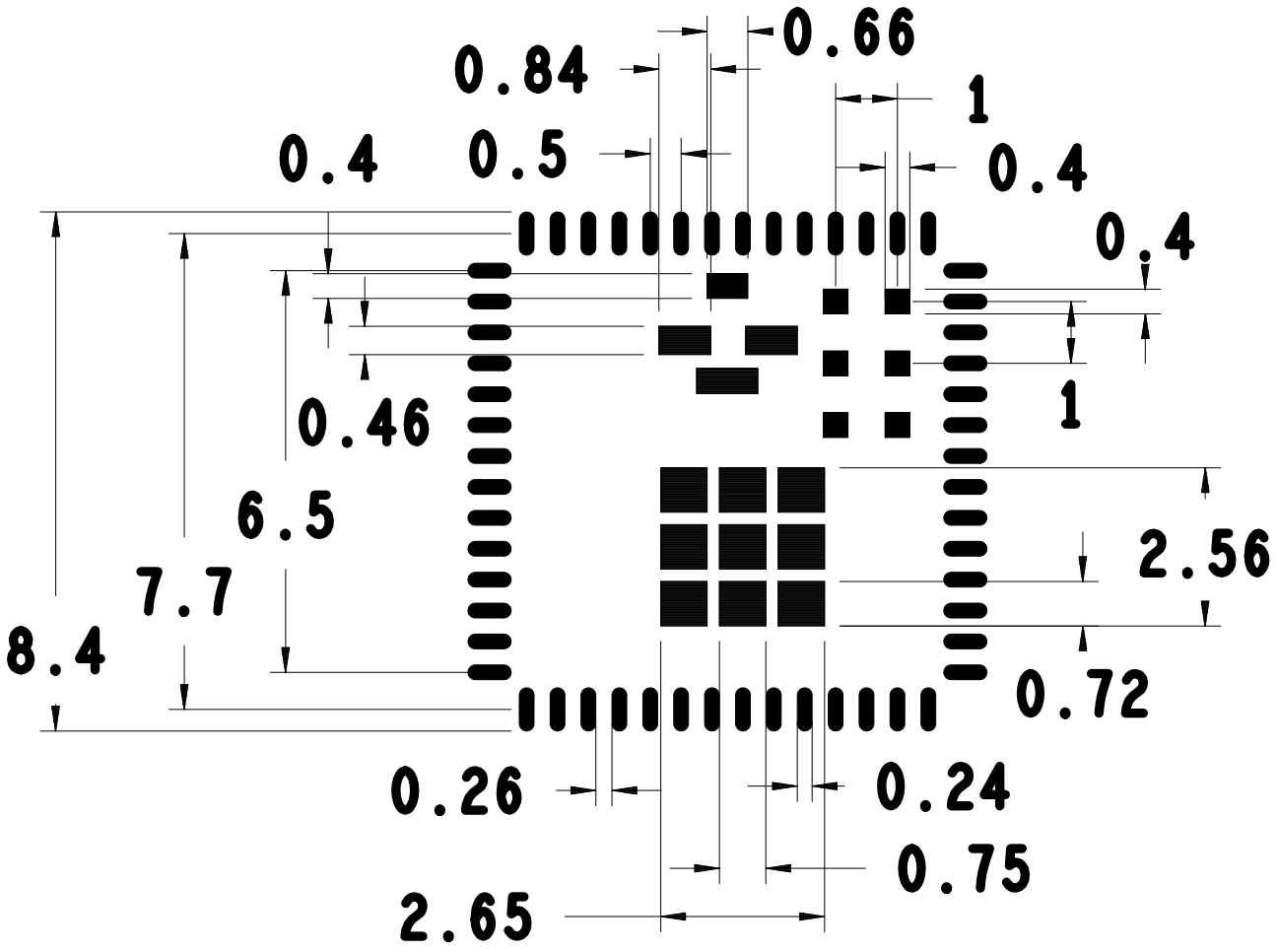

Figure 3. 63-pin LGA Solder Stencil Pattern

2.2.1 LGA Problems with Excess Solder

Excess solder may cause the LGA to “float” or bridge between the package contacts. To use the correct amount of solder paste applied to the PCB, take into consideration the following:

- Stencil thickness
- Other components mounted on the PCB
- Manufacturing equipment
- Assembly house experience

3 63-Pin LGA Package Dimensions

Figure 4 shows the LGA 63 package dimensions.

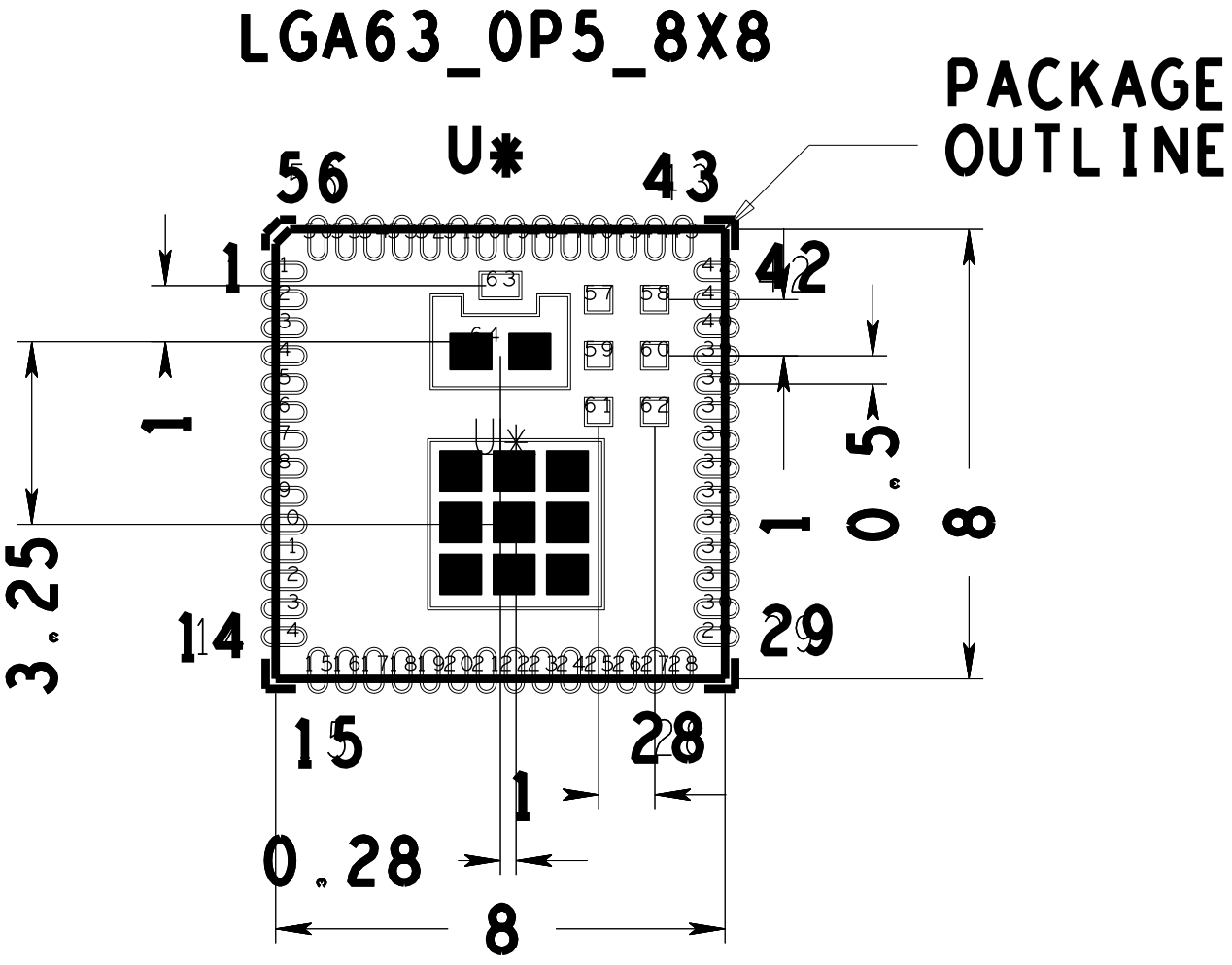

Figure 4. LGA Package Dimensions

3.1 63-pin LGA Device Marking Details

The MKW2x devices are in the 63-pin LGA (8x8mm), Case 2234-01. The following figure show device marking examples for the LGA device.

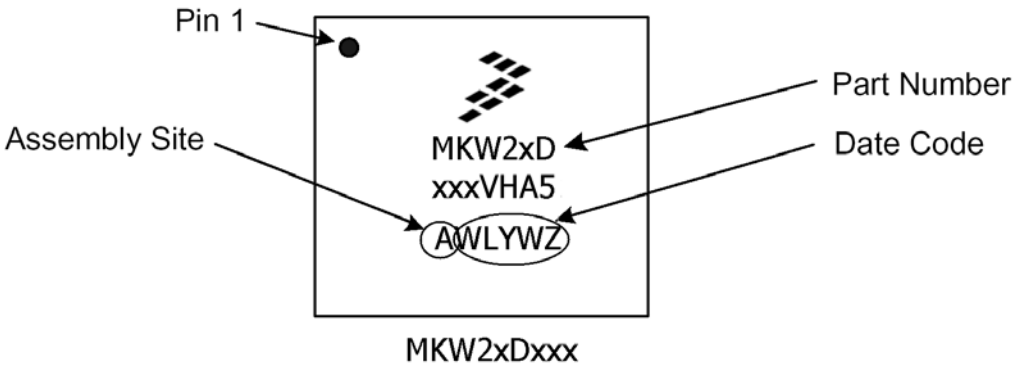

Figure 5. LGA-63 Device Marking

4 63-Pin LGA Soldering Profile

Figure 6 shows the soldering profile Freescale uses and recommended for the MKW2x LGA 63 package, in a board size approximately 2.08”x2.08”.

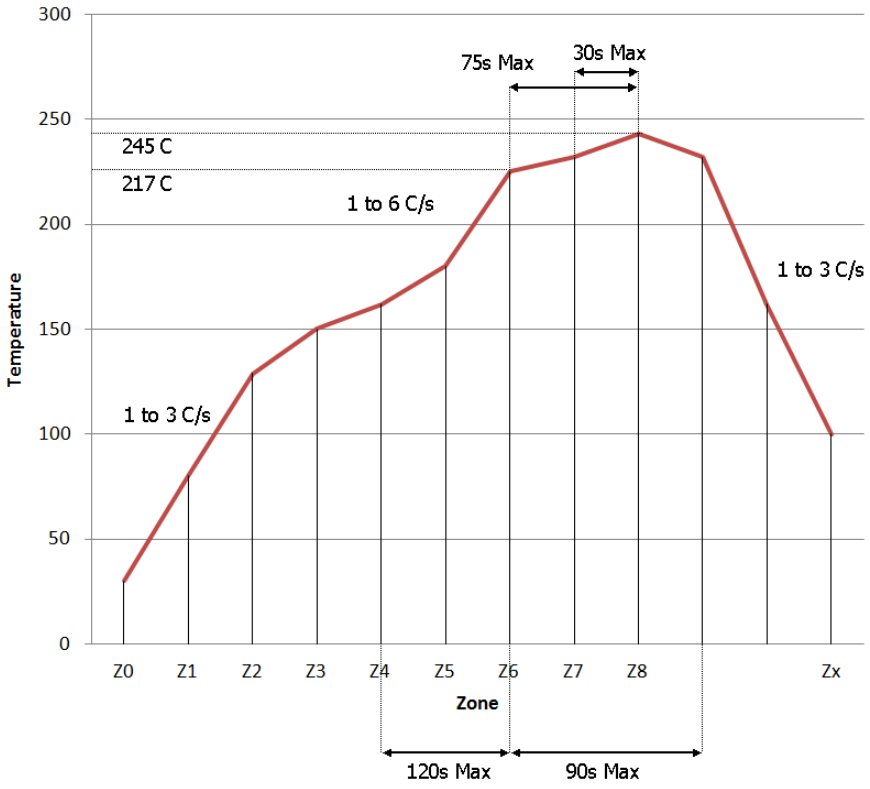

Figure 6. LGA-63 Soldering Profile

5 Design and Board Layout Considerations

To have successful wireless hardware development, the proper device footprint, RF layout, circuit matching, antenna design and RF measurement capability are essential. RF circuit design, layout and antenna design are specialties requiring investment in tools and experience. With Freescale's available hardware reference designs, RF design considerations and guidelines herein, hardware engineers can successfully design IEEE 802.15.4 radio boards with good performance.

The device footprint and layout are critical and affect the RF performance by the design implementation. For these reasons, use of the Freescale recommended RF hardware reference designs are important for first time successful board performance. Additionally, the reference platforms have been optimized for radio performance. If the recommended footprint and design are followed exactly in the RF region of the board; sensitivity, output power, harmonic and spurious radiation, and range will have a high likelihood first time success.

The following subsections describe important considerations when implementing a wireless hardware design starting with the device footprint, RF circuit implementation and antenna selection. Figure 7 shows an example of a typical layout exhibiting the critical RF section which should be copied exactly for best radio performance. The less critical layout area can be modified without degrading radio performance.

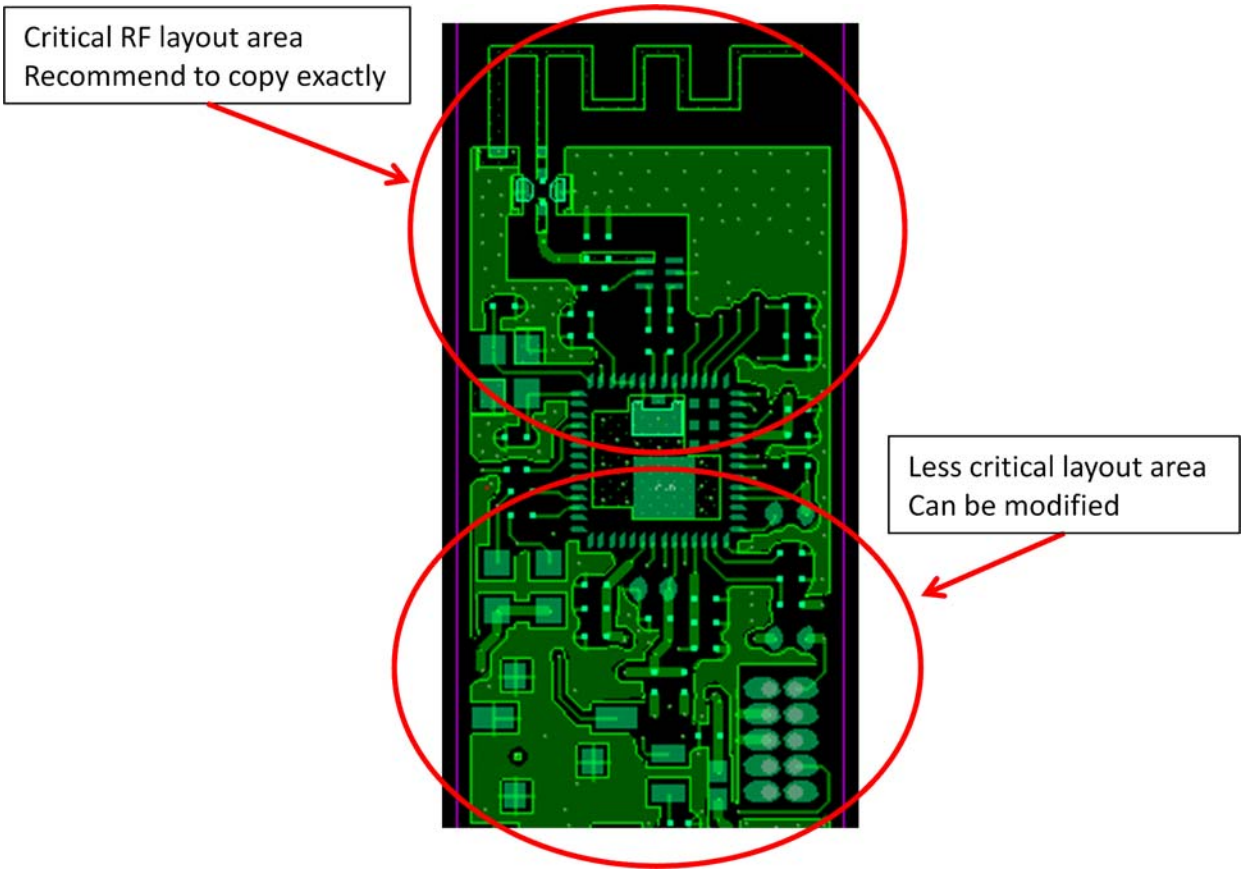

Figure 7. Critical Layout Areas

5.1 MKW2x Device Footprint

The performance of the wireless link is largely influenced by the devices footprint. As a result, a great deal of care has been put into creating a footprint so that receiver sensitivity and output power are optimized allowing board matching and component count to be minimized. Freescale highly recommends copying the die flag exactly as it is shown in Figure 8; this includes via locations as well. Deviation from these parameters can cause performance degradation.

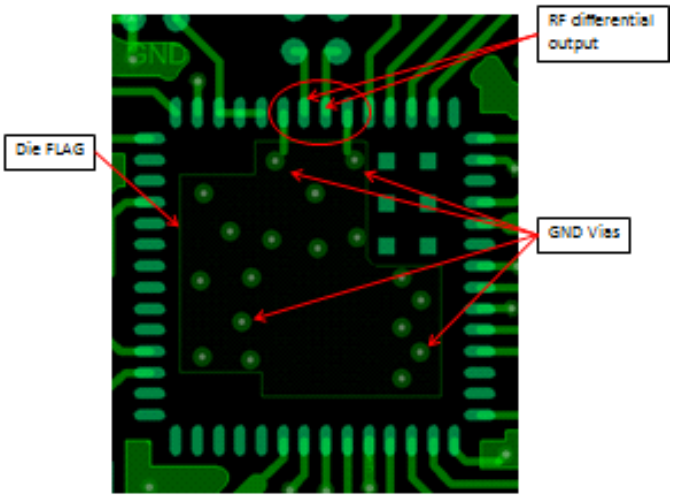

Figure 8. MKW2x Device Footprint

Figure 8 shows the critical areas of the device die flag. These are the following:

- Ground vias and locations
- RF differential output and ground traces
- Die flag shape
- Test pins

5.2 RF Circuit Topology and Matching

Transmission lines take on a variety of shapes such as microstrip, coplanar waveguide, and stripline to name a few. For 802.15.4 applications built on FR4 substrates, the methods of transmission lines typically take the form of microstrip or coplanar waveguide (CPW). These two structures are defined by the dielectric constant of the board material, trace width, board thickness between the trace and the ground. Additionally for CPW, the gap between the trace and the top edge ground plane. These parameters are used to define the characteristic impedance of the transmission line (trace) that is used to convey the RF energy between the radio and the antenna.

Typically, the RF ports from the 802.15.4 radios are differential or balanced. These ports RF impedances at the radio are in the range of 100 Ohms. Freescale's applications typically use a balun to transform the balanced signals to a single ended output with a characteristic impedance of 50 ohms. Therefore, Freescale recommends an antenna with a 50 ohm feed.

A good practice is to review all components in the RF section of a layout and remove all excess metal. In addition, avoid routing of traces near or parallel to RF transmission lines or RF bias lines. RF signals will couple to these pieces of metal, which are usually connected to ground and can distort the signal. Maintaining a continuous ground under an RF trace is critical to maintaining the characteristic impedance of that trace. Avoid any routing on the ground layer that will result in disrupting the ground under the RF traces.

Complexity is the main factor that will determine whether the design of an application board can be two-layer, four-layer, or more. The recommended board stackup for either a two-layer or four-layer board design is as follows:

- Two-layer stackup
  - Top — RF routing of transmission lines, signals and ground
  - Bottom — RF reference ground, signal routing and general ground
- 4-layer stackup
  - Top — RF routing of transmission lines
  - L2 — RF reference ground
  - L3 — DC power
  - Bottom — Signal routing

For more information, see Freescale application note AN2731, Compact Integrated Antennas.

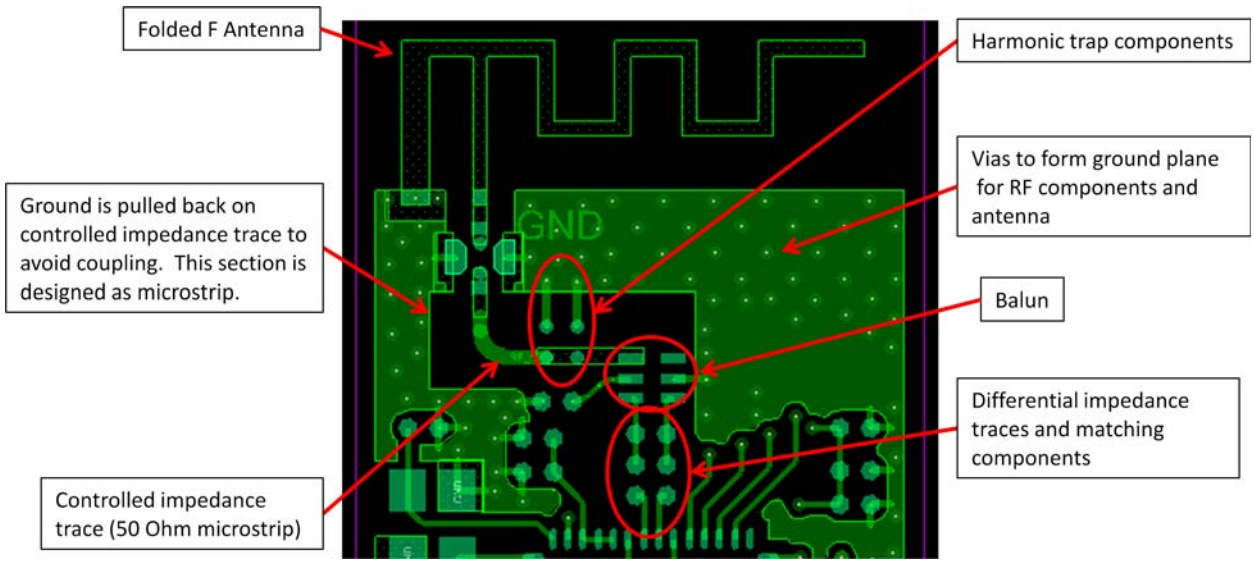

Figure 9. RF Matching Network

- Differential impedance traces should be kept as short as possible
  - Length traces are lossy and inductive
  - Keep trace lengths short between device differential port and balun
- Notice how all traces and grounds are far away from the RF traces (both differential and single ended).

- In Figure 9 the microstrip topology is used. In CPW, the gap to ground is integral to maintaining the characteristic impedance.
- When a harmonic trap is employed, it is easier to use a microstrip transmission line rather than coplanar waveguide (CPW) between the balun and antenna because the constant gap required for CPW is disrupted.

- Harmonic trap components
  - Lengths of trace are added between the component and ground to add effective inductance.
  - Notice the components' long trace length to ground. This creates a tuned resonance.
- Grounding is imperative
  - Vias are used to form ground planes for RF components.
  - Note antenna considerations in the next section.
  - Caution when routing traces near RF lines. PCB traces can act as effective radiators at RF frequencies.
- Examples of PCB Parasitics:
  - At 2.4 GHz, a 10 mil wide PCB trace 275 mils long on 32 mil FR4 is equivalent to a 3.2 nH inductor, +j73 Ohms.
  - A 10 mil via in 32 mil FR4 is about 0.5 to 1 nH.

5.3 Antenna Considerations

There are a large variety of antenna types available to choose from when designing for a wireless system. There are small footprint chip antennas, trace antennas, loop monopole and dipole to name a few, each with their own set of pros and cons depending on the goal of the application. Freescale recommends using one of the proven antenna implementations used in many of our hardware reference designs. Figure 10 shows a folded F antenna used in a small USB dongle. This is a low cost trace implementation that performs very well. If a smaller board footprint is required, the use of a chip antenna would be better suited with the trade off of cost, performance, and range. For more information on compact antenna designs, see Freescale application note AN2731, Compact Integrated Antennas.

For this illustration, Figure 10 uses the folded F trace antenna as an example of what the hardware engineer should be aware of when designing a board layout for a wireless node.

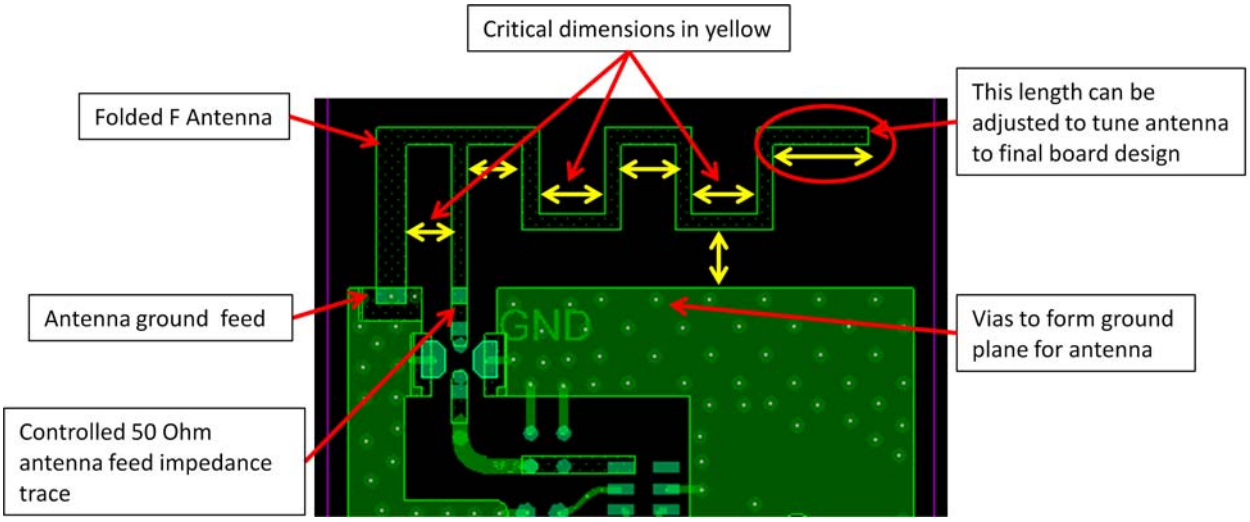

Figure 10. Antenna Network

Steps to good antenna performance:

- Be mindful of critical dimensions:
  - Notice the critical dimensions of the trace antenna. These should be copied exactly.
  - Customer final board sizes may differ from Freescale's reference designs. As a result, the last leg of the trace antenna should be made longer to allow for final board tuning.
  - Antenna tuning may be required to operate at the proper frequency. Ideally, the minimum return loss needs to be centered at 2445 MHz. 10 dB return loss looking into the antenna at the band edges is sufficient to achieve good range and receive sensitivity.
- Antenna impedance is 50 Ohm.
  - This is maintained from balun to antenna feed.
  - The example uses microstrip topology but co-planer waveguide with ground can also be used if desired. In this case the dimensions will change so care should be taken when changing from one topology to another.
- The antenna should be reasonably clear of metallic objects and oriented properly with the ground plane.
- Always check the antenna in its final environment, including the PCB, components, case enclosure, hand effects (if appropriate), battery, etc. Plastic and other materials in the near-field may cause detuning.
- Actual antenna performance can be evaluated in a variety of ways, such as range testing, measuring radiated signal level under controlled conditions, and characteristic testing in an anechoic chamber.

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